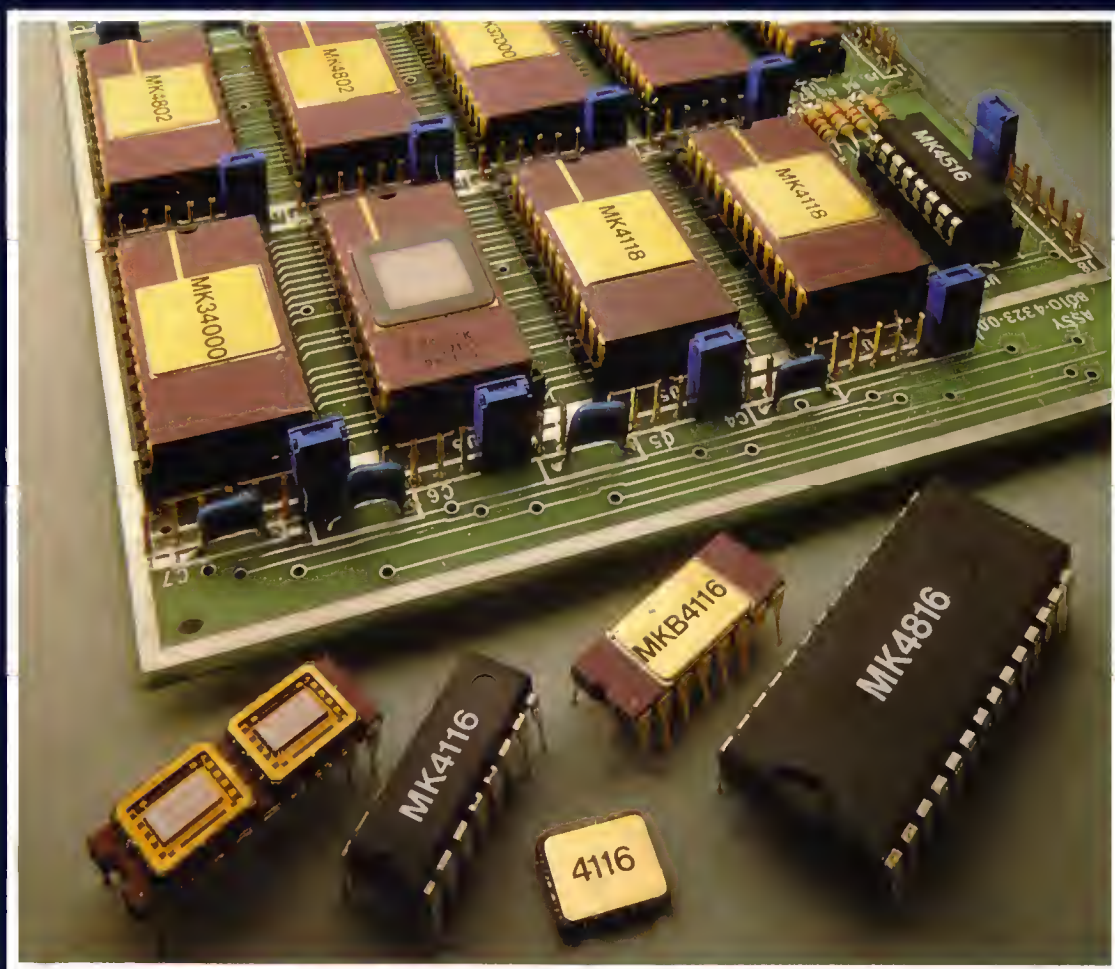


MOSTEK 1980

MEMORY DATA BOOK AND DESIGNERS GUIDE



**1980
Memory
Data Book
and
Designers
Guide**

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STD No. 14822

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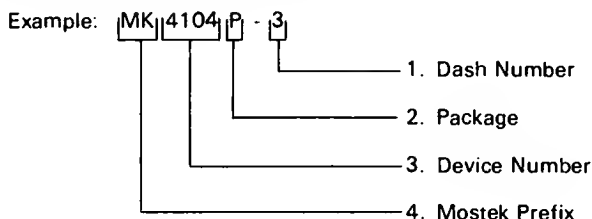
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ORDERING INFORMATION

Factory orders for parts described in this book should include a four-part number as explained below:



ORDER
PKG
INFORM

1. Dash Number

One or two numerical characters defining specific device performance characteristic.

2. Package

P - Gold side-brazed ceramic DIP
J - CER-DIP
N - Epoxy DIP (Plastic)
K - Tin side-brazed ceramic DIP
T - Ceramic DIP with transparent lid
E - Ceramic leadless chip carrier

3. Device Number

1XXX or 1XXXX - Shift Register, ROM
2XXX or 2XXXX - ROM, EPROM
3XXX or 3XXXX - ROM, EPROM
38XX - Microcomputer Components
4XXX or 4XXXX - RAM
5XXX or 5XXXX - Counters, Telecommunication and Industrial
7XXX or 7XXXX - Microcomputer Systems

4. Mostek Prefix

MK-Standard Prefix

MKB-100% 883B screening, with final electrical test at low, room and high-rated temperatures.

MOSTEK®

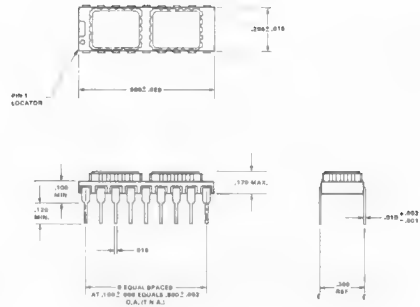
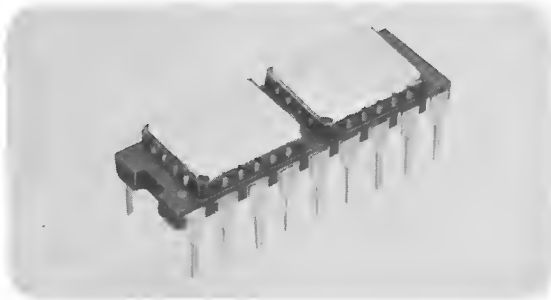
MEMORY PRODUCTS

Package Descriptions

ORDER
PKG
INFORM

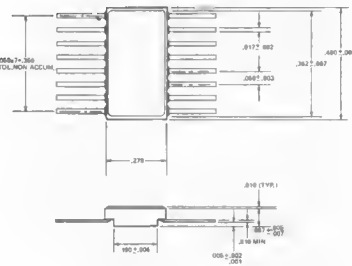
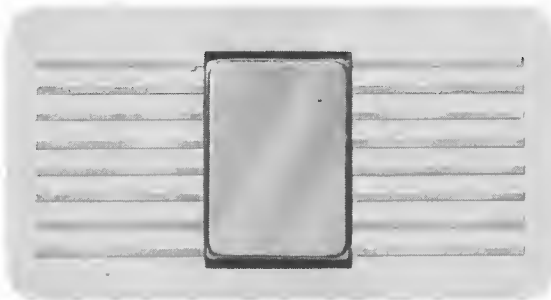
Dual-In-Line Double Density Ceramic Package (D)

18 Pin



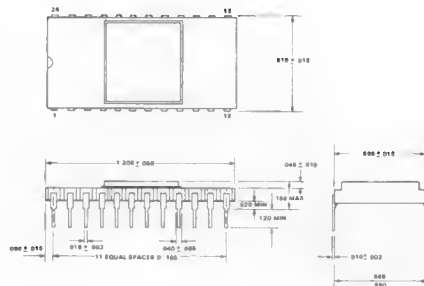
Ceramic Flat Package (F)

16 Pin

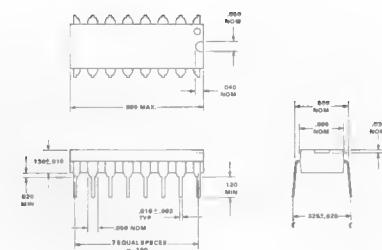
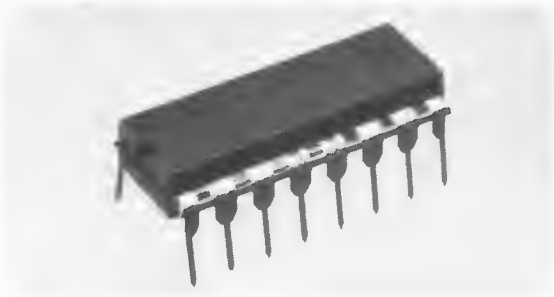


EPROM Hermetic Package (T)

24 Pin

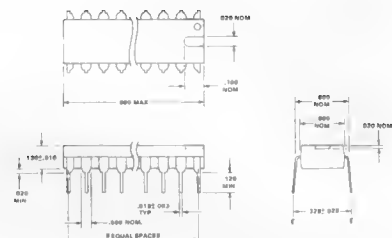
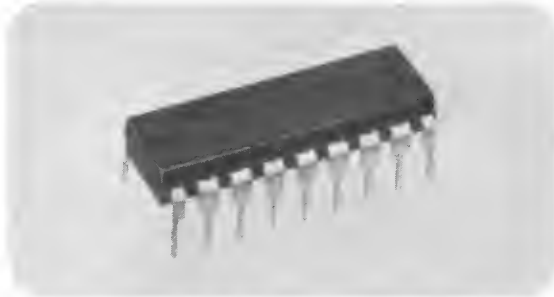


Plastic Dual-In-Line Package (N) 16 Pin



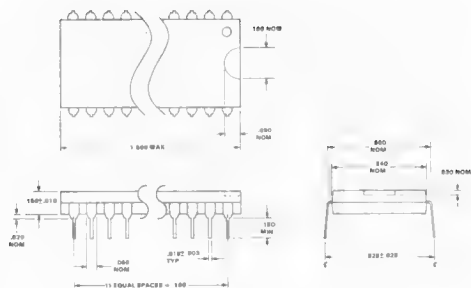
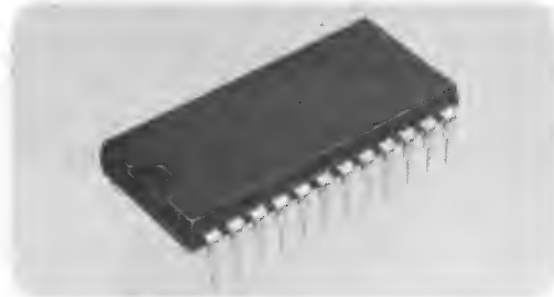
NOTE: Overall length includes .008 flap on either end of package

Plastic Dual-In-Line Package (N) 18 Pin



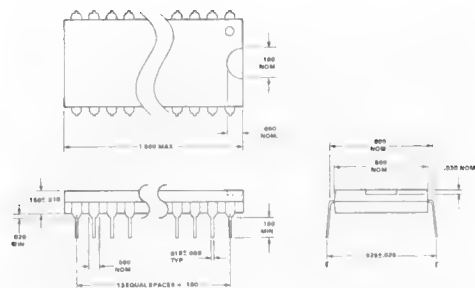
NOTE: Overall length includes .008 flap on either end of package

Plastic Dual-In-Line Package (N) 24 Pin



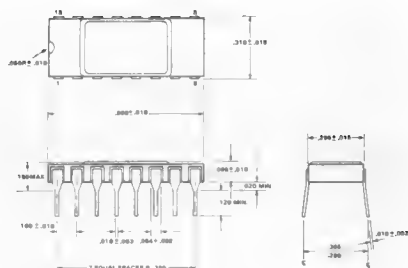
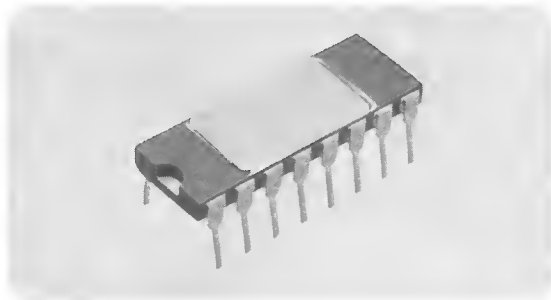
NOTE: Overall length includes .008 flap on either end of package

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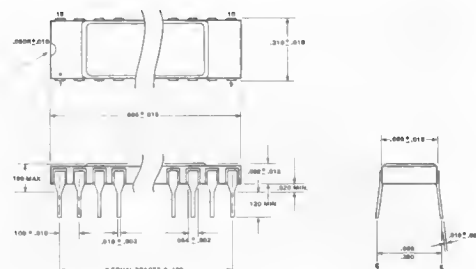
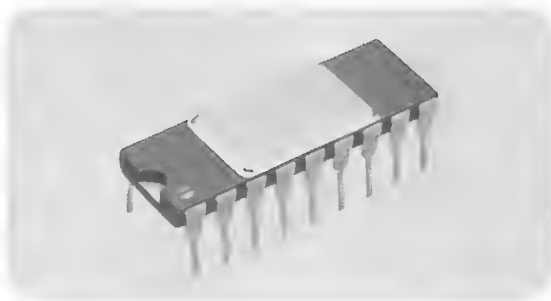


NOTE: Overall length includes .008 flap on either end of package

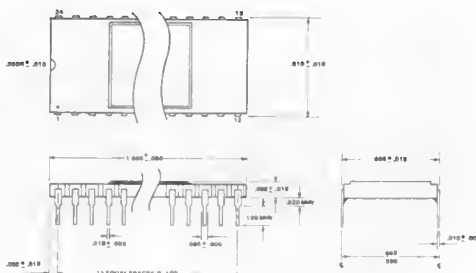
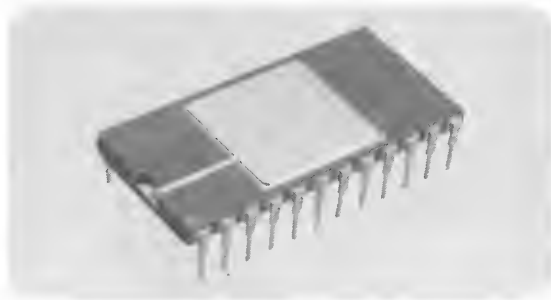
Ceramic Dual-In-Line Package (P)
16 Pin

ORDER
PKG
INFORM

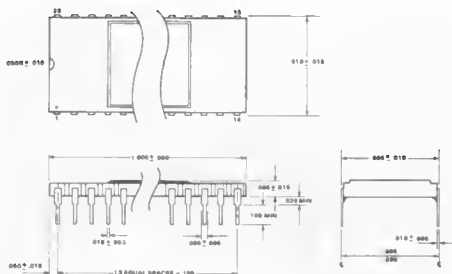
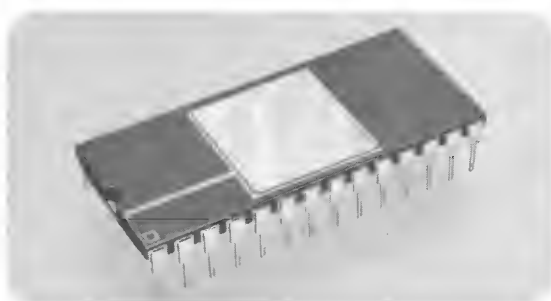
Ceramic Dual-In-Line Package (P)
18 Pin



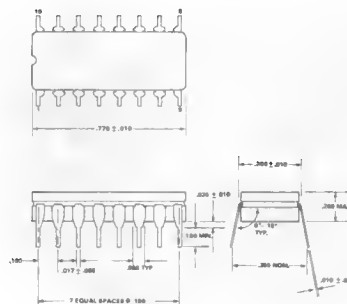
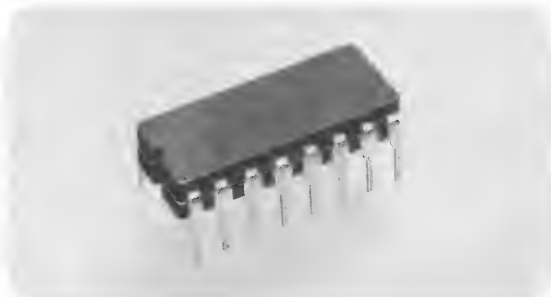
Ceramic Dual-In-Line Package (P)
24 Pin



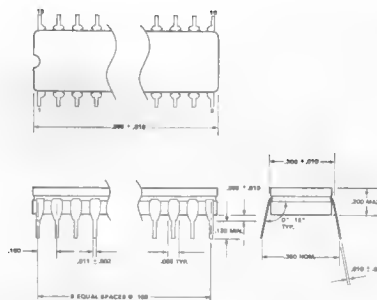
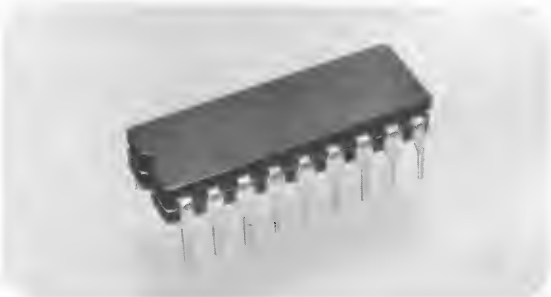
Ceramic Dual-In-Line Package (P)
28 Pin



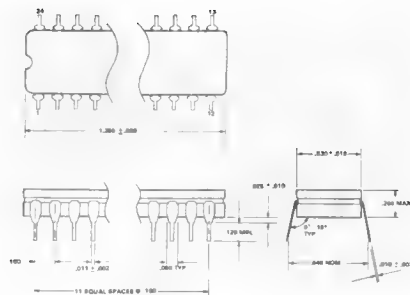
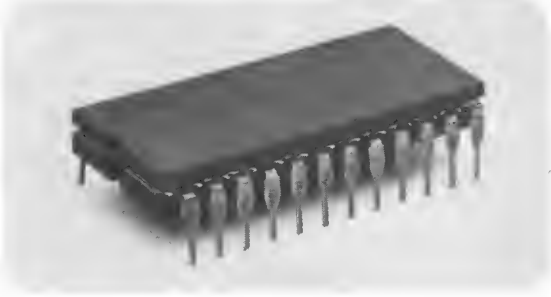
Cerdip Hermetic Packaging (J) 16 Pin



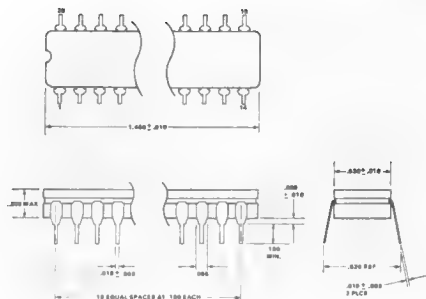
Cerdip Hermetic Packaging (J) 18 Pin



Cerdip Hermetic Packaging (J) 24 Pin



Cerdip Hermetic Packaging (J) 28 Pin



Leadless Hermetic Chip Carrier (E) 18 Pin

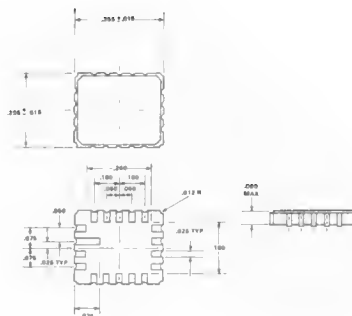
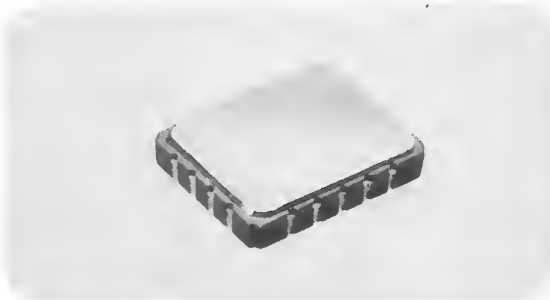


Figure A

Leadless Hermetic Chip Carrier (E) 18 Pin

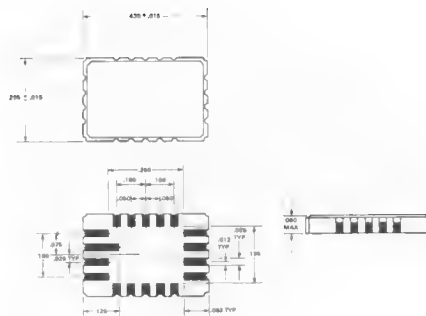
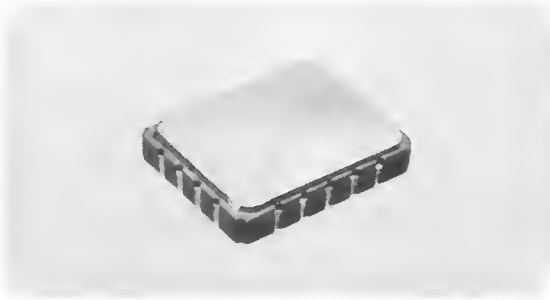
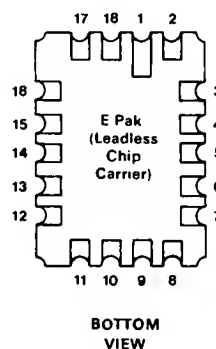


Figure B

E-PACK CARRIER PINOUT

Pin #	MK4104	MK4116	* MK4516	** MK4164
1	A ₀	V _{BB}	RFSH	RFSH
2	A ₁	D _{IN}	D _{IN}	D _{IN}
3	A ₂	WE	WRITE	WRITE
4	A ₃	RAS	RAS	RAS
5	A ₄	N/C	N/C	N/C
6	A ₅	A ₀	A ₀	A ₀
7	D _{OUT}	A ₂	A ₂	A ₂
8	WE	A ₁	A ₁	A ₁
9	V _{SS}	V _{DD}	V _{CC}	V _{CC}
10	CE	V _{CC}	N/C	A ₇
11	D _{IN}	A ₅	A ₅	A ₅
12	A ₁₁	A ₄	A ₄	A ₄
13	A ₁₀	A ₃	A ₃	A ₃
14	A ₉	N/C	N/C	N/C
15	A ₈	A ₆	A ₆	A ₆
16	A ₇	D _{OUT}	D _{OUT}	D _{OUT}
17	A ₆	CAS	CAS	CAS
18	V _{CC}	V _{SS}	V _{SS}	V _{SS}



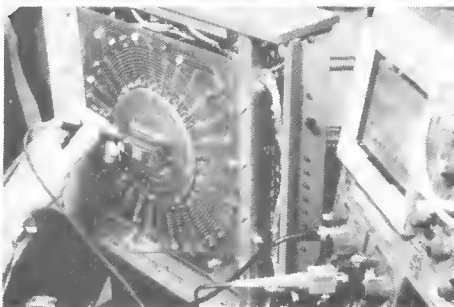
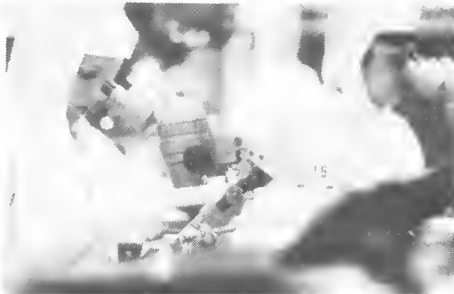
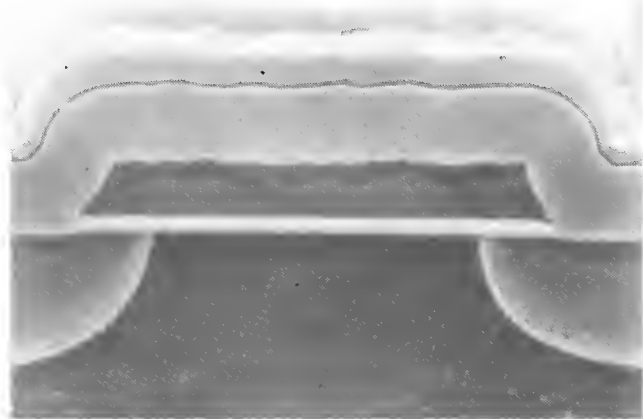
* The chip carrier for MK4116 and MK4516 will be per Figure A.

** The chip carrier for MK4164 will be per Figure B.

(E-PACKS for MK4516 and MK4164 will be offered at a later date)

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Mostek - Technology For Today And Tomorrow



SALES
OFFICES

TECHNOLOGY

From the beginning, Mostek has been recognized as an innovator. In 1970, Mostek developed the MK4006 1K dynamic RAM and the world's first single-chip calculator circuit, the MK6010. These technical breakthroughs proved the benefits of ion-implantation and cost-effectiveness of MOS. Now, Mostek represents one of the industry's most productive bases of MOS/LSI technology. Each innovation - in memories, microcomputers and telecommunications - adds to that technological capability.

QUALITY

The worth of a Mostek product is measured by its quality. How well it's designed, manufactured and tested. How well it works in your system.

In design, production and testing, our goal is meeting the spec every time. This goal requires a strict discipline, both from the company and from the individual. This discipline, coupled with a very personal pride, has driven Mostek to build in quality at every level, until every product we take to the market is as well-engineered as can be found in the industry.

PRODUCTION CAPABILITY

Mostek's commitment to increasing

production capability has made us the world's largest manufacturer of dynamic RAMs. In 1979 we shipped 25 million 4K and 16K dynamic RAMs. We built our first telecommunication tone dialer in 1974; since then, we've shipped over 5 million telecom circuits. The MK3870 single-chip microprocessor is also a large volume product with over two million in application around the world. To meet the demand for our products, production capability must be constantly increased. To accomplish this, Mostek has been in a constant process of expanding and refining our production capabilities.

THE PRODUCTS

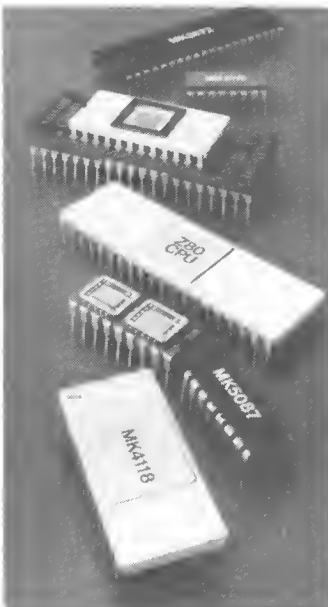
Telecommunications and Industrial Products

Mostek has made a solid commitment to telecommunications with a new generation of products, such as Integrated Pulse Dialers, Tone Dialers, CODECs, monolithic filters, tone receivers, A/D converters and counter time-base circuits.

Since 1974 over five million telecom circuits have been shipped, making Mostek the leading supplier of tone/pulse dialers and CODECs.

Memory Products

Through innovations in both circuit



design, wafer processing and production, Mostek has become the industry's leading supplier of memory products.

An example of Mostek leadership is our new BYTEWYDE™ family of static RAMs, ROMs, and EPROMs. All provide high performance, N words x 8-bit organization and common pin configurations to allow easy system upgrades in density and performance. Another important product area is fast static RAMs. With major advances in technology, Mostek static RAMs now feature access times as low as 55 nanoseconds. With high density ROMs and PROMs, static RAMs, dynamic RAMs and pseudostatic RAMs, Mostek now offers one of industry's broadest and most versatile memory families.

Microcomputer Components

Mostek's microcomputer components are designed for a wide range of applications.

Our Z80 family is the highest performance 8-bit microcomputer available today. The MK3870 family is one of the industry's most popular 8-bit single-chip microcomputers, offering upgrade options in ROM, RAM, and I/O, all in the same socket. The MK3874 EPROM version supports and prototypes the entire family.

Microcomputer Systems

Supporting the entire component product

line is the powerful MATRIX™ micro-computer development system, a Z80-based, dual floppy-disk system that is used to develop and debug software and hardware for all Mostek microcomputers.

A software operating system, FLP-80DOS, speeds and eases the design cycle with powerful commands. BASIC, FORTRAN, and PASCAL are also available for use on the MATRIX.

Mostek's MD Series™ features both stand-alone microcomputer boards and expandable microcomputer boards. The expandable boards are modularized by function, reducing system cost because the designer buys only the specific functional modules his system requires. All MDX boards are STD-Z80 BUS compatible.

The STD-Z80 BUS is a multi-sourced motherboard interconnect system designed to handle any MDX card in any card slot.

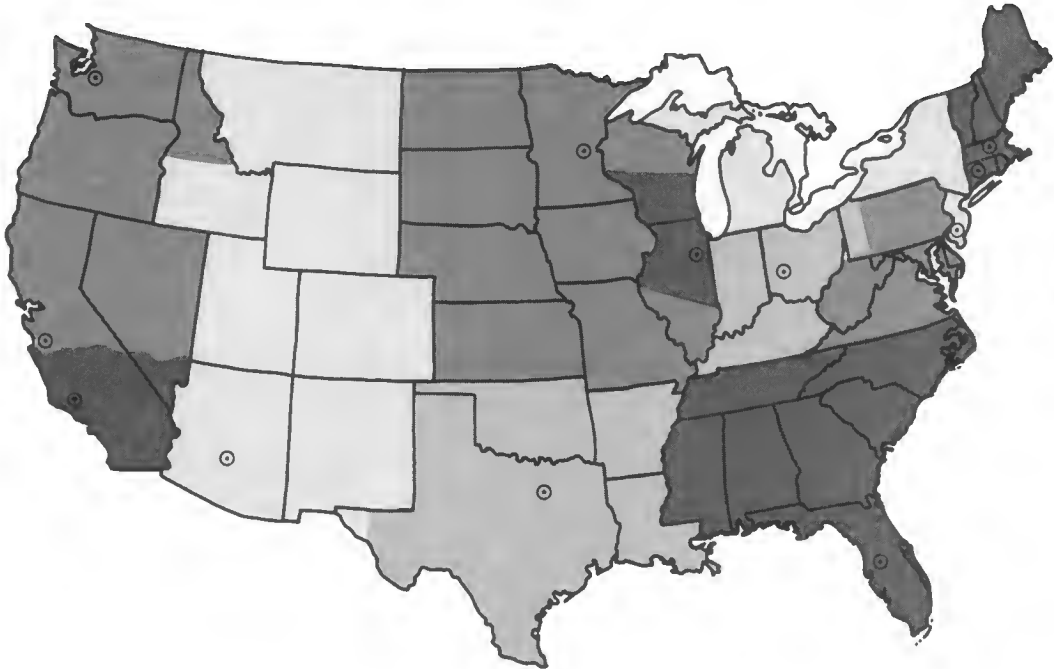
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(49) 2102-280.24
Telex - 8585180

Siegfried Ecker

Konigsberger Strasse 2
D-6120 Michelstadt
(49) 6061-2233
Telex - 4191830

Matronic GmbH

Lichtenberger Weg 3
D-7400 Tubingen
(49) 7071-24.43.31
Telex - 726.28.79

Dema-Electronic GmbH

Blutenstrasse 21
D-8 Munchen 40
(49) 89-288018
Telex - 28345

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199-203 Hennessy Road
Wanchai, Hong Kong
(5)-72.93.76
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Compres S.r.l.
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I-20092 Cinisello Balsamo
(39) 2-928.08.09/928.03.45
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4th Floor, Shindo Bldg.
3-12-5 Uchikanda,
Chiyoda-Ku,
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(81) 3-254.27.51
Telex - 25761

Teijin Advanced Products Corp

1-1 Uchisaiwai-Cho
2-Chome Chiyoda-Ku
Tokyo, 100
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Telex - 23548

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Room 303-Tae Sung Bldg.
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Jongro-Ku
Seoul
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(020) 428. 933
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Rodelikta
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Transvaal
789-1400
Telex - 8-0838 SA

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Comelta S.A.
Cia Electronica Tecnicas Aplicadas
Consejo de Ciento, 204
Entlo 3A
Barcelona 11
(34) 3-254.66.07/08
Telex - 19394

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S-11251 Stockholm
(46) 8-13.21.60
Telex - 10689

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Memotec AG
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(41) 63-28 11 22
Telex - 68636

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UNITED KINGDOM

Celdis Limited
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Telex - 848370

Distronic Limited

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Elizabeth Way,
Herlow
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Telex - 81387

A.M. Lock Co., Ltd.

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Chadderton,
Oldham, Lancashire
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Telex - 669971

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645 High Road,
Seven Kings,
Ilford,
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1980 MEMORY DATA BOOK

I	Table of Contents	TABLE OF CONTENTS
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MOSTEK®

16K-BIT READ ONLY MEMORY

MK34000(P/J/N)-3

FEATURES

- 2K x 8 organization with static interface
- 350ns max access time
- Single +5V $\pm 10\%$ power supply
- 330mW max power dissipation
- Contact programmed for fast turn-around

- Three programmable chip selects
- Inputs and three-state outputs — TTL compatible
- Outputs drive 2 TTL loads and 100pF
- RAM/EPROM pin compatible
- Pin compatible with Mostek's BYTEWYDE™ Memory Family

DESCRIPTION

The MK34000 is a new generation N-channel silicon gate MOS Read Only Memory circuit organized as 2048 words by 8 bits. As a state-of-the-art device, the MK34000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with highest possible performance, while maintaining low power dissipation and wide operating margins.

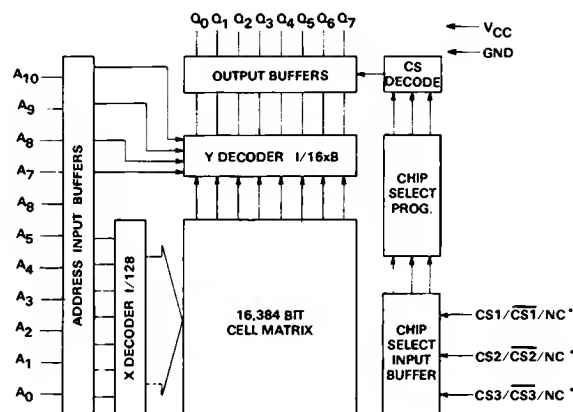
The MK34000 requires a single +5 volt ($\pm 10\%$ tolerance) power supply and has complete TTL compatibility at all inputs and outputs (a feature made possible by Mostek's ion-implantation technique). The three chip select inputs can be programmed for any desired combination of active high's or low's or even an optional "DON'T CARE" state. The convenient static operation of the MK34000 coupled with the programmable chip select inputs and three-state TTL

compatible outputs results in extremely simple interface requirements.

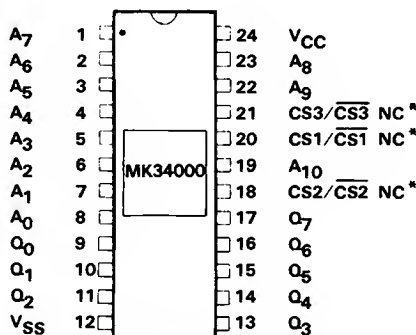
An outstanding feature of the MK34000 is the use of contact programming over gate mask programming. Since the contact mask is applied at a later processing stage, wafers can be partially processed and stored. When an order is received, a contact mask, which represents the desired bit pattern, is generated and applied to the wafers. Only a few processing steps are left to complete the part. Therefore, the use of contact programming reduces the turnaround time for a custom ROM.

Any application requiring a high performance, high bit density ROM can be satisfied by this device. The MK34000 is ideally suited for 8-bit microprocessor systems such as those which utilize the Z80 or F8. The MK34000 also provides significant cost advantages over PROM.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



*Programmable Chip Selects

ROMS

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to V_{SS}	-0.5V to +7V
Operating Temperature T_A (Ambient)	0°C to +70°C
Storage Temperature - Ceramic (Ambient)	-65°C to +150°C
Storage Temperature - Plastic (Ambient)	-55°C to +125°C
Power Dissipation	1 Watt

*Stresses greater than these listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

($V_{CC} = 5V \pm 10\%$; $0^\circ C \leq T_A \leq +70^\circ C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	6
V_{IL}	Input Logic 0 Voltage	-0.5		0.8	V	
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	V	

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = 5V \pm 10\%$; $0^\circ C \leq T_A \leq +70^\circ C$)⁶

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC}	V_{CC} Power Supply Current		60	mA	1
I_{IL}	Input Leakage Current		10	μA	2
I_{OL}	Output Leakage Current		10	μA	3
V_{OL}	Output Logic 0 Voltage @ $I_{OUT} = 3.3mA$		0.4	V	
V_{OH}	Output Logic 1 Voltage. @ $I_{OUT} = -220 \mu A$	2.4	V_{CC}	V	

AC ELECTRICAL CHARACTERISTICS

($V_{CC} = 5V \pm 10\%$; $0^\circ C \leq T_A \leq +70^\circ C$)⁶

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{ACC}	Address to output delay time		350	ns	4
t_{CS}	Chip select to output delay time		175	ns	4
t_{CD}	Chip deselect to output delay time		150	ns	4

CAPACITANCE

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_{IN}	Input Capacitance	6	8	pF	5
C_{OUT}	Output Capacitance	10	15	pF	5

NOTES:

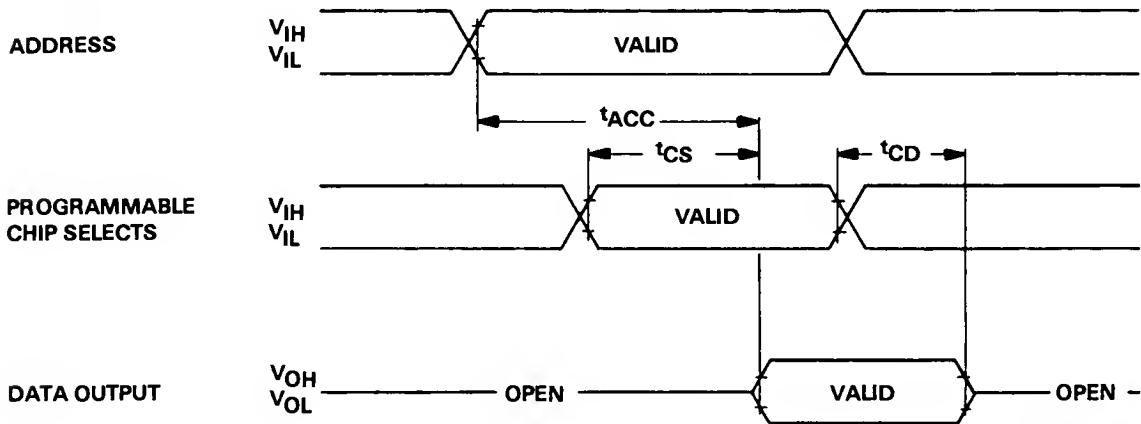
1. All inputs 5.5V, Data Outputs open.
2. $V_{IN} = 0V$ to 5.5V ($V_{CC} = 5V$)
3. Device unselected; $V_{OUT} = 0V$ to 5.5V.
4. Measured with 2 TTL loads and 100pF, transition times = 20ns.

5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:

$$C = \frac{I \Delta t}{\Delta V} \text{ with current equal to a constant } 20mA.$$

6. A minimum 2ms time delay is required after the application of V_{CC} (+5) before proper device operation is achieved.

TIMING DIAGRAM



The chip select inputs can be user programmed so that either the input is enabled by a Logic 0 voltage (V_{IL}), a Logic 1 voltage (V_{IH}), or the input is always enabled (regardless of the state of the input). See chart below for programming instructions.

ROMS

MOSTEK 34000 ROM PUNCHED CARD CODING FORMAT (1)

FIRST CARD

COLS	INFORMATION FIELD
1-30	Customer
31-50	Customer Part Number
60-72	Mostek Part Number (2)

SECOND CARD

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

THIRD CARD

1-5	Mostek Part Number (2)
33	Chip Select One "1" = CS_1 or "0" = $\overline{CS_1}$ or "2" = Don't Care
35	Chip Select Two "1" = CS_2 or "0" = $\overline{CS_2}$ or "2" = Don't Care
37	Chip Select Three "1" = CS_3 or "0" = $\overline{CS_3}$ or "2" = Don't Care

FOURTH CARD

1-9	Data Format (3)
15-28	Logic - ("Positive Logic" or "Negative Logic")
35-57	Verification Code (4)

DATA FORMAT

128 data cards (16 data words/card) with the following format:

COLS	INFORMATION FIELD
1-4	Four digit octal address of first output word on card
5-7	Three digit octal output word specified by address in column 1-4
8-52	Next fifteen output words, each word consists of three octal digits.

NOTES:

1. Positive or negative logic formats are accepted as noted in the fourth card.
2. Assigned by Mostek; may be left blank.
3. Mostek punched card coding format should be used. Punch "Mostek" starting in column one.
4. Punches as: (e) VERIFICATION HOLD - i.e. customer verification of the data as reproduced by Mostek is required prior to production of the ROM. To accomplish this Mostek supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
(b) VERIFICATION PROCESS - i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification; (c) VERIFICATION NOT NEEDED - i.e. the customer will not receive a CVDS and production will begin immediately.

MOSTEK®

16K-BIT MOS READ-ONLY MEMORY

MK34073(P/J/N)-3

FEATURES

- ☐ 2K x 8 organization with static interface
- ☐ 350ns max access time
- ☐ Single +5V \pm 10% power supply
- ☐ 330mW max power dissipation
- ☐ Full ASCII compatible character sets (128 characters)
- ☐ Contains both Horizontal (5x8) and Vertical (5x7) character sets.
- ☐ Inputs and three-state outputs—TTL compatible
- ☐ Outputs drive 2 TTL loads and 100pF

DESCRIPTION

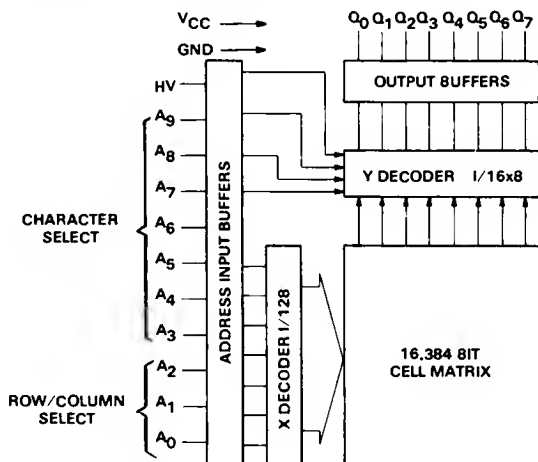
The MK34073 is a pre-programmed version of MOSTEK's high performance MK34000 16K bit ROM. The MK34073 incorporates advanced circuit techniques to provide maximum circuit density and reliability along with high speed (350ns access) and low power operation. The MK34073 requires a single +5 volt (\pm 10% tolerance) power supply and has complete TTL compatibility on all inputs and outputs.

The MK34073 is pre-programmed for character generator applications. It contains two separate character fonts for use in raster scan or matrix printer applications. Each font is ASCII compatible

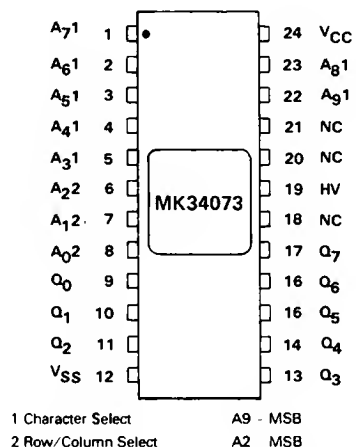
and contains augmented character sets with all upper and lower case characters. Font selection is accomplished by setting Pin 19 (HV) to a logic '1' ($V_{IN} \geq 2.0$ Volts) to select the 5 x 8 horizontal output character set or to a logic '0' ($V_{IN} \leq 0.8$ Volts) to select the 5 x 7 vertical output character set. Character selection is made by placing the ASCII code of the desired character on A3-A9 and row/column selection is made on A0-A2.

Electrical specifications for the MK34073 can be found on the MK34000 data sheet available from MOSTEK.

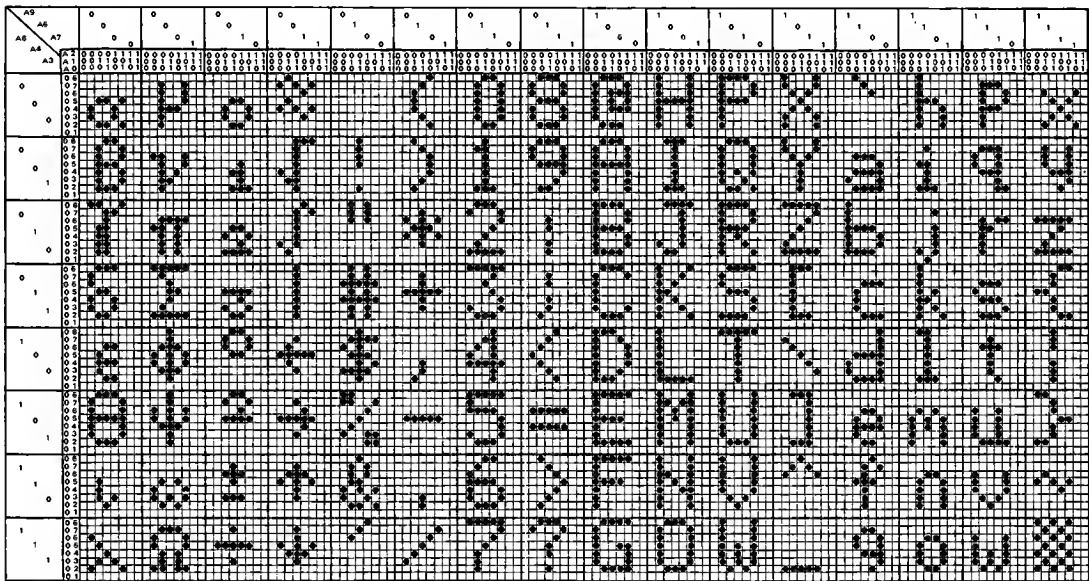
FUNCTIONAL DIAGRAM



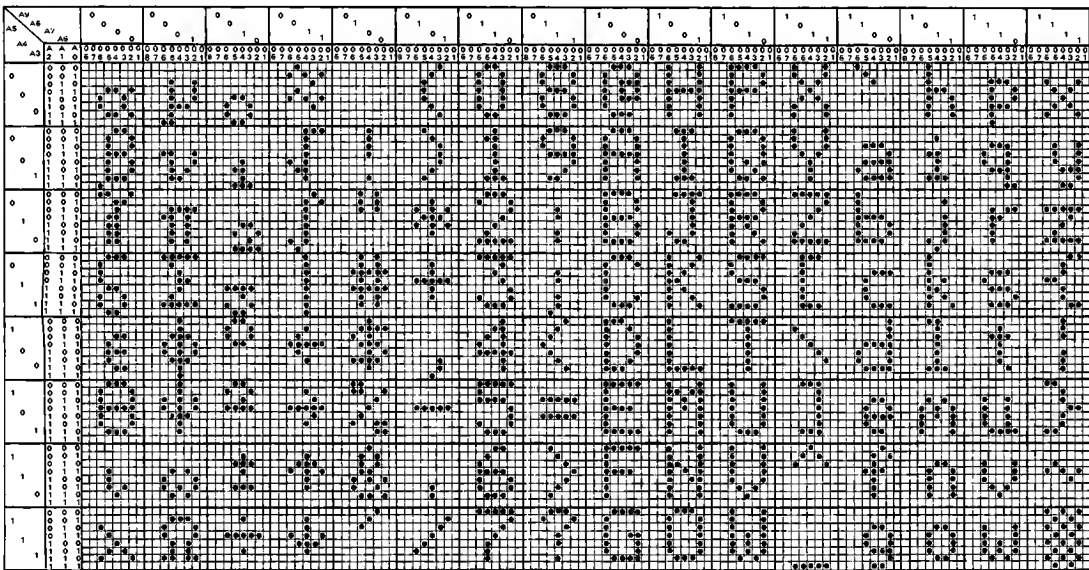
PIN CONNECTIONS



COLUMN OUTPUT (HV = 0)



HORIZONTAL OUTPUT (HV = 1)



A dot is representative of an output 'high' level.

MOSTEK®

64K-BIT READ-ONLY MEMORY

MK36000(P/J/N)-4/5

FEATURES

- MK36000 8K x 8 Organization—
"Edge Activated" * operation (\overline{CE})
- Access Time/Cycle Time

P/N	Access	Cycle
MK36000-4	250ns	375ns
MK36000-5	300ns	450ns
- Single +5V \pm 10% Power Supply
- Standard 24 pin DIP (EPROM Pin Out Compatible)

- Low Power Dissipation - 220mW Max Active
- Low Standby Power Dissipation—45mW Max.
(\overline{CE} High)
- On chip latches for addresses
- Inputs and three-state outputs-TTL compatible
- Outputs drive 2 TTL loads and 100 pF

DESCRIPTION

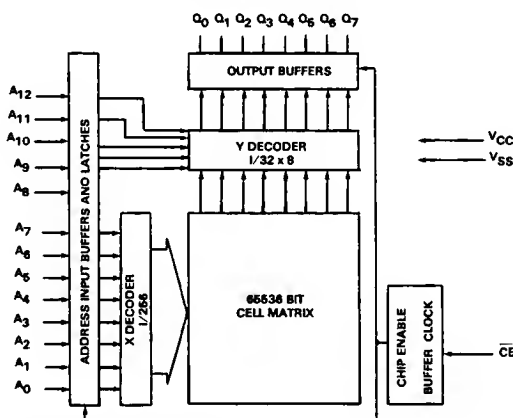
The MK36000 is a new generation N-channel silicon gate MOS Read Only Memory, organized as 8192 words by 8 bits. As a state-of-the-art device, the MK36000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating margins.

The MK36000 utilizes what is fast becoming an industry standard method of device operation. Use of a static storage cell with clocked control periphery allows the circuit to be put into an automatic low power standby mode. This is accomplished by maintaining the chip enable (\overline{CE}) input at a TTL high level. In this mode, power dissipation is reduced to typically 45mW, as compared to unlocked devices which

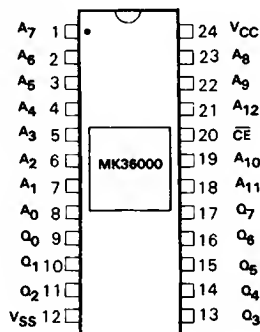
draw full power continuously. In system operation, a device is selected by the \overline{CE} input, while all others are in a low power mode, reducing the overall system power. Lower power means reduced power supply cost, less heat to dissipate and an increase in device and system reliability.

The edge activated chip enable also means greater system flexibility and an increase in system speed. The MK36000 features onboard address latches controlled by the \overline{CE} input. Once the address hold time specification has been met, new address data can be applied in anticipation of the next cycle. Outputs can be wire-OR'ed together, and a specific device can be selected by utilizing the \overline{CE} input with no bus conflict on the outputs. The \overline{CE} input allows the fastest access times yet available in 5 volt only

FUNCTIONAL DIAGRAM (MK36000)



PIN CONNECTIONS



PIN NAMES

A0-A12	Address	V _{SS}	GND
Q0-Q7	Outputs	\overline{CE}	Chip Enable
V _{CC}	+5V		

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to V _{SS}	-1.0V to +7V
Operating Temperature T _A (Ambient)	0°C to +70°C
Storage Temperature - Ceramic (Ambient)	-65°C to +150°C
Storage Temperature - Plastic (Ambient)	-55°C to +125°C
Power Dissipation	1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS⁶

(0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V _{CC}	Power Supply Voltage	4.5	5.0	5.5	Volts	6
V _{IL}	Input Logic 0 Voltage	-1.0		0.8	Volts	
V _{IH}	Input Logic 1 Voltage	2.0		V _{CC}	Volts	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%) (0°C ≤ T_A ≤ +70°C)⁶

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I _{CC1}	V _{CC} Power Supply Current (Active)			40	mA	1
I _{CC2}	V _{CC} Power Supply Current (Standby)			8	mA	7
I _I (L)	Input Leakage Current	-10		10	μA	2
I _O (L)	Output Leakage Current	-10		10	μA	3
V _{OL}	Output Logic "0" Voltage @ I _{OUT} = 3.3mA			0.4	volts	
V _{OH}	Output Logic "1" Voltage @ I _{OUT} = -220 μA	2.4			volts	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%) (0°C ≤ T_A ≤ +70°C)⁶

SYM	PARAMETER	-4		-5		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t _C	Cycle Time	375		450		ns	4
t _{CE}	$\overline{\text{CE}}$ Pulse Width	250	10000	300	10000	ns	4
t _{AC}	$\overline{\text{CE}}$ Access Time		250		300	ns	4
t _{OFF}	Output Turn Off Delay		60		75	ns	4
t _{AH}	Address Hold Time Referenced to $\overline{\text{CE}}$	60		75		ns	
t _{AS}	Address Setup Time Referenced to $\overline{\text{CE}}$	0		0		ns	
t _p	$\overline{\text{CE}}$ Precharge Time	125		150		ns	

NOTES:

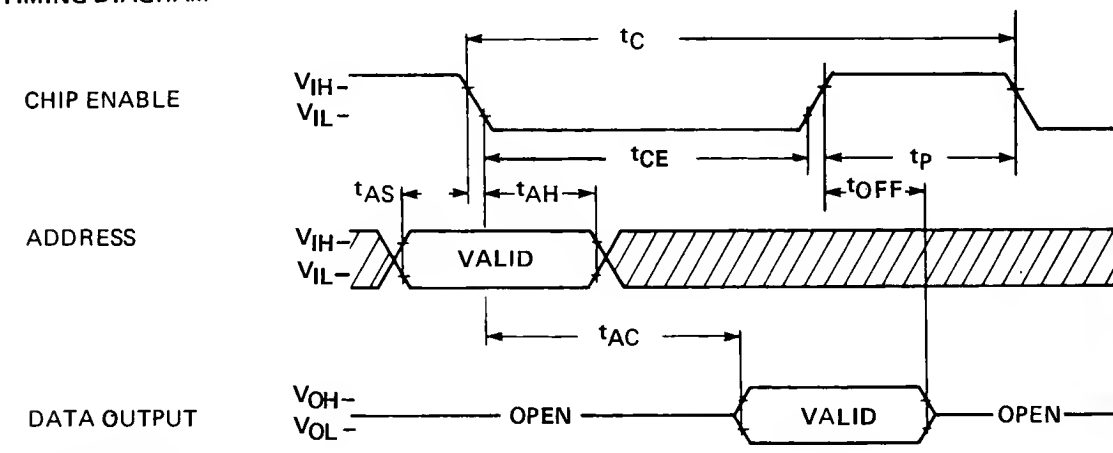
- Current is proportional to cycle rate. I_{CC1} is measured at the specified minimum cycle time. Data Outputs open.
- V_{IN} = 0V to 5.5V (V_{IL} = 5V)
- Device unselected; V_{OUT} = 0V to 5.5V
- Measured with 2 TTL loads and 100pF, transition times = 20ns
- Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:

$$C = \frac{\Delta Q}{\Delta V} \text{ with } \Delta V = 3 \text{ volts}$$
- A minimum 2msac time delay is required after the application of V_{CC} (+5) before proper device operation is achieved. $\overline{\text{CE}}$ must be at V_{IH} for this time period.
- $\overline{\text{CE}}$ high.

CAPACITANCE ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_i	Input Capacitance	5	8	pF	5
C_o	Output Capacitance	7	15	pF	5

TIMING DIAGRAM



DESCRIPTION (Continued)

ROM's and imposes no loss in system operating flexibility over an unlocked device.

Other system oriented features include fully TTL compatible inputs and outputs. The three state outputs, controlled by the \overline{CE} input, will drive a minimum of 2 standard TTL loads. The MK36000 operates from a single +5 volt power supply with a wide $\pm 10\%$ tolerance, providing the widest operating margins available. The MK36000 is packaged in the industry standard 24 pin DIP.

Any application requiring a high performance, high bit density ROM can be satisfied by the MK36000 ROM. This device is ideally suited for 8 bit micro-processor systems such as those which utilize the Z-80. It can offer significant cost advantages over PROM.

OPERATION

The MK36000 is controlled by the chip enable (\overline{CE}) input. A negative going edge at the \overline{CE} input will

activate the device as well as strobe and latch the inputs into the onchip address registers. At access time the outputs will become active and contain the data read from the selected location. The outputs will remain latched and active until \overline{CE} is returned to the inactive state.

Programming Data

MOSTEK is now able to utilize a wide spectrum of data input formats and media. Those presently available are listed in the following table:

ROMS

PRELIMINARY

MOSTEK®

64K-BIT MOS READ-ONLY MEMORY

MK37000 (P/J/N)-5

FEATURES

- Organization: 8K x 8 Bit ROM - JEDEC Pinout
- Pin compatible with Mostek's BYTEWYDE™ Memory Family
- Access Time/Cycle Time

P/N	ACCESS	CYCLE
MK37000-5	300ns	450ns

- Mask ROM replacement for MK2764 EPROM
- No Connections allow easy upgrade to future generation higher density ROMs
- Low power dissipation: 220mW max active, 45mW max standby
- \overline{CE} and \overline{OE} functions facilitate Bus control

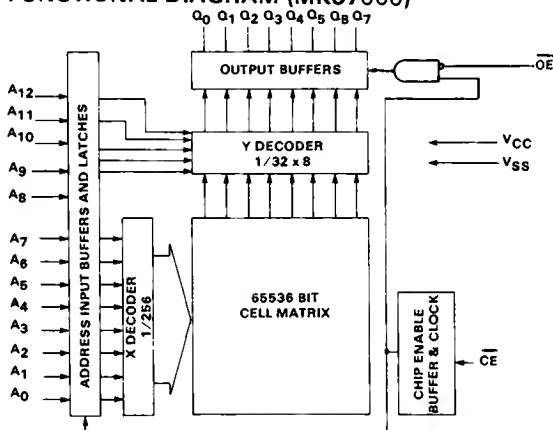
DESCRIPTION

The MK37000 is a N-channel silicon gate MOS Read Only Memory, organized as 8192 words by 8 bits. As a state-of-the-art device, the MK37000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating margins. The MK37000 is to be used as a pin/function compatible mask programmable alternative to the MK2764 8K x 8 bit EPROM. As a member of the Mostek BYTEWYDE

Memory Family, the MK37000 brings to the memory market a new era of ROM, PROM and EPROM compatibility previously unavailable.

Use of clocked control periphery and a standard static ROM cell makes the MK37000 the lowest power 64K ROM available. Active power is a mere 220mW while standby (\overline{CE} high) is only 45mW. To provide greater system flexibility an output enable (\overline{OE}) function has been added using one of the extra pins available on the

FUNCTIONAL DIAGRAM (MK37000)

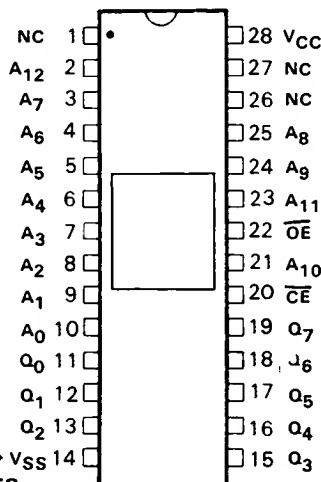


TRUTH TABLE

CE	OE	MODE	OUTPUTS	POWER
V_{IH}	X	Deselect	High-Z	Standby
V_{IL}	V_{IH}	Inhibit	High-Z	Active
V_{IL}	V_{IL}	Read	DOUT	Active

X = Don't Care

PIN CONNECTIONS



PIN NAMES

A0 - A12 - Address	NC -	No Connection
\overline{CE} - Chip Enable	\overline{OE} -	Output Enable
Q0 - Q7 - Outputs	V_{CC} -	+5V supply
	V_{SS} -	Ground

ROMS

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to V_{SS}	-1.0V to +7V
Operating Temperature T_A (Ambient)	0°C to +70°C
Storage Temperature—Ceramic (Ambient)	-65°C to +150°C
Storage Temperature—Plastic (Ambient)	-55°C to +125°C
Power Dissipation	1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS*

(0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	
V_{IL}	Input Logic 0 Voltage	-1.0		0.8	V	
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	V	

DC ELECTRICAL CHARACTERISTICS *

($V_{CC} = 5V \pm 10\%$) (0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{CC1}	V_{CC} Power Supply Current (Active)			40	mA	1
I_{CC2}	V_{CC} Power Supply Current (Standby)			8	mA	7
$I_{I(L)}$	Input Leakage Current	-10		10	μA	2
$I_{O(L)}$	Output Leakage Current	-10		10	μA	3
V_{OL}	Output Logic "0" Voltage @ $I_{OUT} = 3.3mA$			0.4	V	
V_{OH}	Output Logic "1" Voltage @ $I_{OUT} = -220\mu A$	2.4			V	

AC ELECTRICAL CHARACTERISTICS*

($V_{CC} = 5V \pm 10\%$) (0°C ≤ T_A ≤ +70°C)

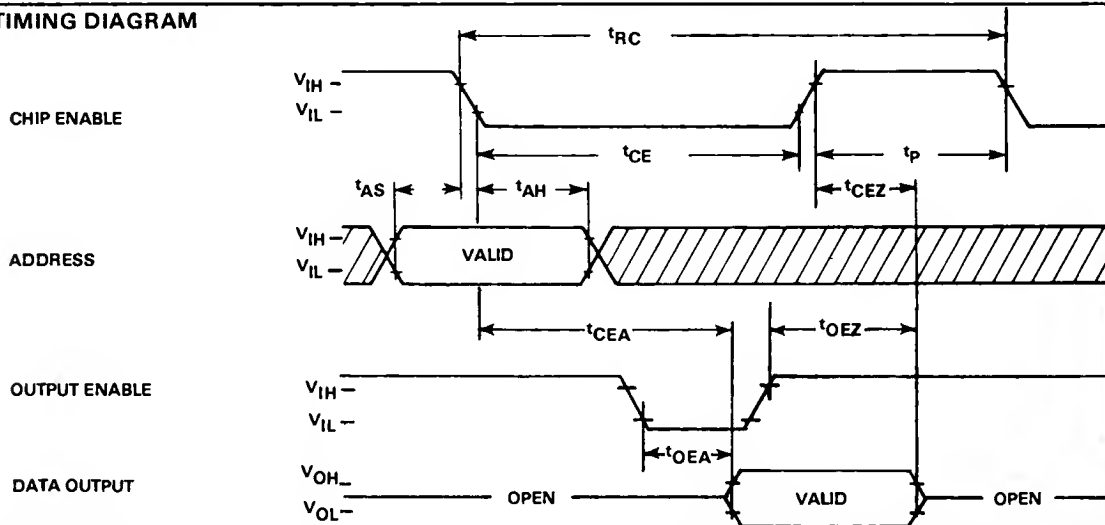
SYM	PARAMETER	-5		UNITS	NOTES
		MIN	MAX		
t_{RC}	Read Cycle Time	450		ns	4
t_{CE}	\overline{CE} Pulse Width	300	10,000	ns	4
t_{CEA}	\overline{CE} Access Time		300	ns	4
t_{CEZ}	Chip Enable Data Off Time		75	ns	
t_{AH}	Address Hold Time Referenced to \overline{CE}	75		ns	
t_{AS}	Address Setup Time Referenced to \overline{CE}	0		ns	
t_p	\overline{CE} Precharge Time	150		ns	
t_{OEA}	Output Enable Access Time		100	ns	
t_{OEZ}	Output Enable Data Off Time		75	ns	

CAPACITANCE

(0°C ≤ T_A ≤ 70°C)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C _I	Input Capacitance	5	8	pF	5
C _O	Output Capacitance	7	15	pF	5

TIMING DIAGRAM



NOTES:

1. Current is proportional to cycle rate. I_{CC1} is measured at the specified minimum cycle time. Data Outputs open.
2. V_{IN} = 0V to 5.5V
3. Device unselected; V_{OUT} = 0V to 5.5V
4. Measured with 2 TTL loads and 100pF, transition times = 20ns
5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:
C = $\frac{\Delta Q}{\Delta V}$ with $\Delta V = 3$ volts
6. A minimum 2ms time delay is required after the application of V_{CC} (+5) before proper device operation is achieved. \overline{CE} must be at V_{IH} for this time period.
7. \overline{CE} high

DESCRIPTION (Continued)

28 pin DIP. This function matches that found on all of the new BYTEWYDE family of memories available from Mostek.

The use of clocked \overline{CE} mode of operation provides an automatic power down mode of operation. The MK37000 features on chip address latches controlled by the \overline{CE} input. Once address hold time is met, new address data can be provided to the device in anticipation of a subsequent cycle. It is not necessary to maintain the address up to access time to access valid data. The output enable function controls only the outputs and is not latched by \overline{CE} . The \overline{CE} input can be used for device selection and the \overline{OE} input used to avoid bus conflicts so that outputs can be 'OR'ed together when using multiple devices.

Other system oriented features include fully TTL compatible inputs and outputs. The three state outputs, controlled by the \overline{OE} input, will drive a minimum of 2 standard TTL loads. The MK37000 operates from a single +5 volt power supply with a wide ± 10%

tolerance, providing the widest operating margins available. The MK37000 is packaged in the industry standard 28 pin DIP. Pin 1 and 26 are not connected to allow easy upward compatibility with next generation higher density ROM which will use these pins for addresses. Pin 27 is not connected in order to maintain compatibility with RAMs which use this pin as a write enable (\overline{WE}) control function.

Any application requiring a high performance, high bit density ROM can be satisfied by the MK37000. This device is ideally suited for 8 bit microprocessor systems such as those which utilize the MK3880. It can offer significant cost advantages over PROM.

OPERATION

The MK37000 is controlled by the chip enable (\overline{CE}) and output enable (\overline{OE}) inputs. A negative going edge at the \overline{CE} input will activate the device and latch the addresses into the on chip address registers. The output buffers, under the control of \overline{OE} , will become active in \overline{CE} access

time (t_{CEA}) if the output enable access time (t_{OEA}) requirement is met. The on chip address register allows addresses to be changed after the specified hold time (t_{AH}) in preparation for the next cycle. The outputs will remain valid and active until either \overline{CE} or \overline{OE} is returned to the inactive state. After chip deselect time (t_{CEZ}) the output buffers will go to a high impedance state. The \overline{CE} input must remain inactive (high) between subsequent cycles for time t_p to allow for precharging the nodes of the internal circuitry.

MK37000 ROM CODE DATA INPUT PROCEDURE

The preferred method of supplying code data to Mostek is in the form of programmed EPROMs (see table). In addition to the programmed set, Mostek requires an additional set of blank EPROMs for supplying customer code verification. When multiple EPROMs are required to describe the ROM they shall be designated in ascending address space with the numbers 1, 2, 3, etc. As an example, EPROM #1 would start with address space 0000 and go to 07FF for a 2K x 8 device. EPROM #2 would then start at address space 0800 and so on. A

total of (4) 2K x 8 devices would be required to totally describe the address space of the 8K x 8 MK37000.

A paper printout and verification approval letter will accompany each verification EPROM set returned to the customer. Approval is considered to be excepted when the signed verification letter is returned to Mostek. The original set of EPROMs will be retained by Mostek for the duration of the prototyping process.

Acceptable EPROMs for Code Data

Table 1

EPROM	# REQUIRED
2716/2516	4
2732	2
2764	1

MOSTEK®

2048 x 8-BIT EPROM

Electrically Programmable/Ultraviolet Erasable ROM

MK2716 (J)-5/6/7/8

FEATURES

- 16,384 Bit Ultraviolet Erasable, Electrically Programmable ROM, organized as 2048 words by 8 bits
- Single +5 volt power supply during READ operation
- Fast Access Time in READ mode

P/N	ACCESS TIME
MK2716-5	300ns
MK2716-6	350ns
MK2716-7	390ns
MK2716-8	450ns

- Low Power Dissipation: 525mW max active
- Power Down Mode: 132mW max standby
- Three State Output OR-tie capability

DESCRIPTION

The MK2716 is a 2048 x 8 bit electrically programmable/ultraviolet erasable Read Only Memory. The circuit is fabricated with Mostek's advanced N-channel silicon gate technology for the highest performance and reliability. The MK2716 offers significant advances over

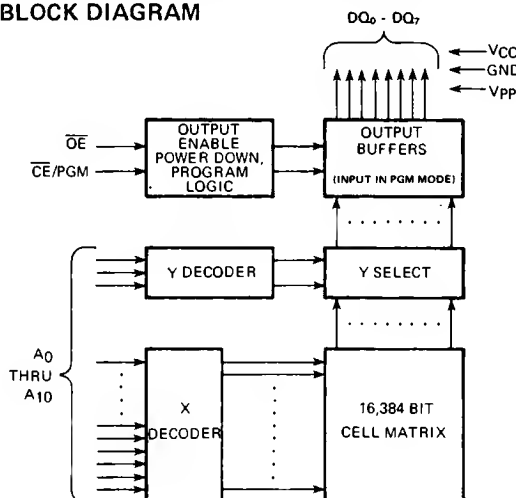
- Five modes of operation for greater system flexibility (see Table)
- Single programming requirement: single location programming with one 50msec pulse
- Pin Compatible with Mostek's BYTEWYDE™ Memory Family
- TTL compatible in all operating modes
- Standard 24 pin DIP with transparent lid

MODE SELECTION

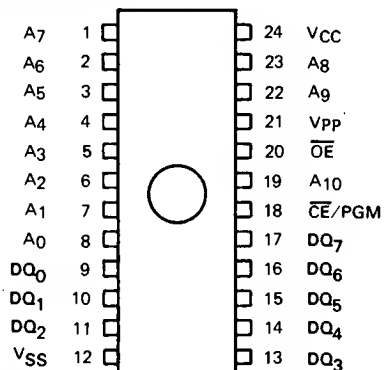
MODE PIN	\overline{CE}/PGM (18)	\overline{OE} (20)	VPP (21)	OUTPUTS
READ	V_{IL}	V_{IL}	+5	Valid Out
STANDBY	V_{IH}	Don't Care	+5	Open
PROGRAM	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	Input
PROGRAM VERIFY	V_{IL}	V_{IL}	+25	Valid Out
PROGRAM INHIBIT	V_{IL}	V_{IH}	+25	Open

$V_{CC}(24) = 5V$ all modes

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

A0-A10	Addresses	DQ0-DQ7	Data Outputs*
\overline{CE}/PGM	Chip Enable/ Program	\overline{OE}	Output Enable
		VSS	Ground

*Inputs in Program Mode

ROMS

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} (Except V_{pp})	-0.3V to +6V
Voltage on V_{pp} supply pin relative to V_{SS}	-0.3V to +28V
Operating Temperature T_A (Ambient)	$0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$
Storage Temperature (Ambient)	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$
Power Dissipation	1 Watt
Short Circuit Open Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION**RECOMMENDED DC OPERATING CONDITIONS AND CHARACTERISTICS^{1,3,7}**

($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$) ($V_{CC} = +5V \pm 5\%$, $V_{pp} = V_{CC}$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{IL}	Input Low Voltage	-0.1		0.8	V	
I_{CC1}	V_{CC} Standby Power Supply Current ($\overline{OE} = V_{IL}$; $\overline{CE} = V_{IH}$)		10	25	mA	2
I_{CC2}	V_{CC} Active Power Supply Current ($\overline{OE} = \overline{CE} = V_{IL}$)		57	100	mA	2
I_{pp1}	V_{pp} Current ($V_{pp} = 5.25V$)			6	mA	2
V_{OH}	Output High Voltage ($I_{OH} = -400\mu A$)	2.4			V	
V_{OL}	Output Low Voltage ($I_{OL} = 2.1mA$)			.45	V	
I_{IL}	Input Leakage Current ($V_{IN} = 5.25V$)			10	μA	
I_{OL}	Output Leakage Current ($V_{OUT} = 5.25V$)			10	μA	

AC CHARACTERISTICS^{1,2,4}

($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$) ($V_{CC} = +5V \pm 5\%$, $V_{pp} = V_{CC}$)

SYM	PARAMETER	-5		-6		-7		-8		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_{ACC}	Address to Output Delay ($\overline{CE} = \overline{OE} = V_{IL}$)		300		350		390		450	ns	
t_{CE}	CE to Output Delay ($\overline{OE} = V_{IL}$)		300		350		390		450	ns	5
t_{OE}	Output Enable to Output Delay ($\overline{CE} = V_{IL}$)		120		120		120		120	ns	9
t_{DF}	Chip Deselect to Output Float ($\overline{CE} = V_{IL}$)	0	100	0	100	0	100	0	100	ns	8
t_{OH}	Address to Output Hold ($\overline{CE} = \overline{OE} = V_{IL}$)	0		0		0		0		ns	

CAPACITANCE
(T_A = 25°C)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C _{IN}	Input Capacitance	4	6	pF	6
C _{OUT}	Output Capacitance	8	12	pF	6

- NOTES:
1. V_{CC} must be applied on or before V_{pp} and removed after or at the same times as V_{pp}.

2. V_{pp} and V_{CC} may be connected together (except during programming,) in which case the supply current is the sum of I_{CC} and I_{pp1}. Data Outputs open.

3. All voltages with respect to V_{SS}.

4. Load conditions = ITTL load and 100pF., tr = tf = 20ns, reference levels are 1V or 2V for inputs and .8V and 2V for outputs.

5. t_{OE} is referenced to \overline{CE} or the addresses, whichever occurs last.

6. Effective Capacitance calculated from the equation $C = \frac{\Delta Q}{\Delta V}$ where $\Delta V = 3V$

7. Typical numbers are for T_A = 25°C and V_{CC} = 5.0V ΔV

8. t_{DF} is applicable to both \overline{CE} and \overline{OE} , whichever occurs first.

9. \overline{OE} may follow up to t_{ACC} - t_{OE} after the falling edge of \overline{CE} without affecting t_{ACC}.
- TIMING DIAGRAMS
READ CYCLE ($\overline{CE} = V_{IL}$)
- Timing diagram for a Read Cycle ($\overline{CE} = V_{IL}$). The diagram shows three signals: ADDRESSES, \overline{OE} , and OUTPUT. ADDRESSES transitions from V_{IH} to V_{IL} (shaded area) and back. \overline{OE} transitions from V_{IH} to V_{IL} and back. OUTPUT is OPEN until t_{ACC} after the falling edge of \overline{OE} , then becomes VALID for t_{OH} . t_{DF} is the delay from the falling edge of \overline{OE} to the start of VALID output. A ROMS block is shown on the right.
- STANDBY POWER
DOWN MODE
($\overline{OE} = V_{IL}$)
- Timing diagram for Standby Power Down Mode ($\overline{OE} = V_{IL}$). The diagram shows three signals: ADDRESS, \overline{CE} , and OUTPUT. ADDRESS is VALID. \overline{CE} transitions from V_{IH} to V_{IL} (labeled STANDBY) and back (labeled ACTIVE). OUTPUT is VALID FOR CURRENT ADDRESS until t_{DF} after the falling edge of \overline{CE} , then becomes OPEN. t_{CE} is the delay from the falling edge of \overline{CE} to the start of VALID output. A ROMS block is shown on the right.
- IV-17

PROGRAM OPERATION⁸

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS^{1,2}

($T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$) ($V_{CC} = 5\text{V} \pm 5\%$, $V_{PP} = 25\text{V} \pm 1\text{V}$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{IL}	Input Leakage Current		10	μA	3
V_{IL}	Input Low Level	-0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC}+1$	V	
I_{CC}	V_{CC} Power Supply Current		100	mA	
I_{PP1}	V_{PP} Supply Current		6	mA	4
I_{PP2}	V_{PP} Supply Current during Programming Pulse		30	mA	5

AC CHARACTERISTICS AND OPERATING CONDITIONS^{1,2,6,7}

($T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$) ($V_{CC} = 5\text{V} \pm 5\%$), $V_{PP} = 25\text{V} \pm 1\text{V}$)

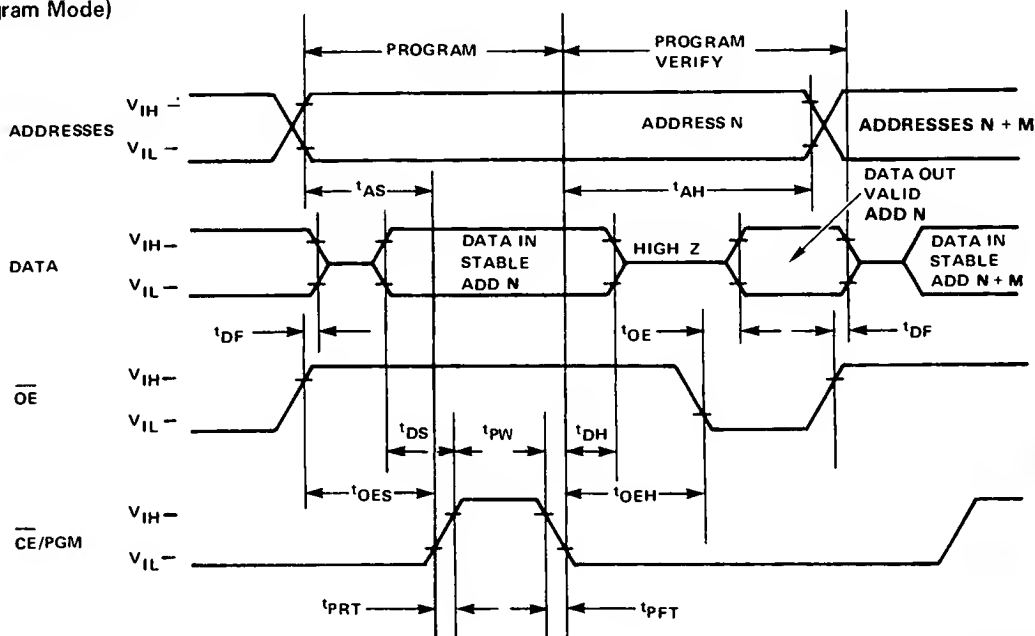
SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{AS}	Address Setup Time	2			μs	
t_{OES}	\overline{OE} Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	2			μs	
t_{OEH}	\overline{OE} Hold Time	2			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DF}	Output Enable to Output Float	0		120	ns	4
t_{OE}	Output Enable to Output Delay			120	ns	4
t_{PW}	Program Pulse Width	45	50	55	ms	
t_{PRT}	Program Pulse Rise Time	5			ns	
t_{PFT}	Program Pulse Fall Time	5			ns	

NOTES:

- V_{CC} must be applied at the same time or before V_{PP} and removed after or at the same time as V_{PP} . To prevent damage to the device it must not be inserted into a board with V_{PP} at 25V.
- Care must be taken to prevent overshoot of the V_{PP} supply when switching to +25V.
- $0.45\text{V} \leq V_{IN} \leq 5.25\text{V}$
- $\overline{CE}/\text{PGM} = V_{IL}$
- $\overline{CE}/\text{PGM} = V_{IH}$
- $t_T \approx 20\text{nsec}$
- 1V or 2V for inputs and .8V or 2V for outputs are used as timing reference levels.
- Although speed selections are made for READ operation all programming specifications are the same for all dash numbers.

TIMING DIAGRAM

(Program Mode)



DESCRIPTION CONTINUED

hardwired logic-in cost, system flexibility, turnaround time and performance.

The MK2716 has many useful system oriented features including a STANDBY mode of operation which lowers the device power from 525mW maximum active power to 132mW maximum for an overall savings of 75%.

Programming can be done with a single TTL level pulse, and may be done on any individual location either sequentially or at random. The three-state output controlled by the \overline{OE} input allows OR-tie capability for construction of large arrays. A single power supply requirement of +5 volts makes the MK2716 ideally suited for use with Mostek's new 5 volt only microprocessors such as the MK3880 (Z80). The MK2716 is packaged in the industry standard 24-pin dual-in line package with a transparent hermetically sealed lid. This allows the user to expose the chip to ultraviolet light to erase the data pattern. A new pattern may then be written into the device by following the program procedures outlined in this data sheet.

The MK2716 is specifically designed to fit those applications where fast turnaround time and pattern experimentation are required. Since data may be altered in the device (erase and reprogram) it allows for early debugging of the system program. Since single location programming is available the MK2716 can

have its data content increased (assuming all 2048 bytes were not programmed) at any time for easy updating of system capabilities in the field. Once the data/program is fixed and the intention is to produce large numbers of systems, Mostek also supplies a pin compatible mask programmable ROM, the MK34000. To transfer the program data to ROM, the user need only send the PROM along with device information to Mostek, from which the ROM with the desired pattern can be generated. This means a reduction in the possibility of error when converting data to other forms (cards, tape, etc.) for this purpose. However, data may still be input by any of these traditional means such as paper tape, card deck, etc.

READ OPERATION

The MK2716 has five basic modes of operation. Under normal operating conditions (non-programming) there are two modes including READ and STANDBY. A READ operation is accomplished by maintaining pin 18 (\overline{CE}) at V_{IL} and pin 21 (V_{PP}) at +5 volts. If \overline{OE} (pin 20) is held active low after addressing ($A_0 - A_{10}$) have stabilized then valid output data will appear on the output pins at access time t_{ACC} (address access). In this mode, access time may be referenced to \overline{OE} (t_{OE}) depending on when \overline{OE} occurs (see timing diagrams).

POWER DOWN operation is accomplished by taking pin 18(\overline{CE}) to a TTL high level (V_{IH}). The power is reduced by 75% from 525mW maximum to 132mW. In power down V_{pp} must be at +5 volts and the outputs will be open-circuit regardless of the condition of \overline{OE} . Access time from a high to low transition of \overline{CE} (t_{CE}) is the same as from addresses (t_{ACC}). (See STANDBY Timing Diagram).

PROGRAMMING INSTRUCTIONS

The MK2716 as shipped from Mostek will be completely erased. In this initial state and after any subsequent erasure, all bits will be at a '1' level (output high). Information is introduced by selectively programming '0's into the proper bit locations. Once a '0' has been programmed into the chip it may be changed only by erasing the entire chip with UV light.

Word address selection is done by the same decode circuitry used in the READ mode. The MK2716 is put into the PROGRAM mode by maintaining V_{pp} at +25V, and \overline{OE} at V_{IH} . In this mode the output pins serve as inputs (8 bits in parallel) for the required program data. Logic levels for other inputs and the V_{CC} supply voltage are the same as in the READ mode.

To program a "byte" (8 bits) of data, a TTL active high level pulse is applied to the \overline{CE} /PGM pin once addresses and data are stabilized on the inputs. Each location must have a pulse applied with only one pulse per location required. Any individual location, a sequence of locations or locations at random may be programmed in this manner. The program pulse has a minimum width of 45msec and a maximum of 55msec, and must not be programmed with a high level D.C. signal applied to the \overline{CE} /PGM pin.

PROGRAM INHIBIT is another useful mode of operation when programming multiple parallel addressed MK2716's with different data. It is necessary only to maintain \overline{OE} at V_{IH} , V_{pp} at +25, allow addresses and data to stabilize and pulse the \overline{CE} /PGM pin of the device to be programmed. Data may then be changed and the next device pulsed. The devices with \overline{CE} /PGM at V_{IL} will not be programmed.

PROGRAM VERIFY allows the MK2716 program data to be verified without having to reduce V_{pp} from +25V to +5V. V_{pp} should only be used in the PROGRAM/PROGRAM INHIBIT and PROGRAM VERIFY Modes and must be at +5V in all other modes.

MK2716 ERASING PROCEDURE

The MK2716 may be erased by exposure to high intensity ultraviolet light, illuminating the chip thru the transparent window. This exposure to ultraviolet light induces the flow of a photo current from the floating gate thereby discharging the gate to its initial state. An ultraviolet source of 2537Å yielding a total integrated dosage of 15 Watt-seconds/cm² is required. Note that all bits of the MK2716 will be erased. The erasure time is approximately 15 to 20 minutes utilizing a ultra-violet lamp with a 12000μW/cm² power rating. The lamp should be used without short wave filters, and the MK2716 to be erased should be placed about one inch away from the lamp tubes. It should be noted that as the distance between the lamp and the chip is doubled, the exposure time required goes up by a factor of 4. The UV content of sunlight is insufficient to provide a practical means of erasing the MK2716. However, it is not recommended that the MK2716 be operated or stored in direct sunlight, as the UV content of sunlight may cause erasure of some bits in a short period of time.

2048 x 8-BIT EPROM

Electrically Programmable/Ultraviolet Erasable ROM

MK2716(J)-12

FEATURES

- 16,384 Bit Ultraviolet Erasable Electrically Programmable ROM organized as 2,048 words by 8 bits
- Single +5 volt supply during READ operation
- Access Time in READ mode
- Low Power Dissipation: 525mW max active
- Power Down mode: 132mW max standby

P/N	ACCESS TIME
MK2716-12	650ns

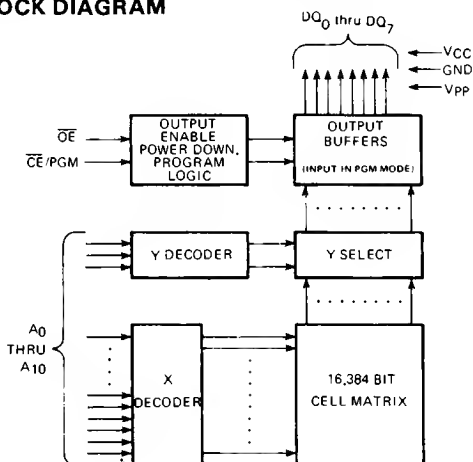
- Three State Output OR-tie capability
- Five modes of operation for greater system flexibility (see Table)
- Single programming requirement: single location programming with one 50msec pulse
- Pin Compatible with Mostek's BYTEWYDE™ memory family
- TTL compatible in all operating modes
- Standard 24 pin DIP with transparent lid

DESCRIPTION

The MK2716 is a 2048 x 8 bit electrically programmable/ultraviolet erasable Read Only Memory. The circuit is fabricated with Mostek's advanced N-Channel silicon gate technology for the highest performance and reliability. The MK2716 offers significant advances over hardwired logic in cost, system flexibility, turnaround time and performance.

The MK2716 has many useful system oriented features including a STANDBY mode of operation which lowers the device power from 525mW maximum active power to 132mW maximum for an overall savings of 75%.

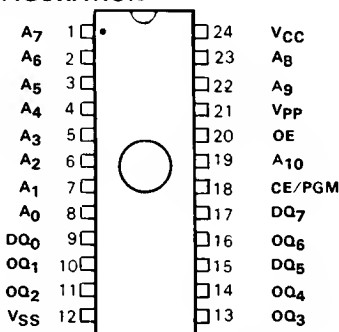
BLOCK DIAGRAM



MODE SELECTION

MODE PIN	CE/PGM (18)	OE (20)	VPP (21)	OUTPUTS
READ	V _{IL}	V _{IL}	+5	Valid Out
STANDBY	V _{IH}	Don't Care	+5	Open
PROGRAM	Pulsed V _{IL} to V _{IH}	V _{IH}	+25	Input
PROGRAM VERIFY	V _{IL}	V _{IL}	+25	Valid Out
PROGRAM INHIBIT	V _{IL}	V _{IH}	+25	Open
V _{CC} (24) = 5V all modes				

PIN CONFIGURATION



PIN NAMES

A ₀ -A ₁₀	Addresses	DQ ₀ -OQ ₇	Outputs*
CE/PGM	Chip Enable/Program	V _{SS}	Ground
OE	Output Enable		
*Inputs in Program Mode			

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} (Except V_{PP})	-0.3V to +6V
Voltage on V_{PP} supply pin relative to V_{SS}	-0.3V to +28V
Operating Temperature T_A (Ambient)	$0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$
Storage Temperature (Ambient)	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$
Power Dissipation	1 Watt
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

RECOMMENDED D.C. OPERATING CONDITIONS AND CHARACTERISTICS ^{1,3,7}

($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$) ($V_{CC} = +5\text{V} \pm 5\%$, $V_{PP} = V_{CC}$)³

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	Volts	
V_{IL}	Input Low Voltage	-0.1		0.8	Volts	
I_{CC1}	V_{CC} Standby Power Supply Current ($\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$)		10	25	mA	2
I_{CC2}	V_{CC} Active Power Supply Current ($\overline{OE} = \overline{CE} = V_{IL}$)		57	100	mA	2
I_{PP1}	V_{PP} Current ($V_{PP} = 5.25\text{V}$)			6	mA	2
V_{OH}	Output High Voltage ($I_{OH} = -400\text{ }\mu\text{A}$)	2.4			Volts	
V_{OL}	Output Low Voltage ($I_{OL} = 2.1\text{mA}$)			.45	Volts	
I_{IL}	Input Leakage Current ($V_{IN} = 5.25\text{V}$)	-10		10	μA	
I_{OL}	Output Leakage Current ($V_{OUT} = 5.25\text{V}$)	-10		10	μA	

A.C. CHARACTERISTICS ^{1,2,4}

($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$) ($V_{CC} = +5\text{V} \pm 5\%$, $V_{PP} = V_{CC}$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{ACC}	Address to Output Delay ($\overline{CE} = \overline{OE} = V_{IL}$)		650	ns	
t_{CE}	\overline{CE} to Output Delay ($\overline{OE} = V_{IL}$)		650	ns	5
t_{OE}	Output Enable to Output Delay ($\overline{CE} = V_{IL}$)		230	ns	9
t_{DF}	Chip Deselect to Output Float ($\overline{CE} = V_{IL}$)	0	150	ns	8
t_{OH}	Address to Output Hold ($\overline{CE} = \overline{OE} = V_{IL}$)	0		ns	

NOTE: All timing diagrams and operating modes (including program timing) are the same as on the standard -5, -6, -7 and -8 data sheet. This spec is to be used in conjunction with the standard data sheet.

CAPACITANCE

($T_A = 25^\circ\text{C}$)⁷

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_{IN}	Input Capacitance	4	6	pF	6
C_{OUT}	Output Capacitance	8	12	pF	6

NOTES:

- V_{CC} must be applied on or before V_{pp} and removed after or at the same times as V_{pp} .
- V_{pp} and V_{CC} may be connected together (except during programming) in which case the supply current is the sum of I_{CC} and I_{pp1} . Data outputs open.
- All voltages with respect to V_{SS} .
- Load conditions - ITTL load and 100pF, $t_r = t_f = 20\text{ns}$, reference levels are 1V or 2V for inputs and 8V and 2V for outputs
- t_{OE} is referenced to \overline{CE} or the addresses, whichever occurs last.
- Effective Capacitance calculated from the equation $C = \frac{\Delta Q}{\Delta V}$ where $\Delta V = 3V$
- Typical numbers are for $T_A = 25^\circ\text{C}$ and $V_{CC} = 5.0V$
- t_{DF} is applicable to both \overline{CE} and \overline{OE} , whichever occurs first.
- \overline{OE} may follow up to $t_{ACC} - t_{OE}$ after the falling edge of \overline{CE} without effecting t_{ACC}

DESCRIPTION CONTINUED

Programming can be done with a single TTL level pulse, and may be done on any individual location either sequentially or at random. The three-state output controlled by the \overline{OE} input allows OR-tie capability for construction of large arrays. A single power supply requirement of +5 volts makes the MK2716 ideally suited for use with Mostek's new 5 volt only microprocessors such as the MK3880 (Z80). The MK2716 is packaged in the industry standard 24-pin dual-in line package with a transparent hermetically sealed lid. This allows the user to expose the chip to ultraviolet light to erase the data pattern. A new pattern may then be written into the device by following the program procedures outlined in this data sheet.

The MK2716 is specifically designed to fit those applications where fast turnaround time and pattern experimentation are required. Since data may be altered in the device (erase and reprogram) it allows for early debugging of the system program. Since single location programming is available the MK2716 can have its data content increased (assuming all 2048 bytes were not programmed) at any time for easy updating of system capabilities in the field. Once the data/program is fixed and the intention is to produce large numbers of systems, Mostek also supplies a pin compatible mask programmable ROM, the MK34000. To transfer the program data to ROM, the user need only send the PROM along with device information to Mostek, from which the ROM with the desired pattern can be generated. This means a reduction in the possibility of error when converting data to other forms (cards, tape, etc.) for this purpose. However, data may still be input by any of these traditional means such as paper tape, card, deck, etc.

READ OPERATION

The MK2716 has five basic modes of operation. Under normal operating conditions (non-programming) there are two modes including READ and STANDBY. A READ operation is accomplished by maintaining pin 18 (\overline{CE}) at V_{IL} and pin 21 (V_{pp}) at +5 volts. If \overline{OE} (pin 20) is held active low after addressing (A0 - A10) have stabilized then valid output data will appear on the output pins at access time t_{ACC} (address access). In this mode, access time may be referenced to \overline{OE} (t_{OE}) depending on when \overline{OE} occurs (see timing diagrams).

POWER DOWN operation is accomplished by taking pin 18 (\overline{CE}) to a TTL high level (V_{IH}). The power is reduced by 75% from 525mW maximum to 132mW. In power down V_{pp} must be at +5 volts and the outputs will be open-circuit regardless of the condition of \overline{OE} . Access time from a high to low transition of \overline{CE} (t_{CE}) is the same as from addresses (t_{ACC}). (See STANDBY Timing Diagram).

PROGRAMMING INSTRUCTIONS

The MK2716 as shipped from Mostek will be completely erased. In this initial state and after any subsequent erasure, all bits will be at a '1' level (output high). Information is introduced by selectively programming '0's into the proper bit locations. Once a '0' has been programmed into the chip it may be changed only by erasing the entire chip with UV light.

Word address selection is done by the same decode circuitry used in the READ mode. The MK2716 is put into the PROGRAM mode by maintaining V_{pp} at +25V, and \overline{OE} at V_{IH} . In this mode the output pins serve as inputs (8 bits in parallel) for the required program data.

Logic levels for other inputs and the V_{CC} supply voltage are the same as in the READ mode.

To program a "byte" (8 bits) of data, a TTL active high level pulse is applied to the \overline{CE}/PGM pin once addresses and data are stabilized on the inputs. Each location must have a pulse applied with only one pulse per location required. Any individual location, a sequence of locations or locations at random may be programmed in this manner. The program pulse has a minimum width of 45 msec and a maximum of 55msec, and must not be programmed with a high level DC signal applied to the \overline{CE}/PGM pin.

PROGRAM INHIBIT is another useful mode of operation when programming multiple parallel addressed MK2716's with different data. It is necessary only to maintain \overline{OE} at V_{IH} , V_{PP} at +25, allow addresses and data to stabilize and pulse the \overline{CE}/PGM pin of the device to be programmed. Data may then be changed and the next device pulsed. The devices with \overline{CE}/PGM at V_{IL} will not be programmed.

PROGRAM VERIFY allows the MK2716 program data to be verified without having to reduce V_{PP} from +25V to +5V. V_{PP} should only be used in the PROGRAM/

PROGRAM INHIBIT and PROGRAM VERIFY modes and must be at +5V in all other modes.

MK2716 ERASING PROCEDURE

The MK2716 may be erased by exposure to high intensity ultraviolet light, illuminating the chip thru the transparent window. This exposure to ultraviolet light induces the flow of a photo current from the floating gate thereby discharging the gate to its initial state. An ultraviolet source of 2537Å yielding a total integrated dosage of 15 Watt-seconds/cm² is required. Note that all bits of the MK2716 will be erased. The erasure time is approximately 15 to 20 minutes utilizing an ultraviolet lamp with a 12000 $\mu W/cm^2$ power rating. The lamp should be used without shortwave filters, and the MK2716 to be erased should be placed about one inch away from the lamp tubes. It should be noted that as the distance between the lamp and the chip is doubled, the exposure time required goes up by a factor of 4. The UV content of sunlight is insufficient to provide a practical means of erasing the MK2716. However, it is not recommended that the MK2716 be operated or stored in direct sunlight, as the UV content of sunlight may cause erasure of some bits in a short period of time.

FEATURES

- MK2764 - Organized 8K x 8 bit EPROM
- Single +5 volt power supply during READ operation
- Single location programming capability
- Fast access time in READ mode

P/N	ACCESS TIME
MK2764-8	450ns

- Output Enable (\overline{OE}) function for greater system flexibility

DESCRIPTION

The MK2764 is an 8192 x 8 bit electrically programmable/ultraviolet erasable Read Only Memory. The circuit is fabricated with Mostek's advanced N-channel silicon gate technology for the highest performance and reliability. The MK2764 offers significant advances over hardwired logic in cost, system flexibility, turnaround time and performance.

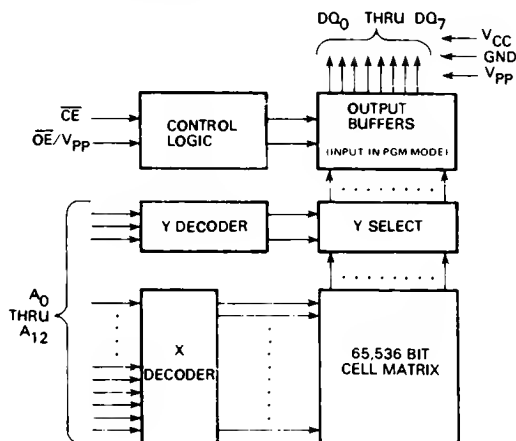
The MK2764 has many useful system oriented features including a STANDBY mode of operation which lowers the device power from 525mW maximum active power to 132mW maximum for an overall savings of 75%.

- Power Down mode: 132mW max standby
- Low power dissipation: 525mW active max
- Pin compatible with Mostek's BYTEWYDE™ Memory Family
- Pin compatible mask programmable ROM available: MK37000
- TTL compatible in all operating modes (except V_{pp} in Program Mode and Program Inhibit)
- Standard 28 pin DIP with transparent lid
- Five basic modes of operation (see Table)

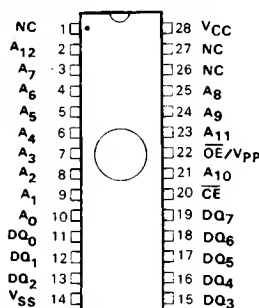
MODE SELECTION

MODE PIN	\overline{CE} (20)	\overline{OE}/V_{pp} (22)	OUTPUTS
READ	V_{IL}	V_{IL}	Valid
STANDBY	V_{IH}	Don't Care	Open
PROGRAM	Pulsed V_{IH} to V_{IL}	+25	Inputs
DESELECT	V_{IL}	V_{IH}	Open
PROGRAM INHIBIT	V_{IH}	+25	Open
V_{CC} (28) = 5V all modes			

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

A_0 - A_{12}	Addresses	\overline{OE}/V_{pp}	Output Enable
\overline{CE}	Chip Enable	NC	Program
DQ_0 - DQ_7	Data Outputs*		No Connect
V_{SS}	Ground		

*Inputs in program mode

ROMS

1980 MEMORY DATA BOOK

I	Table of Contents	TABLE OF CONTENTS
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MOSTEK®

4096x1-BIT DYNAMIC RAM

MK4027(J/N)-2/3

FEATURES

- Industry standard 16-pin DIP (MK 4096) configuration
- 120ns access time, 320ns cycle (MK4027-1)
150ns access time, 320ns cycle (MK4027-2)
200ns access time, 375ns cycle (MK4027-3)
- $\pm 10\%$ tolerance on all supplies (+12V, $\pm 5V$)
- ECL compatible on V_{BB} power supply ($-5.7V$)
- Low Power: 462mW active (max)
27mW standby (max)
- Improved performance with "gated \overline{CAS} ", " \overline{RAS} only" refresh and page mode capability
- All inputs are low capacitance and TTL compatible
- Input latches for addresses, chip select and data in
- Three-state TTL compatible output
- Output data latched and valid into next cycle

DESCRIPTION

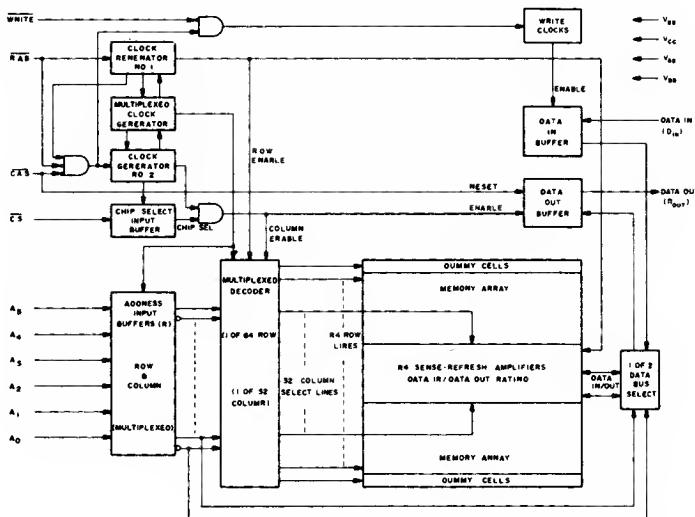
The MK 4027 is a 4096 word by 1 bit MOS random access memory circuit fabricated with MOSTEK's N-channel silicon gate process. This process allows the MK 4027 to be a high performance state-of-the-art memory circuit that is manufacturable in high volume. The MK 4027 employs a single transistor storage cell utilizing a dynamic storage technique and dynamic control circuitry to achieve optimum performance with low power dissipation.

A unique multiplexing and latching technique for the address inputs permits the MK 4027 to be packaged in a standard 16-pin DIP on 0.3 in. centers. This package size provides high system-bit densities and is compatible with widely available automated testing and insertion equipment.

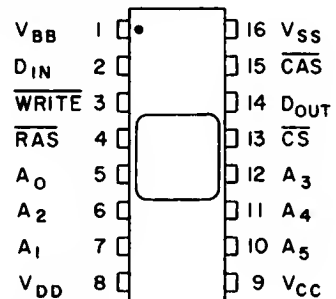
System oriented features include direct interfacing capability with TTL, only 6 very low capacitance address lines to drive, on-chip address and data registers which eliminates the need for interface registers, input logic levels selected to optimize noise immunity, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MK 4027 also incorporates several flexible operating modes. In addition to the usual read and write cycles, read-modify write, page-mode, and RAS-only refresh cycles are available with the MK 4027. Page-mode timing is very useful in systems requiring Direct Memory Access (DMA) operation.

DYNAMIC
RAMS

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A ₀ -A ₅	ADDRESS INPUTS
CAS	COLUMN ADDRESS STROBE
CS	CHIP SELECT
DIN	DATA IN
DOUT	DATA OUT
RAS	ROW ADDRESS STROBE
WRITE	READ/WRITE INPUT
VBB	POWER (-5V)
VCC	POWER (+5V)
VDD	POWER (+12V)
VSS	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V _{BB}	−0.5V to +20V
Voltage on V _{DD} , V _{CC} relative to V _{SS}	−1.0V to +15V
V _{BB} −V _{SS} (V _{DD} −V _{SS} > 0)	0V
Operating temperature, T _A (Ambient)	0°C to + 70°C
Storage temperature (Ambient)(Ceramic)	−65°C to + 150°C
Storage temperature (Ambient)(Plastic)	−55°C to + 125°C
Short circuit output current	50mA
Power dissipation	1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS ⁴

(0°C ≤ T_A ≤ 70°C) ¹

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V _{DD}	Supply Voltage	10.8	12.0	13.2	volts	2
V _{CC}	Supply Voltage	4.5V	5.0	5.5	volts	2,3
V _{SS}	Supply Voltage	0	0	0	volts	2
V _{BB}	Supply Voltage	−4.5	−5.0	−5.7	volts	2
V _{IHC}	Logic 1 Voltage, RAS, CAS, WRITE	2.4		7.0	volts	2
V _{IH}	Logic 1 Voltage, all inputs except RAS, CAS, WRITE	2.2		7.0	volts	2
V _{IL}	Logic 0 Voltage, all inputs	−1.0		.8	volts	2

DC ELECTRICAL CHARACTERISTICS ⁴

(0°C ≤ T_A ≤ 70°C) ¹ (V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ± 10%; V_{SS} = 0V; −5.7V ≤ V_{BB} ≤ −4.5V)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I _{DD1}	Average V _{DD} Power Supply Current			35	mA	5
I _{DD2}	Standby V _{DD} Power Supply Current			2	mA	8
I _{DD3}	Average V _{DD} Power Supply Current during "RAS only" cycles			25	mA	
I _{CC}	V _{CC} Power Supply Current				mA	6
I _{BB}	Average V _{BB} Power Supply Current			150	μA	
I _{I(L)}	Input Leakage Current (any input)			10	μA	7
I _{O(L)}	Output Leakage Current			10	μA	8,9
V _{OH}	Output Logic 1 Voltage @ I _{OUT} = −5mA	2.4			volts	
V _{OL}	Output Logic 0 Voltage @ I _{OUT} = 3.2mA			0.4	volts	

NOTES

- T_A is specified for operation at frequencies to t_{RC} ≥ t_{RC} (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible provided that all AC parameters are met. See figure 2 for derating curve.
- All voltages referenced to V_{SS}.
- Output voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
- Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
- Current is proportional to cycle rate, I_{DD1} (max) is measured at the cycle rate specified by t_{RC} (min). See figure 1 for I_{DD1} limits at other cycle rates.
- I_{CC} depends on output loading. During readout of high level data V_{CC} is connected through a low impedance (135μ typ) to Data Out. At all other times I_{CC} consists of leakage currents only.
- All device pins at 0 volts except V_{BB} which is at −5 volts and the pin under test which is at +10 volts.
- Output is disabled (high-impedance) and RAS and CAS are both at a logic 1. Transient stabilization is required prior to measurement of this parameter.
- 0V ≤ V_{OUT} ≤ +10V.
- Effective capacitance is calculated from the equation:

$$C = \frac{\Delta Q}{\Delta V}$$
with ΔV = 3 volts.
- A.C. measurements assume t_T = 5ns.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS(4, 11, 17)
 $(0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C})^1$ ($V_{DD} = 12.0\text{V} \pm 10\%$, $V_{CC} = 5.0\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, $-5.7\text{V} \leq V_{BB} \leq -4.5\text{V}$)

	PARAMETER	MK4027-2		MK4027-3		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t _{RC}	Random read or write cycle time	320		375		ns	12
t _{RWC}	Read write cycle time	320		375		ns	12
t _{RMW}	Read modify write cycle time	320		405		ns	12
t _{PC}	Page mode cycle time	170		225		ns	12
t _{RAC}	Access time from row address strobe		150		200	ns	13, 15
t _{CAC}	Access time from column address strobe		100		135	ns	14, 15
t _{OFF}	Output buffer turn-off delay		40		50	ns	
t _{RP}	Row address strobe precharge time	100		120		ns	
t _{RAS}	Row address strobe pulse width	150	10,000	200	10,000	ns	
t _{RSH}	Row address strobe hold time	100		135		ns	
t _{CAS}	Column address strobe pulse width	100		135		ns	
t _{CSH}	Column address strobe hold time	150		200		ns	
t _{RCD}	Row to column strobe delay	20	50	25	65	ns	16
t _{ASR}	Row address set-up time	0		0		ns	
t _{RAH}	Row address hold time	20		25		ns	
t _{ASC}	Column address set-up time	-10		-10		ns	
t _{CAH}	Column address hold time	45		55		ns	
t _{AR}	Column address hold time referenced to RAS	95		120		ns	
t _{CSC}	Chip select set-up time	-10		-10		ns	
t _{CH}	Chip select hold time	45		55		ns	
t _{CHR}	Chip select hold time referenced to RAS	95		120		ns	
t _T	Transition time (rise and fall)	3	35	3	50	ns	17
t _{RCS}	Read command set-up time	0		0		ns	
t _{RCH}	Read command hold time	0		0		ns	
t _{WCH}	Write command hold time	45		55		ns	
t _{WCR}	Write command hold time referenced to RAS	95		120		ns	
t _{WP}	Write command pulse width	45		55		ns	
t _{RWL}	Write command to row strobe lead time	50		70		ns	
t _{CWL}	Write command to column strobe lead time	50		70		ns	
t _{DS}	Data in set-up time	0		0		ns	18
t _{DH}	Data in hold time	45		55		ns	18
t _{DHR}	Data in hold time referenced to RAS	95		120		ns	
t _{CRP}	Column to row strobe precharge time	0		0		ns	
t _{CP}	Column precharge time	60		80		ns	
t _{RFSH}	Refresh period		2		2	ms	
t _{WCS}	Write command set-up time	0		0		ns	19
t _{CWD}	CAS to WRITE delay	60		80		ns	19
t _{RWD}	RAS to WRITE delay	110		145		ns	19
t _{DOH}	Data out hold time	10		10		μs	

Notes Continued

12. The specifications for t_{PC} (min) and t_{QWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$) is assured. See figure 2 for derating curve.
13. Assumes that t_{RCO} ≤ t_{RCD} (max).
14. Assumes that t_{RCO} ≥ t_{RCD} (max).
15. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
16. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

17. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
18. These parameters are referenced to CAS leading edge in random write cycles and to WRITE leading edge in delayed write or read-modify-write cycles.
19. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in a read/write or read/modify/write cycle only. If t_{WCS} ≥ t_{WCS} (min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If t_{CWD} ≥ t_{CWD} (min) and t_{RWD} ≥ t_{RWD} (min), the cycle is a read-write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.

DYNAMIC RAMS

AC ELECTRICAL CHARACTERISTICS

(0°C ≤T_A ≤70°C) (V_{DD} = 12.0V ± 10%; V_{SS} = 0V; -5.7V ≤V_{BB} ≤-4.5V)

	PARAMETER	TYP	MAX	UNITS	NOTES
C 11	Input Capacitance (A ₀ -A ₅), D _{1IN} , \overline{CS}	4	5	pF	10
C 12	Input Capacitance \overline{RAS} , \overline{CAS} , \overline{WRITE}	8	10	pF	10
C ₀	Output Capacitance (D _{OUT})	5	7	pF	8,10

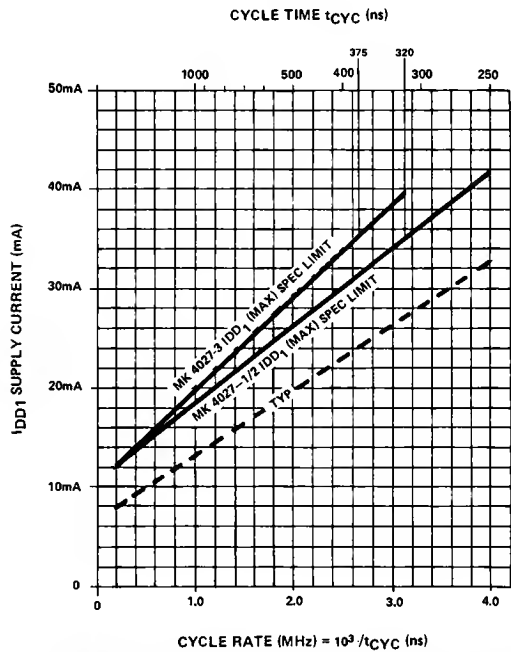


Figure 1. Maximum I_{DD1} versus cycle rate for device operation at extended frequencies.

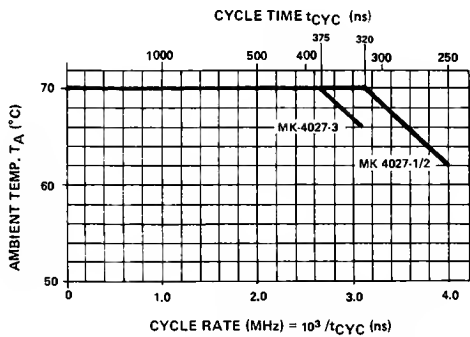
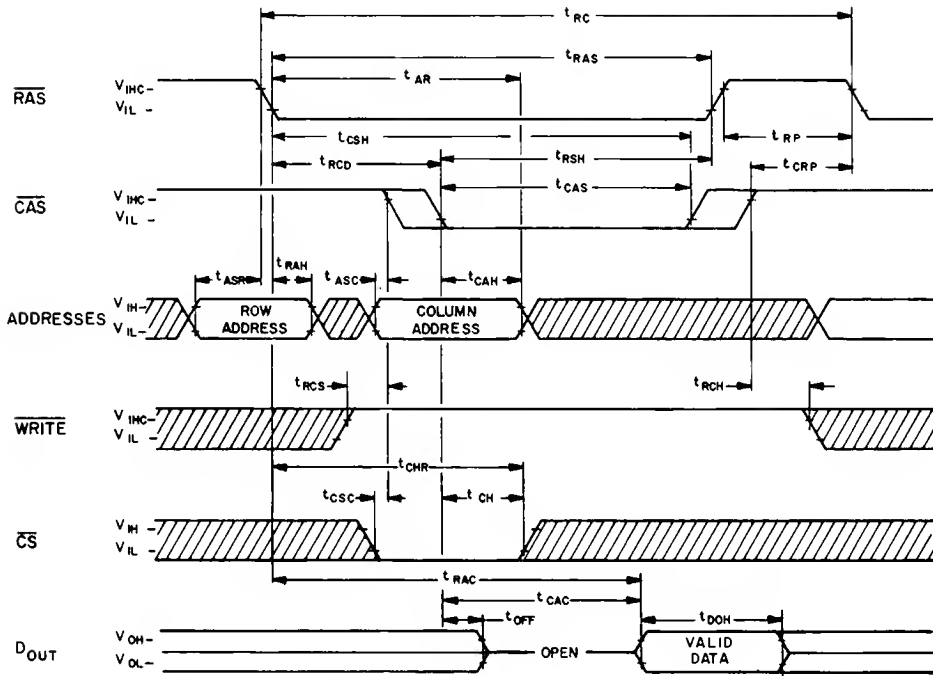
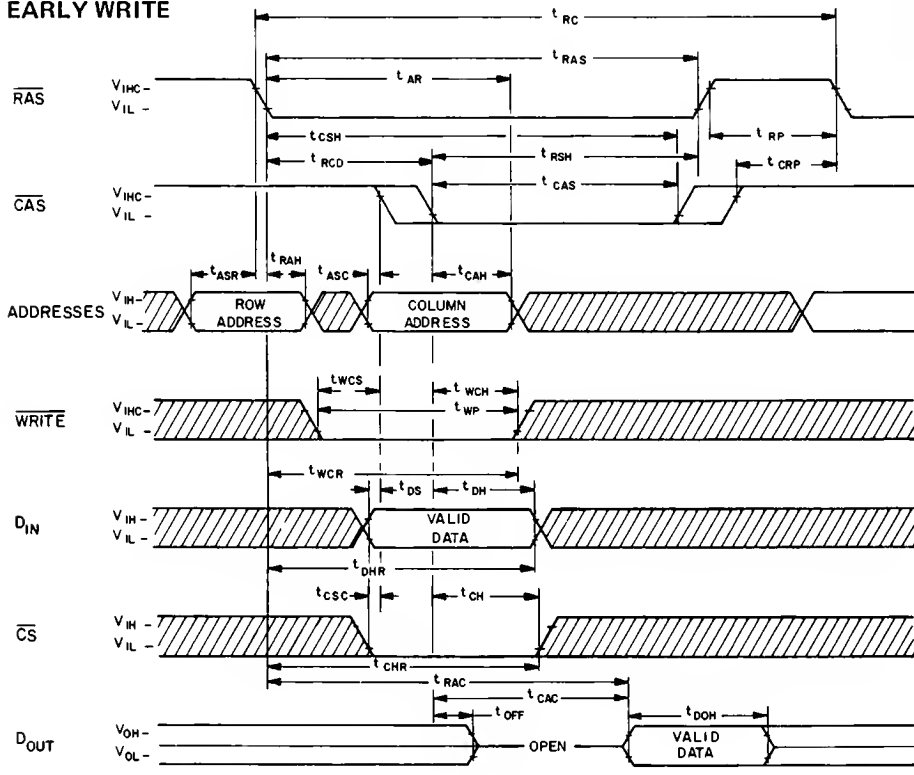


Figure 2. Maximum ambient temperature versus cycle rate for extended frequency operation.

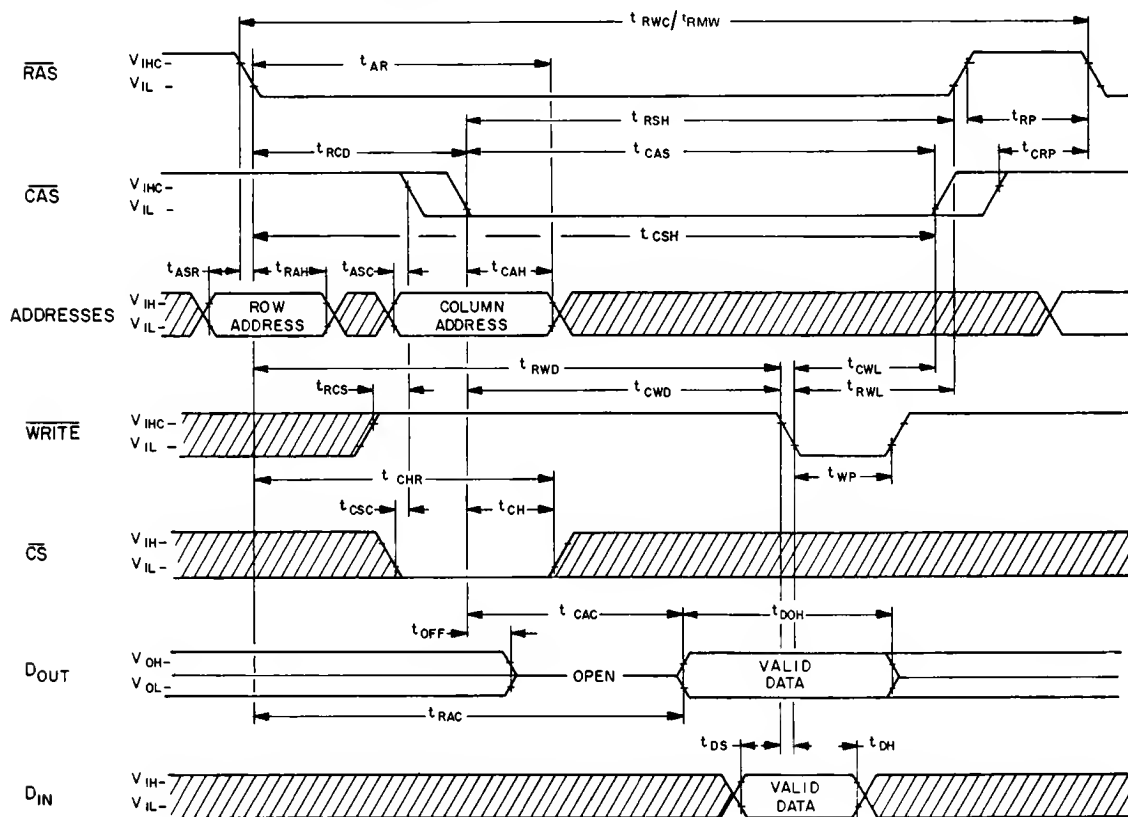
READ CYCLE



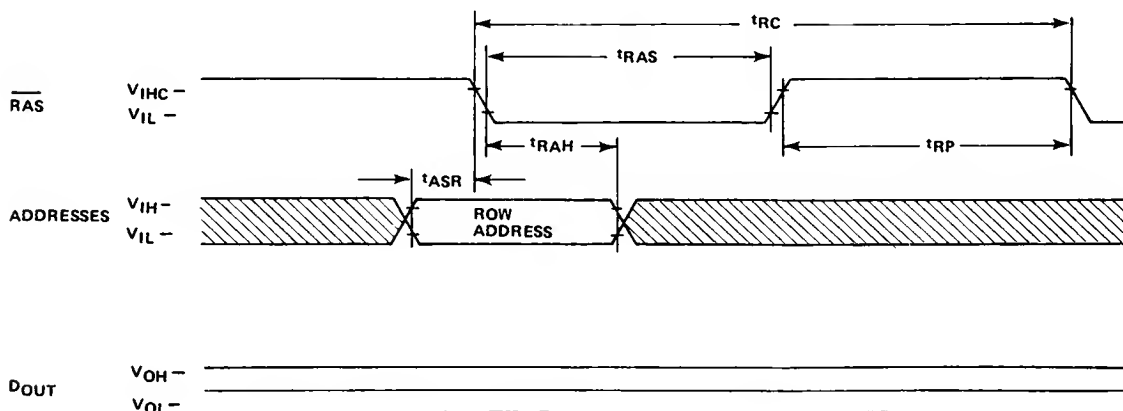
EARLY WRITE



READ-WRITE / READ-MODIFY-WRITE CYCLE



"RAS ONLY" REFRESH CYCLE



NOTE: **DOUT** remains unchanged from previous cycle.

DYNAMIC RAMS



ADDRESSING

The 12 address bits required to decode 1 of the 4096 cell locations within the MK 4027 are multiplexed onto the 6 address inputs and latched into the on-chip address latches by externally applying two negative going TTL level clocks. The first clock, the Row Address Strobe (RAS), latches the 6 row address bits into the chip. The second clock, the Column Address Strobe (CAS), subsequently latches the 6 column address bits plus Chip Select (CS) into the chip. The internal circuitry of the MK 4027 is designed to allow the column information to be externally applied to the chip before it is actually required. Because of this, the hold time requirements for the input signals associated with the Column Address Strobe are also referenced to RAS. However, this gated CAS feature allows the system designer to compensate for timing skews that may be encountered in the multiplexing operation. Since the Chip Select signal is not required until CAS time, which is well into the memory cycle, its decoding time does not add to system access or cycle time.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of WRITE and CAS while RAS is active. The later of the signals (WRITE or CAS) to make its negative transition is the strobe for the Data In register. This permits several options in the write cycle timing. In a write cycle, if the WRITE input is brought low prior to CAS, the Data In is strobed by CAS, and the set-up and hold times are referenced to CAS. If the data input is not available at CAS time or if it is desired that the cycle be a read-write cycle, the WRITE signal must be delayed until after CAS. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of WRITE rather than to CAS. (To illustrate this feature, Data In is referenced to WRITE in the timing diagram depicting the read-write and page mode write cycles while the "early write" cycle diagram shows Data In referenced to CAS.) Note that if the chip is unselected (CS high at CAS time) WRITE commands are not executed and, consequently, data stored in the memory is unaffected.

Data is retrieved from the memory in a read cycle by maintaining WRITE in the inactive or high state throughout the portion of the memory cycle in which CAS is active. Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT LATCH

Any change in the condition of the Data Out Latch is initiated by the CAS signal. The output buffer is not affected by memory (refresh) cycles in which only the RAS signal is applied to the MK 4027.

Whenever $\overline{\text{CAS}}$ makes a negative transition, the output will go unconditionally open-circuited, independent of the state of any other input to the chip. If the cycle in progress is a read, read-modify-write, or a delayed write cycle and the chip is selected, then the output latch and buffer will again go active and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle in progress is a write cycle (WRITE active low before CAS goes low) and the chip is selected, then at access time the output latch and buffer will contain the input data. Once having gone active, the output will remain valid until the MK 4027 receives the next CAS negative edge. Intervening refresh cycles in which a RAS is received (but no CAS) will not cause valid data to be affected. Conversely, the output will assume the open-circuit state during any cycle in which the MK 4027 receives a CAS but no RAS signal (regardless of the state of any other inputs). The output will also assume the open circuit state in normal cycles (in which both RAS and CAS signals occur) if the chip is unselected.

The three-state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The output resistance to V_{CC} (logic 1 state) is $420\ \Omega$ maximum and $135\ \Omega$ typically. The output resistance to V_{SS} (logic 0 state) is $125\ \Omega$ maximum and $35\ \Omega$ typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4027 refresh operation. This allows all system logic except the RAS timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses within each 2 millisecond time interval. Any cycle in which a RAS signal occurs, accomplishes a refresh operation. A read cycle will refresh the selected row, regardless of the state of the Chip Select (CS) input. A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the selected cell. If, during a refresh cycle, the MK 4027 receives a RAS signal but no CAS signal, the state of the output will not be affected. However, if "RAS-only" refresh cycles (where RAS is the only signal applied to the chip) are continued for extended periods, the output buffer may eventually lose proper data and go open-circuit. The output buffer will regain activity with the first cycle in which a CAS signal is applied to the chip.

POWER DISSIPATION/STANDBY MODE

Most of the circuitry used in the MK 4027 is dynamic and most of the power drawn is the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency rather than active duty cycle. Typically, the power is 170mW at 1 μ sec cycle rate for the MK 4027 with a worse case power of less than 470mW at 320nsec cycle time. To minimize the overall system power, the Row Address Strobe (RAS) should be decoded and supplied to only the selected chips. The CAS must be supplied to all chips (to turn off the unselected output). Those chips that did not receive a RAS, however, will not dissipate any power on the CAS edges, except for that required to turn off the outputs. If the RAS signal is decoded and supplied only to the selected chips, then the Chip Select (CS) input of all chips can be at a logic 0. The chips that receive a CAS but no RAS will be unselected (output open-circuited) regardless of the Chip Select input. For refresh cycles, however, either the CS input of all chips must be high or the CAS input must be held high to prevent several "wire-OR'd" outputs from turning on with opposing force. Note that the MK 4027 will dissipate considerably less power when the refresh operation is accomplished with a "RAS-only" cycle as opposed to a normal RAS/CAS memory cycle.

PAGE MODE OPERATION

The "Page Mode" feature of the MK 4027 allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and keeping the RAS signal at a logic 0 throughout all successive memory cycles in which the row address is common.

This "page mode" of operation will not dissipate the power associated with the negative going edge of RAS. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times. The chip select input (CS) is operative in page mode cycles just as in normal cycles. It is not necessary that the chip be selected during the first operation in a sequence of page cycles. Likewise, the CS input can be used to select or disable any cycle(s) in a series of page cycles. This feature allows the page boundary to be extended beyond the 64 column locations in a single chip. The page boundary can be extended by applying RAS to multiple 4K memory blocks and decoding CS to select the proper block.

POWER UP

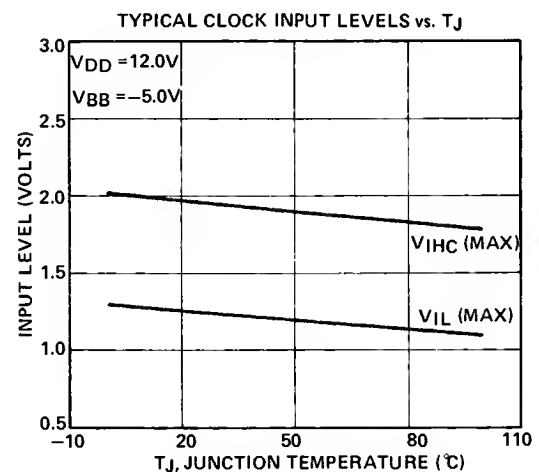
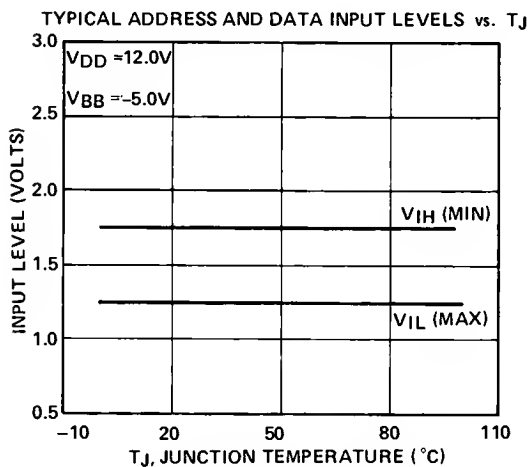
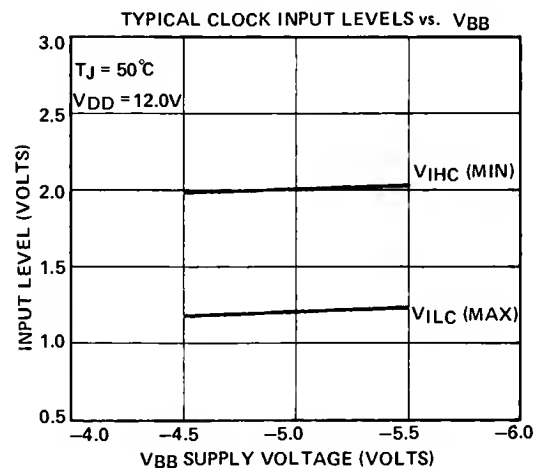
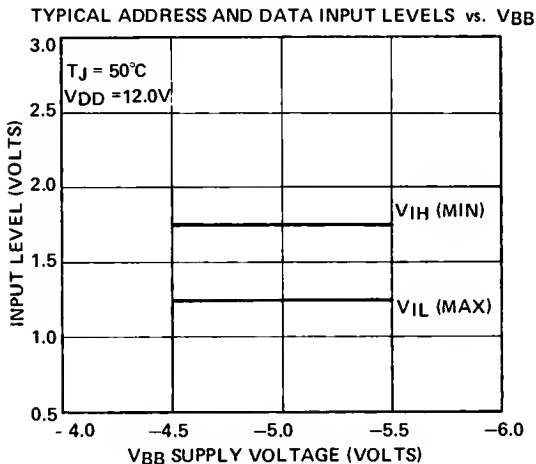
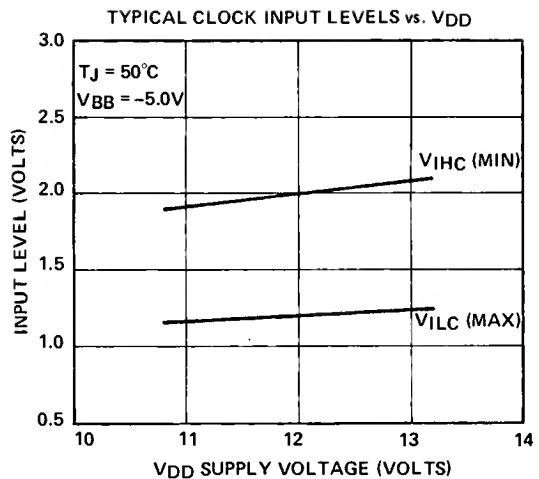
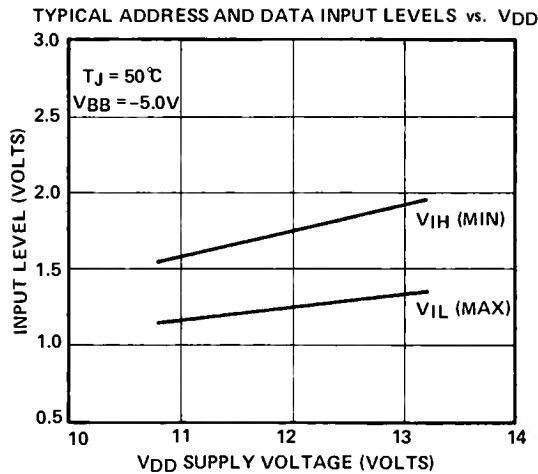
The MK 4027 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, MOSTEK recommends sequencing of power supplies such that VBB is applied first and removed last. VBB should never be more positive than VSS when power is applied to VDD.

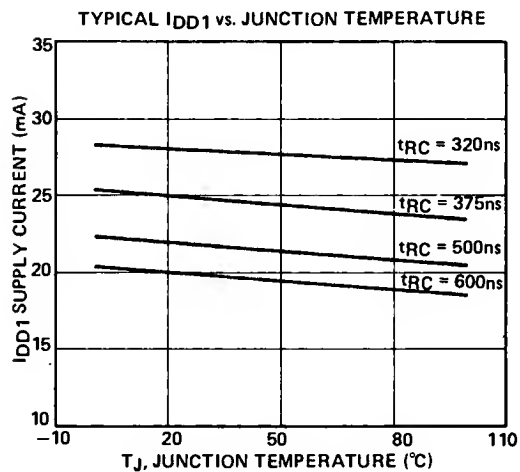
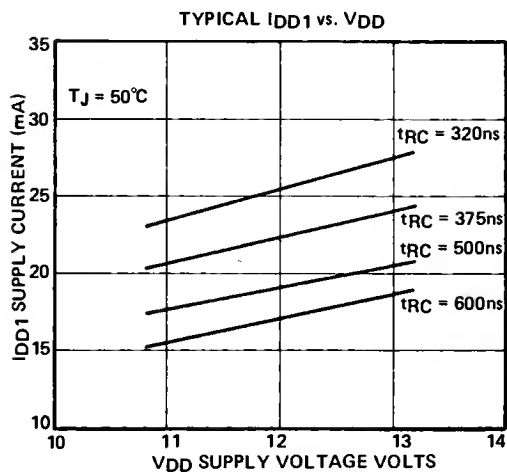
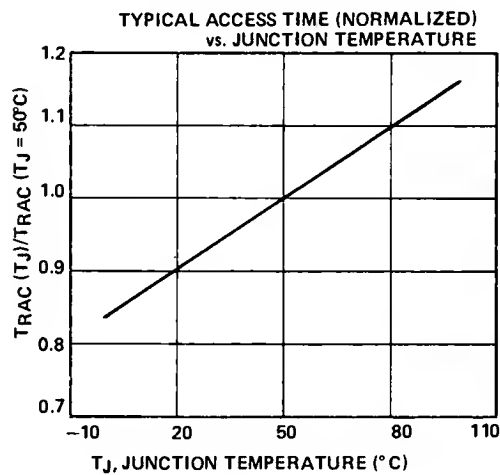
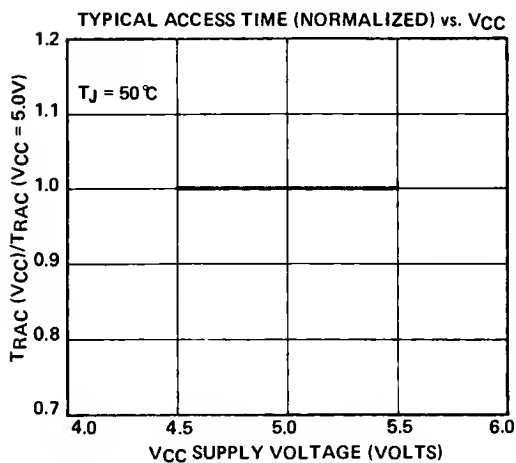
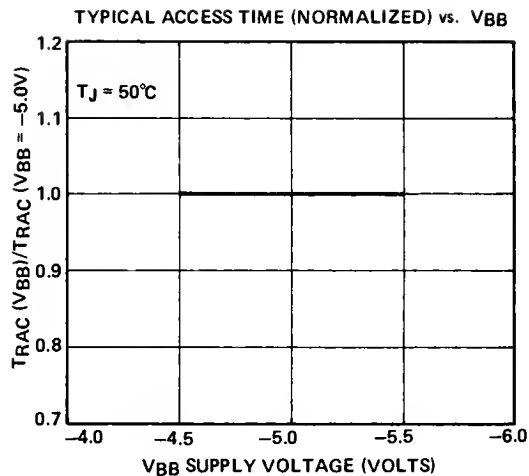
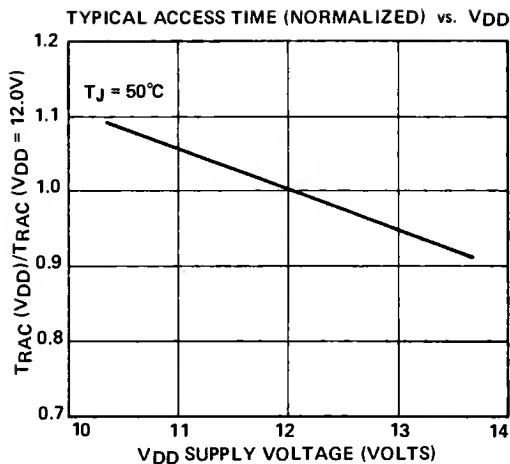
Under system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing RAS and Data Out to the inactive state.

After power is applied to the device, the MK 4027 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

DYNAMIC
RAMS

TYPICAL DEVICE CHARACTERISTICS





FEATURES

- Industry standard 16-pin DIP (MK.4096) configuration
- 250ns access time, 380ns cycle
- $\pm 10\%$ tolerance on all supplies (+12V, $\pm 5V$)
- ECL compatible on V_{BB} power supply ($-5.7V$)
- Low Power: 462mW active (max)
27mW standby (max)
- Improved performance with "gated \overline{CAS} ", " \overline{RAS} only" refresh and page mode capability
- All inputs are low capacitance and TTL compatible
- Input latches for addresses, chip select and data in
- Three-state TTL compatible output
- Output data latched and valid into next cycle

DESCRIPTION

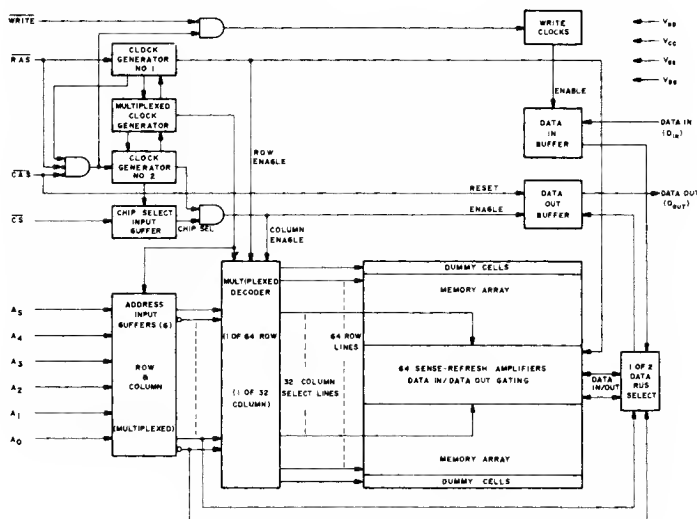
The MK 4027 is a 4096 word by 1 bit MOS random access memory circuit fabricated with MOSTEK's N-channel silicon gate process. This process allows the MK 4027 to be a high performance state-of-the-art memory circuit that is manufacturable in high volume. The MK 4027 employs a single transistor storage cell utilizing a dynamic storage technique and dynamic control circuitry to achieve optimum performance with low power dissipation.

A unique multiplexing and latching technique for the address inputs permits the MK 4027 to be packaged in a standard 16-pin DIP on 0.3 in. centers. This package size provides high system-bit densities and is compatible with widely available automated testing and insertion equipment.

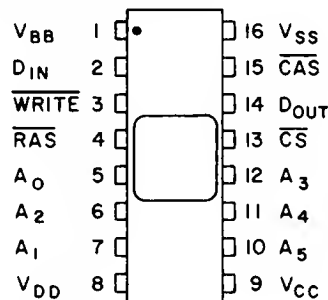
System oriented features include direct interfacing capability with TTL, only 6 very low capacitance address lines to drive, on-chip address and data registers which eliminates the need for interface registers, input logic levels selected to optimize noise immunity, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MK 4027 also incorporates several flexible operating modes. In addition to the usual read and write cycles, read-modify write, page-mode, and \overline{RAS} -only refresh cycles are available with the MK 4027. Page-mode timing is very useful in systems requiring Direct Memory Access (DMA) operation.

DYNAMIC RAMS

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A ₀ -A ₅	ADDRESS INPUTS
\overline{CAS}	COLUMN ADDRESS STROBE
\overline{CS}	CHIP SELECT
D _{IN}	DATA IN
D _{OUT}	DATA OUT
\overline{RAS}	ROW ADDRESS STROBE
WRITE	READ/WRITE INPUT
V_{BB}	POWER (-5V)
V_{CC}	POWER (+5V)
V_{DD}	POWER (+12V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB}	-0.5V to +20V
Voltage on V_{DD} , V_{CC} relative to V_{SS}	-1.0V to +15V
$V_{BB}-V_{SS}$ ($V_{DD}-V_{SS} > 0$)	0V
Operating temperature, T_A (Ambient)	0°C to +70°C
Storage temperature (Ambient)(Ceramic)	-65°C to +150°C
Storage temperature (Ambient)(Plastic)	-55°C to +125°C
Short Circuit Output Current	50mA
Power dissipation	1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS⁴ (0°C ≤ T_A ≤ 70°C)¹

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	10.8	12.0	13.2	volts	2
V_{CC}	Supply Voltage	4.5V	5.0	5.5	volts	2,3
V_{SS}	Supply Voltage	0	0	0	volts	2
V_{BB}	Supply Voltage	-4.5	-5.0	-5.7	volts	2
V_{IHC}	Logic 1 Voltage, \overline{RAS} , \overline{CAS} , \overline{WRITE}	2.4		7.0	volts	2
V_{IH}	Logic 1 Voltage, all inputs except \overline{RAS} , \overline{CAS} , \overline{WRITE}	2.2		7.0	volts	2
V_{IL}	Logic 0 Voltage, all inputs	-1.0		.8	volts	2

DC ELECTRICAL CHARACTERISTICS⁴ (0°C ≤ T_A ≤ 70°C)¹ ($V_{DD} = 12.0V \pm 10\%$; $V_{CC} = 5.0V \pm 10\%$; $V_{SS} = 0V$; $-5.7V \leq V_{BB} \leq -4.5V$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{DD1}	Average V_{DD} Power Supply Current			35	mA	5
I_{DD2}	Standby V_{DD} Power Supply Current			2	mA	8
I_{DD3}	Average V_{DD} Power Supply Current during "RAS only" cycles			25	mA	
I_{CC}	V_{CC} Power Supply Current				mA	6
I_{BB}	Average V_{BB} Power Supply Current			150	μA	
$I_{I(L)}$	Input Leakage Current (any input)			10	μA	7
$I_{O(L)}$	Output Leakage Current			10	μA	8,9
V_{OH}	Output Logic 1 Voltage @ $I_{OUT} = -5mA$	2.4			volts	
V_{OL}	Output Logic 0 Voltage @ $I_{OUT} = 3.2mA$			0.4	volts	

NOTES

- T_A is specified for operation at frequencies to $t_{RC} \geq t_{RC}(\min)$.
- All voltages referenced to V_{SS} .
- Output voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the $V_{OH}(\min)$ specification is not guaranteed in this mode.
- Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
- Current is proportional to cycle rate. $I_{DD1}(\max)$ is measured at the cycle rate specified by $t_{RC}(\min)$. See figure 1 for I_{DD1} limits at other cycle rates.
- I_{CC} depends on output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to Data Out. At all other times I_{CC} consists of leakage currents only.
- All device pins at 0 volts except V_{BB} which is at -5 volts and the pin under test which is at +10 volts.
- Output is disabled (high-impedance) and \overline{RAS} and \overline{CAS} are both at a logic 1. Transient stabilization is required prior to measurement of this parameter.
- $0V \leq V_{OUT} \leq +10V$.
- Effective capacitance is calculated from the equation:
$$C = \frac{\Delta Q}{\Delta V}$$
 with $\Delta V = 3$ volts.
- A.C. measurements assume $T_T = 5ns$.
- The specifications for $t_{RC}(\min)$ and $t_{RWC}(\min)$ are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS(4, 11, 17)
 (0° C ≤ T_A ≤ 70° C)¹ (V_{DD} = 12.0V ± 10%, V_{CC} = 5.0V ± 10%, V_{SS} = 0V, -5.7V ≤ V_{BB} ≤ -4.5V)

	PARAMETER	MK4027-4		UNITS	NOTES
		MIN	MAX		
t _{RC}	Random read or write cycle time	380		ns	12
t _{RWC}	Read write cycle time	395		ns	12
t _{RMW}	Read modify write cycle time	470		ns	12
t _{PC}	Page mode cycle time	285		ns	12
t _{RAC}	Access time from row address strobe		250	ns	13,15
t _{CAC}	Access time from column address strobe		165	ns	14,15
t _{OFF}	Output buffer turn-off delay	0	60	ns	
t _{RP}	Row address strobe precharge time	120		ns	
t _{RAS}	Row address strobe pulse width	250	10,000	ns	
t _{RSH}	Row address strobe hold time	165		ns	
t _{CAS}	Column address strobe pulse width	165		ns	
t _{CSH}	Column address strobe hold time	250		ns	
t _{RCD}	Row to column strobe delay	35	85	ns	16
t _{ASR}	Row address set-up time	0		ns	
t _{RAH}	Row address hold time	35		ns	
t _{ASC}	Column address set-up time	-10		ns	
t _{CAH}	Column address hold time	75		ns	
t _{AR}	Column address hold time referenced to $\overline{\text{RAS}}$	160		ns	
t _{CSC}	Chip select set-up time	-10		ns	
t _{CH}	Chip select hold time	75		ns	
t _{CHR}	Chip select hold time referenced to $\overline{\text{RAS}}$	160		ns	
t _T	Transition time (rise and fall)	3	50	ns	17
t _{RCS}	Read command set-up time	0		ns	
t _{RCH}	Read command hold time	0		ns	
t _{WCH}	Write command hold time	75		ns	
t _{WCR}	Write command hold time referenced to $\overline{\text{RAS}}$	160		ns	
t _{WP}	Write command pulse width	75		ns	
t _{RWL}	Write command to row strobe lead time	85		ns	
t _{CWL}	Write command to column strobe lead time	85		ns	
t _{DS}	Data in set-up time	0		ns	18
t _{DH}	Data in hold time	75		ns	18
t _{DHR}	Data in hold time referenced to $\overline{\text{RAS}}$	160		ns	
t _{CRP}	Column to row strobe precharge time	0		ns	
t _{CP}	Column precharge time	110		ns	
t _{RFSH}	Refresh period		2	ms	
t _{WCS}	Write command set-up time	0		ns	19
t _{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ delay	90		ns	19
t _{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ delay	175		ns	19
t _{DOH}	Data out hold time	10		μs	

DYNAMIC
RAMS

Notes Continued

13. Assumes that t_{RC} ≤ t_{RC} (max.).

14. Assumes that t_{RC} ≥ t_{RC} (max.).

15. Measured with a load circuit equivalent to 2 TTL loads and 100pF

16. Operation within the t_{RC} (max) limit insures that t_{RAC} (max) can be met. t_{RC} (max) is specified as a reference point only; if t_{RC} is greater than the specified t_{RC} (max) limit, then access time is controlled exclusively by t_{CAC}.

17. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

18. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in random write cycles and to $\overline{\text{WRITE}}$ leading edge in delayed write or read-modify-write cycles.

19. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in a read/write or read/modify/write cycle only. If t_{WCS} ≥ t_{WCS} (min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If t_{CWD} ≥ t_{CWD} (min) and t_{RWD} ≥ t_{RWD} (min), the cycle is a read-write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.

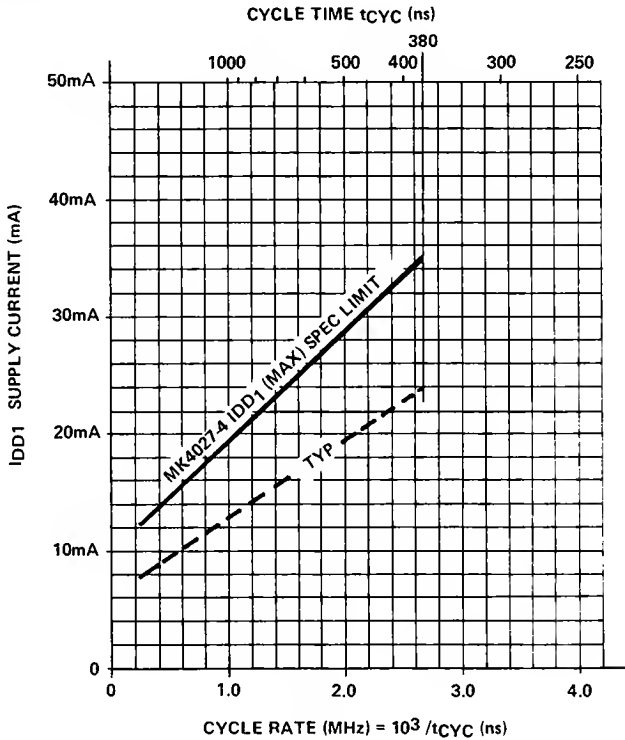
AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{DD} = 12.0V ± 10%; V_{SS} = 0V; -5.7V ≤ V_{BB} ≤ -4.5V)

	PARAMETER	TYP	MAX	UNITS	NOTES
C 11	Input Capacitance (A ₀ -A ₅), D _{1N} , \overline{CS}	4	5	pF	10
C 12	Input Capacitance \overline{RAS} , \overline{CAS} , WRITE	8	10	pF	10
C 0	Output Capacitance (D _{OUT})	5	7	pF	8,10

MAXIMUM I_{DD1} vs. CYCLE RATE FOR DEVICE OPERATION
AT EXTENDED FREQUENCIES

Figure 1



SUPPLEMENT - To be used in conjunction with MK4027(J/N)-1/2/3 data sheet.

MOSTEK®

4096 x 1-BIT DYNAMIC RAM

MK4096(K/N)-6/16/11

FEATURES

- Industry standard 16-pin DIP configuration (available in plastic (N) and ceramic (K) packages)
- All inputs are low capacitance and TTL compatible
- Input latches for address, chip select and data in
- Inputs protected against static charge
- Three-state TTL compatible output, latched and valid into next cycle
- Proven reliability with high performance

DESCRIPTION

The MK 4096 is the recognized industry standard 4096 word by 1 bit MOS Random Access Memory circuit packaged in a standard 16-pin DIP on 0.3 inch centers. This package configuration is made possible by a unique multiplexing and latching technique for the address inputs. The use of the 16-pin DIP for the MK 4096 provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

The MK 4096 is fabricated with MOSTEK's standard Self-Aligned, Poly-Interconnect, N-Channel (SPIN) process. The SPIN process allows the MK 4096 to be a highly manufacturable, state-of-the-art memory circuit that exhibits the reliability and performance standards necessary for today's (and tomorrow's) data processing applications. The MK 4096 employs a single transistor storage cell, utilizing a dynamic storage technique and dynamic control circuitry to

achieve optimum performance with low power dissipation.

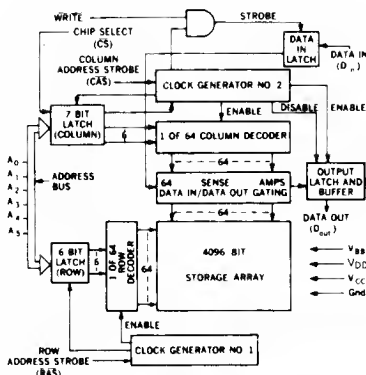
System oriented features incorporated within the MK 4096 include direct interfacing capability with TTL, 6 instead of 12 address lines to drive, on-chip registers which can eliminate the need for interface registers, input logic levels selected to optimize the noise immunity, and two chip select methods to allow the user to determine the speed/power characteristics of his memory system.

DYNAMIC RAMS

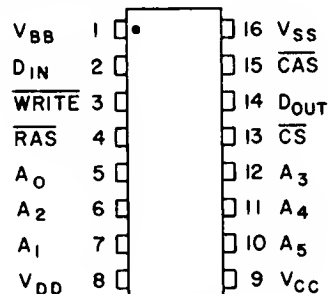
Part Number	Access Time	Cycle Time	Max Power*
MK 4096-6	250 ns	375 ns	450mW
MK 4096-16	300 ns	425 ns	385mW
MK 4096-11	350 ns	500 ns	320mW

*Standby power for all parts < 19mW

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A ₀ - A ₅	ADDRESS INPUTS	D _{IN}	DATA IN
CAS	COLUMN ADDRESS STROBE	D _{OUT}	DATA OUT
CS	CHIP SELECT	V _{BB}	POWER (-5V)
RAS	ROW ADDRESS STROBE	V _{CC}	POWER (+5V)
WRITE	READ/WRITE INPUT	V _{DD}	POWER (+12V)
		V _{SS}	GROUND

NOT FOR NEW DESIGN

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} . . . $-0.5V$ to $+25V$
 $(V_{SS}-V_{BB} \geq 4.5V)$
 Operating temperature T_A (Ambient) . . . $0^\circ C$ to $+70^\circ C$
 Storage temperature (Ceramic) $-65^\circ C$ to $+150^\circ C$
 Storage temperature (Plastic) $-55^\circ C$ to $+125^\circ C$
 Power dissipation 1Watt
 Data out current 50mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS (17) $(0^\circ C \leq T_A \leq +70^\circ C)$

	PARAMETER	MK 4096-6		MK 4096-16		MK 4096-11		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
V_{DD}	Supply Voltage	11.4	12.6	11.4	12.6	11.4	12.6	Volts	1
V_{CC}	Supply Voltage	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	Volts	1,2
V_{SS}	Supply Voltage	0	0	0	0	0	0	Volts	1
V_{BB}	Supply Voltage	-4.5	-5.5	-4.5	-5.5	-4.5	-5.5	Volts	1
V_{IH}	Logic 1 Voltage - RAS, CAS, WRITE	2.7	7.0	2.7	7.0	3.0	7.0	Volts	1,3
V_{IH}	Logic 1 Voltage, all inputs except RAS, CAS, WRITE	2.4	7.0	2.4	7.0	2.4	7.0	Volts	1,3
V_{IL}	Logic 0 Voltage, all inputs	-1.0	0.8	-1.0	0.8	-1.0	0.8	Volts	1,3

DC ELECTRICAL CHARACTERISTICS (17) $(0^\circ C \leq T_A \leq 70^\circ C)(V_{DD} = 12.0V \pm 5\%; V_{CC} = 5.0V \pm 10\%; V_{SS} = 0V; V_{BB} = -5.0V \pm 10\%)$

PARAMETER		MK4096-6		MK4096-16		MK4096-11		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
I_{DD1}	Average V_{DD} Power Supply Current		35		30		25	mA	4
I_{CC}	V_{CC} Power Supply Current							mA	5
I_{BB}	Average V_{BB} Power Supply Current		75		75		75	μA	
I_{DD2}	Standby V_{DD} Power Supply Current		1.5		1.5		1.5	mA	7
I_{DD3}	Average V_{DD} Supply Current during "RAS-only" cycles		25		22		18	mA	4
$I_{I(L)}$	Input Leakage Current (any input)		5		5		5	μA	6
$I_{O(L)}$	Output Leakage Current		10		10		10	μA	7,8
V_{OH}	Output Logic 1 Voltage @ $I_{OUT} = -5mA$	2.4		2.4		2.4		Volts	2
V_{OL}	Output Logic 0 Voltage @ $I_{OUT} = 2mA$		0.4		0.4		0.4	Volts	

NOTES

- All voltages referenced to V_{SS} . V_{BB} must be applied to and removed from the device within 5 seconds of V_{DD} .
- Output voltage will swing from V_{SS} to V_{CC} if $V_{CC} \leq V_{DD} - 4$ volts. If $V_{CC} \geq V_{DD} - 4$ volts, the output will swing from V_{SS} to a voltage somewhat less than V_{DD} .
- Device speed is not guaranteed at input voltages greater than TTL levels (0 to 5V).
- Current is proportional to cycle rate; maximum current is measured at the fastest cycle rate.
- I_{CC} depends upon output loading. The V_{CC} supply is connected to the output buffer only.
- All device pins at 0 volts except V_{BB} which is at -5 volts and the pin under test which is at +10 volts.
- Output is disabled (open-circuit) and \overline{RAS} and \overline{CAS} are both at a logic 1.
- $0V \leq V_{OUT} \leq +10V$.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (10, 15,17)
(0°C ≤ T_A ≤ 70°C) (V_{DD} = 12.0V ± 5%, V_{CC} = 5.0V ± 10%, V_{SS} = 0V, V_{BB} = −5.0V ± 10%)

PARAMETER		MK 4096-6		MK 4096-16		MK 4096-11		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t _{RC}	Random Read or Write Cycle Time	375		425		500		nsec	11
t _{RAC}	Access time from Row Address Strobe		250		300		350	nsec	11,13
t _{CAC}	Access Time from Column Address Strobe		140		165		200	nsec	12,13
t _{OFF}	Output Buffer Turn-Off Delay	0	65	0	80	0	100	nsec	
t _{RP}	Row Address Strobe Precharge Time	115		125		150		nsec	
t _{RAS}	Row Address Strobe Pulse Width	250	10,000	300	10,000	350	10,000	nsec	
t _{RCL}	Row To Column Strobe Lead Time	60	110	80	135	100	150	nsec	14
t _{CAS}	Column Address Strobe Pulse Width	140		165		200		nsec	12
t _{AS}	Address Set-Up Time	0		0		0		nsec	
t _{AH}	Address Hold Time	60		80		100		nsec	
t _{CH}	Chip Select Hold Time	100		100		100		nsec	
t _T	Rise and Fall Times	3	50	3	50	3	50	nsec	15
t _{RCS}	Read Command Set-Up Time	0		0		0		nsec	
t _{RCH}	Read Command Hold Time	0		0		0		nsec	
t _{WCH}	Write Command Hold Time	110		130		150		nsec	
t _{WP}	Write Command Pulse Width	110		130		150		nsec	
t _{CRL}	Column to Row Strobe Lead Time	−40	+40	−50	+50	−50	+50	nsec	
t _{CWL}	Write Command to Column Strobe Lead Time	110		130		150		nsec	
t _{DS}	Data In Set-Up Time	0		0		0		nsec	16
t _{DH}	Data In Hold Time	110		130		150		nsec	16
t _{RFSH}	Refresh Period		2		2		2	msec	
t _{MOD}	Modify Time		10		10		10	μsec	
t _{DOH}	Data Out Hold Time	10		10		10		μsec	

**DYNAMIC
RAMS**

NOTES Continued

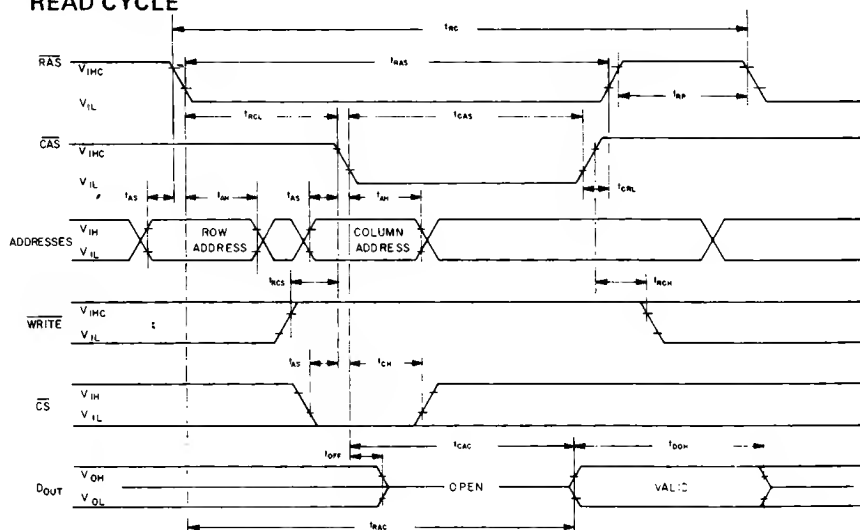
- Capacitance measured with Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I \Delta t}{\Delta V}$ with current equal to a constant 20mA and $\Delta V = 3V$.
- AC measurements assume t_T = 5ns.
- Assumes that t_{RCL} + t_T ≤ t_{RCL} (max).
- Assumes that t_{RCL} + t_T ≥ t_{RCL} (max).
- Measured with a load circuit equivalent to 1 TTL load and C_L = 100pF
- Operation within the t_{RCL} (max) limit insures that t_{RAC} (max) can be met. t_{RCL} (max) is specified as a reference point only; if t_{RCL} is greater than the specified t_{RCL} (max) limit, then access time is controlled exclusively by t_{CAC} and t_{RAS}. t_{RAC} and t_{RCL} will be longer by the amount t_{RCL} + t_T exceeds t_{RCL} (max).
- V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
- These parameters are referenced to \overline{CAS} leading edge in random write cycles and to \overline{WRITE} leading edge in delayed write or read-modify-write cycles.
- After the application of supply voltages or after extended periods of operation without clocks, the device must perform a minimum of one initialization cycle (any valid memory cycle containing both \overline{RAS} and \overline{CAS}) prior to normal operation.

(0°C ≤ T_A ≤ +70°C) (V_{DD} = 12.0V ± 5%, V_{CC} = 5.0V ± 10%, V_{SS} = 0V, V_{BB} = -5.0V ± 10%)

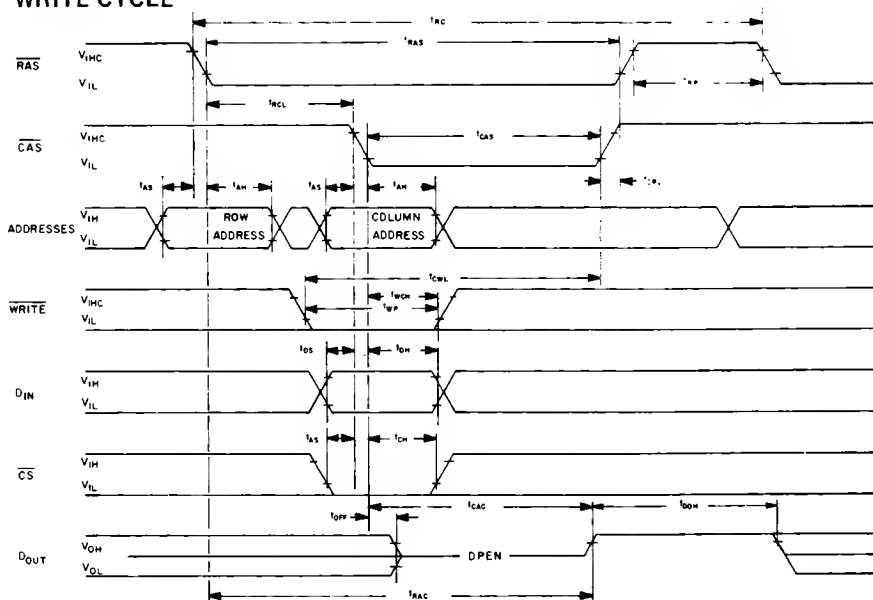
PARAMETER		TYP	MAX	UNITS	NOTES
C _{I1}	Input Capacitance (A ₀ – A ₅)	7	10	pF	9
C _{I2}	Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, D _{IN} , WRITE, $\overline{\text{CS}}$)	5	7	pF	9
C _O	Output Capacitance (D _{OUT})	5	8	pF	7,9

TIMING WAVEFORMS

READ CYCLE

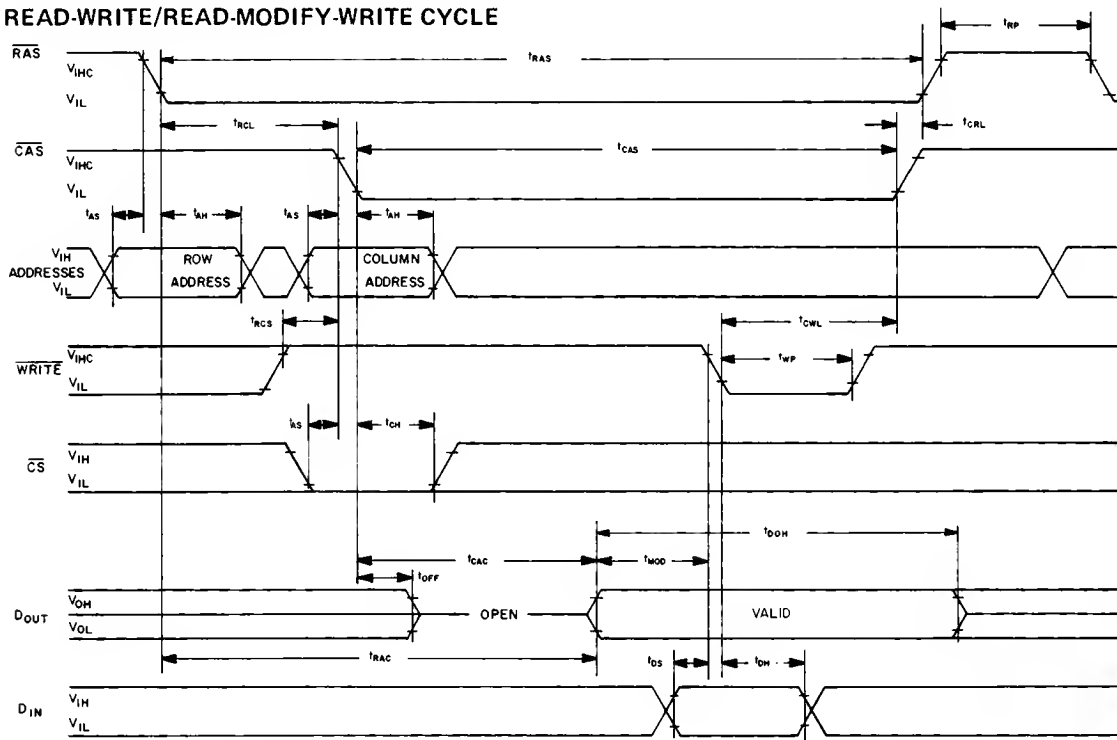


WRITE CYCLE



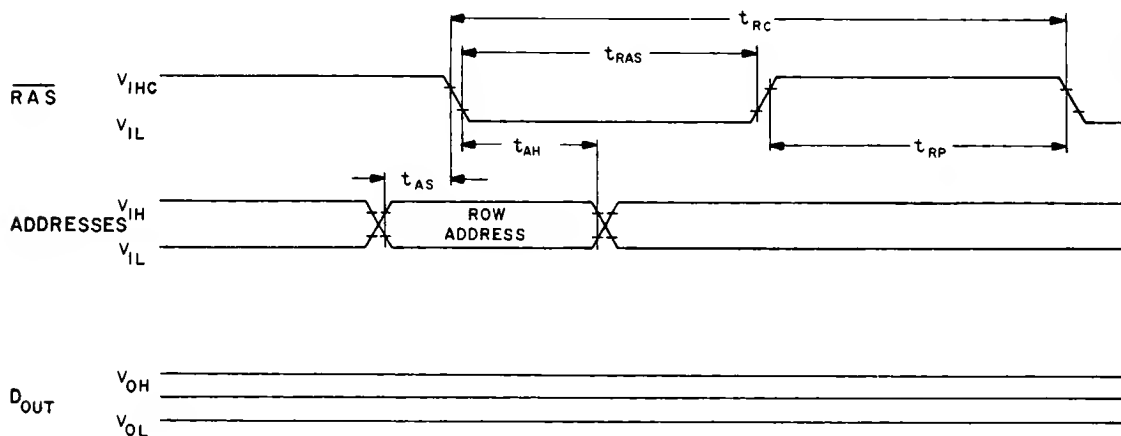
TIMING WAVEFORMS

READ-WRITE/READ-MODIFY-WRITE CYCLE



DYNAMIC
RAMS

"RAS ONLY" REFRESH CYCLE



NOTE:

Prior to the first memory cycle following a period (beyond 2mS) of "RAS-only refresh, a memory-cycle employing both RAS and CAS must be performed to insure proper device operation.

ADDRESSING

The 12 address bits required to decode one of the 4096 cell locations within the MK 4096 are multiplexed onto the 6 address inputs and latched into the on-chip address latches by externally applying two negative going TTL level clocks. The first clock, the Row Address Strobe (RAS), latches the 6 row address bits into the chip. The second clock, the Column Address Strobe (CAS), subsequently latches the 6 column address bits plus Chip Select (CS) into the chip. (Note that since the Chip Select signal is not required until CAS time, which is well into the memory cycle, its decoding time does not add to system access or cycle time). Each of these signals, RAS and CAS, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the CAS clock sequence are inhibited until the occurrence of a delayed signal derived from the RAS clock chain. This "gated CAS" feature allows the CAS clock to be externally activated as soon as the Row Address Hold Time specification (t_{AH}) has been satisfied and the 6 address inputs have been changed from Row address to Column address information.

Note that \overline{CAS} can be activated at any time after t_{AH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing end points result from the internal gating of CAS which are called t_{RCL} (min) and t_{RCL} (max). No data storage or reading errors will result if CAS is applied to the MK 4096 at a point in time beyond the t_{RCL} (max) limit. However, access time will then be determined exclusively by the access time from CAS (t_{CAC}) rather than from RAS (t_{RAC}), and access time from RAS will be lengthened by the amount that t_{RCL} exceeds the t_{RCL} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of WRITE and CAS while RAS is active. The later of the signals (WRITE or CAS) to make its negative transition is the strobe for the Data In register. This permits several options in the write cycle timing. In a write cycle, if the WRITE input is brought low prior to CAS, the Data In is strobed by CAS, and the set-up and hold times are referenced to CAS. If the data input is not available at CAS time or if it is desired that the cycle be a read-write or read-modify-write cycle, the WRITE signal must be delayed until after CAS. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of WRITE rather than to CAS.

(To illustrate this feature, Data In is referenced to WRITE in the timing diagram depicting the read-modify-write cycle while the "early write" cycle diagram shows Data In referenced to CAS). Note that if the chip is unselected (CS high at CAS time) WRITE commands are not executed and, consequently, data stored in the memory is unaffected.

Data is retrieved from the memory in a read cycle by maintaining WRITE in the inactive or high state throughout the portion of the memory cycle in which CAS is active. Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT LATCH

Any change in the condition of the Data Out Latch is initiated by the CAS signal. The output buffer is not affected by memory (refresh) cycles in which only the RAS signal is applied to the MK 4096. Whenever CAS makes a negative transition, the output will go unconditionally open-circuited, independent of the state of any other input to the chip. If the cycle in progress is a read, read-modify-write, or a delayed write cycle and the chip is selected, then the output latch and buffer will again go active and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle in progress is a write cycle (WRITE active low before CAS goes low) and the chip is selected, then at access time the output latch and buffer will contain a logic 1. Once having gone active, the output will remain valid until the MK 4096 receives the next CAS negative edge. Intervening refresh cycles in which a RAS is received (but no CAS) will not cause valid data to be affected. Conversely, the output will assume the open-circuit state during any cycle in which the MK 4096 receives a CAS but no RAS signal (regardless of the state of any other inputs). The output will also assume the open-circuit state in normal cycles (in which both RAS and CAS signals occur) if the chip is unselected.

The three-state data output buffer presents the data output pin with a low impedance to VCC for a logic 1 and a low impedance to VSS for a logic 0. The effective resistance to VCC (logic 1 state) is 500 Ω maximum and 150 Ω typically. The resistance to VSS (logic 0 state) is 200 Ω maximum and 100 Ω typically. The separate VCC pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the VCC pin may have power removed without affecting the MK 4096 refresh operation. This allows all system logic except the RAS/CAS timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses within each 2 millisecond time interval. Any cycle in which a RAS signal occurs accomplishes a refresh operation. A read cycle will refresh the selected row, regardless of the Chip Select (CS) input. A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the selected cell.

For standby operation, a "RAS-only" cycle can be employed to refresh the MK 4096. However, if "RAS-only" refresh cycles (where RAS is the only signal applied to the chip) are continued for extended periods, the output buffer may eventually lose proper

data and go open-circuit. Prior to the first memory cycle following a period (beyond 2ms) of "RAS-only" refresh, a memory cycle employing both RAS and CAS must be performed to precharge the internal circuitry. This "dummy cycle" allows the output buffer to regain activity and enables the device to perform a read or write cycle upon command.

POWER DISSIPATION/STANDBY MODE

Most of the circuitry used in the MK 4096 is dynamic and most of the power drawn is the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency rather than active duty cycle. Typically, the power is 120 mW at a 1 μ sec cycle rate for the MK 4096 with a maximum power of less than 450 mW at 375 nsec cycle time. To minimize the overall system power, the Row Address Strobe (RAS) should be decoded and supplied to only the selected chips. The CAS must be supplied to all chips (to turn off the unselected output). Those chips that did not receive a RAS, however, will not dissipate any power on the CAS edges, except for that required to turn off the outputs. If the RAS signal is decoded and supplied only to the selected chips, then the Chip Select (CS) input of all chips can be at a logic 0. The chips that receive a CAS but no RAS will be unselected (output open-circuited) regardless of the Chip Select input. For refresh cycles, however, either the CS input of all chips must be high or the CAS input must be held high to prevent several "wire-ORed" outputs from turning on with opposing force.

The current waveforms for the current drawn from the V_{DD} and V_{BB} supplies are shown in Figure A. Since the current is pulsed, proper power distribution and bypassing techniques are required to maintain system power supply noise levels at an acceptable level. Low inductance supply lines for V_{DD} and V_{SS} are desirable. One 0.01 microfarad, low inductance, bypass capacitor per two MK 4096 devices and one 6.8 microfarad electrolytic capacitor per eight MK 4096 devices on each of the V_{DD} and V_{BB} supply lines is desirable.

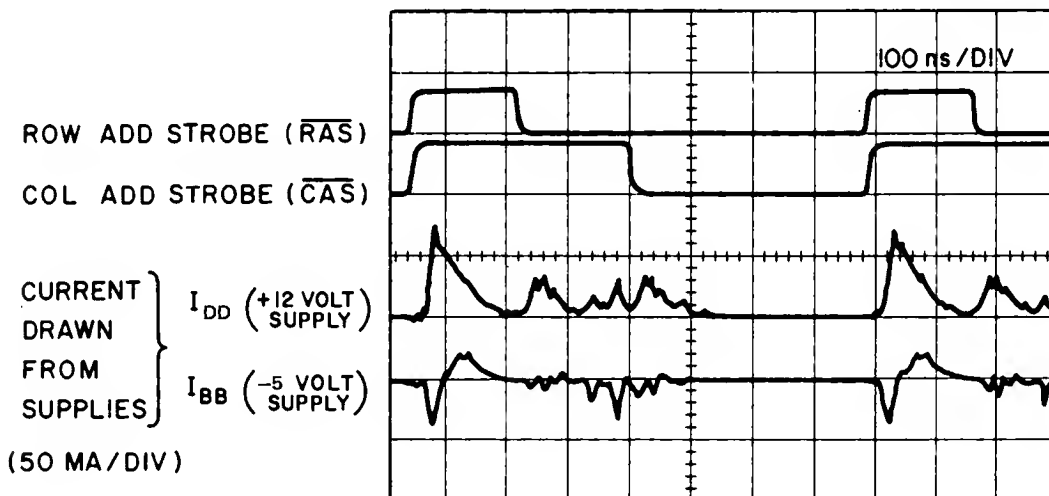
POWER-UP

Under normal operating conditions the MK 4096 requires no particular power-up sequence. However, in order to achieve the most reliable performance from the MK 4096, proper consideration should be given to the V_{BB}/V_{DD} power supply relationship. The V_{BB} supply is an extremely important "protective voltage" since it performs two essential functions within the device. It establishes proper junction isolation and sets field-effect thresholds, both thin field and thick field. Misapplication of V_{BB} or device operation without the V_{BB} supply can affect long term device reliability. For optimum reliability performance from the MK 4096, it is suggested that measures be taken to not have V_{DD} (+12V) applied to the device for over five (5) seconds without the application of V_{BB} (-5V).

After power is applied to the device, the MK 4096 requires at least one memory cycle (RAS/CAS) before proper device operation is achieved. A normal 64 cycle refresh with both RAS and CAS is adequate for this purpose.

POWER SUPPLY CURRENT WAVEFORMS

DYNAMIC RAMS



MOSTEK®

4096x1-BIT DYNAMIC RAM

MK4200(K/N)-11/16

FEATURES

- Industry standard 16-pin DIP configuration (available in plastic (N) and ceramic (K) packages)
- All inputs are low capacitance and TTL compatible, except RAS (MOS level)
- Input latches for address, chip select and data in
- Inputs protected against static charge

- Three-state TTL compatible output, latched and valid into next cycle
- Proven reliability with high performance

Part Number	Access Time	Cycle Time	Max Power*
MK 4200-16	300 ns	425 ns	380 mW
MK 4200-11	350 ns	500 ns	300 mW

*Standby power for all parts <.6 mW

DESCRIPTION

The MK 4200 is a 4096 word by 1 bit MOS Random Access Memory circuit packaged in a standard 16-pin DIP on 0.3 inch centers. This package configuration is made possible by a unique multiplexing and latching technique for the address inputs. The use of the 16-pin DIP for the MK 4200 provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

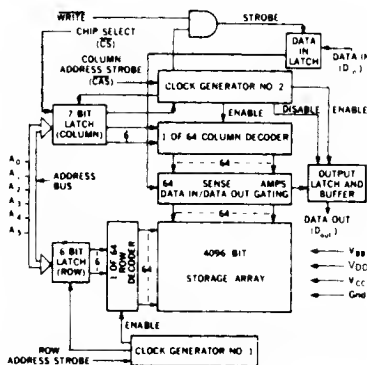
The MK 4200 is fabricated with MOSTEK's standard Self-Aligned, Poly-Interconnect, N-Channel (SPIN) process. The SPIN process allows the MK 4200 to be a highly manufacturable, state-of-the-art memory circuit that exhibits the reliability and performance

standards necessary for today's (and tomorrow's) data processing applications. The MK4200 employs a single transistor storage cell, utilizing a dynamic storage technique and dynamic control circuitry to achieve optimum performance with low power dissipation.

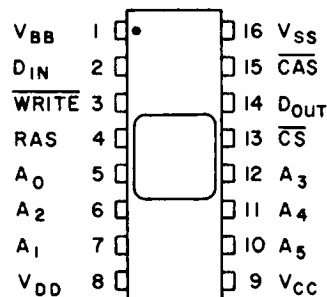
System oriented features incorporated within the MK 4200 include direct interfacing capability with TTL, 6 instead of 12 address lines to drive, on-chip registers, input logic levels selected to optimize the noise immunity, and two chip select methods to allow the user to determine the speed/power characteristics of his memory system.

DYNAMIC
RAMS

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A ₀ - A ₅	ADDRESS INPUTS	DIN	DATA IN
CAS	COLUMN ADDRESS STROBE	DOUT	DATA OUT
CS	CHIP SELECT	VBB	POWER (-5V)
RAS	ROW ADDRESS STROBE	VCC	POWER (+5V)
WRITE	READ/WRITE INPUT	VDD	POWER (+12V)
		VSS	GROUND

NOT FOR NEW DESIGN

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} . . . $-0.5V$ to $+25V$
 $(V_{SS}-V_{BB} \geq 4.5V)$
 Operating temperature T_A (Ambient) . . . $0^\circ C$ to $+70^\circ C$
 Storage temperature (Ceramic) $-65^\circ C$ to $+150^\circ C$
 Storage temperature (Plastic) $-55^\circ C$ to $+125^\circ C$
 Power dissipation 1Watt
 Data out current 50mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS (17)

$(0^\circ C \leq T_A \leq 70^\circ C)$

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	11.4	12.0	12.6	Volts	1
V_{CC}	Supply Voltage	V_{SS}	5.0	V_{DD}	Volts	1,2
V_{SS}	Supply Voltage	0	0	0	Volts	1
V_{BB}	Supply Voltage	-4.5	-5.0	-5.5	Volts	1
V_{IHC}	Logic 1 Voltage, \overline{CAS} , \overline{WRITE}	2.7	5.0	7.0	Volts	1,3
V_{IH}	Logic 1 Voltage, all inputs except RAS, \overline{CAS} , \overline{WRITE}	2.4	5.0	7.0	Volts	1,3
V_{IHR}	Logic 1 Voltage, RAS input	$V_{DD}-1$	12.0	$V_{DD}+1$	Volts	1
V_{IL}	Logic 0 Voltage, all inputs	-1.0	0	0.8	Volts	1,3

DC ELECTRICAL CHARACTERISTICS (17)

$(0^\circ C \leq T_A \leq 70^\circ C)$ ($V_{DD} = 12.0V \pm 5\%$; $V_{CC} = 5.0V \pm 10\%$; $V_{SS} = 0V$; $V_{BB} = -5.0V \pm 10\%$)

PARAMETER		MK 4200-16		MK 4200-11		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{DD1}	Average V_{DD} Power Supply Current		30		25	mA	4
I_{CC}	V_{CC} Power Supply Current					mA	5
I_{BB}	Average V_{BB} Power Supply Current		75		75	μA	
I_{DD2}	Standby V_{DD} Power Supply Current		50		50	μA	7
I_{DD3}	Average V_{DD} Supply Current during "RAS - only" cycles		22		18	mA	4
$I_{I(L)}$	Input Leakage Current (any input)		5		5	μA	6
$I_{O(L)}$	Output Leakage Current		10		10	μA	7,8
V_{OH}	Output Logic 1 Voltage @ $I_{OUT} = -5mA$	2.4		2.4		Volts	2
V_{OL}	Output Logic 0 Voltage @ $I_{OUT} = 2mA$		0.4		0.4	Volts	

NOTES

- All voltages referenced to V_{SS} . V_{BB} must be applied to and removed from the device within 5 seconds of V_{DD} .
- Output voltage will swing from V_{SS} to V_{CC} if $V_{CC} \leq V_{DD} - 4$ volts. If $V_{CC} \geq V_{DD} - 4$ volts, the output will swing from V_{SS} to a voltage somewhat less than V_{DD} .
- Device speed is not guaranteed at input voltages greater than TTL levels (0 to 5V).
- Current is proportional to cycle rate; maximum current is measured at the fastest cycle rate.
- I_{CC} depends upon output loading. The V_{CC} supply is connected to the output buffer only.
- All device pins at 0 volts except V_{BB} which is at -5 volts and the pin under test which is at $+10$ volts.
- Output is disabled (open-circuit); $RAS = V_{IL}$ and $\overline{CAS} = V_{IHC}$.
- $0V \leq V_{OUT} \leq +10V$.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (10, 15, 17)
 (0°C ≤ T_A ≤ 70°C) (V_{DD} = 12.0V ± 5%, V_{CC} = 5.0V ± 10%, V_{SS} = 0V, V_{BB} = -5.0V ± 10%)

PARAMETER		MK 4200-16		MK 4200-11		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t _{RC}	Random Read or Write Cycle Time	425		500		nsec	11
t _{RAC}	Access time from Row Address Strobe		300		350	nsec	11,13
t _{CAC}	Access Time from Column Address Strobe		165		200	nsec	12,13
t _{OFF}	Output Buffer Turn-Off Delay	0	80	0	100	nsec	
t _{RP}	Row Address Strobe Precharge Time	125		150		nsec	
t _{RAS}	Row Address Strobe Pulse Width	300	10,000	350	10,000	nsec	
t _{RCL}	Row To Column Strobe Lead Time	80	135	100	150	nsec	14
t _{CAS}	Column Address Strobe Pulse Width	165		200		nsec	12
t _{AS}	Address Set-Up Time	0		0		nsec	
t _{AH}	Address Hold Time	80		100		nsec	
t _{CH}	Chip Select Hold Time	100		100		nsec	
t _T	Rise and Fall Times	3	50	3	50	nsec	15
t _{RCS}	Read Command Set-Up Time	0		0		nsec	
t _{RCH}	Read Command Hold Time	0		0		nsec	
t _{WCH}	Write Command Hold Time	130		150		nsec	
t _{WP}	Write Command Pulse Width	130		150		nsec	
t _{CRL}	Column to Row Strobe Lead Time	-50	+50	-50	+50	nsec	
t _{CWL}	Write Command to Column Strobe Lead Time	130		150		nsec	
t _{DS}	Data In Set-Up Time	0		0		nsec	16
t _{DH}	Data In Hold Time	130		150		nsec	16
t _{RFSH}	Refresh Period		2		2	msec	
t _{MOD}	Modify Time		10		10	μsec	
t _{DOH}	Data Out Hold Time	10		10		μsec	

**DYNAMIC
RAMS**

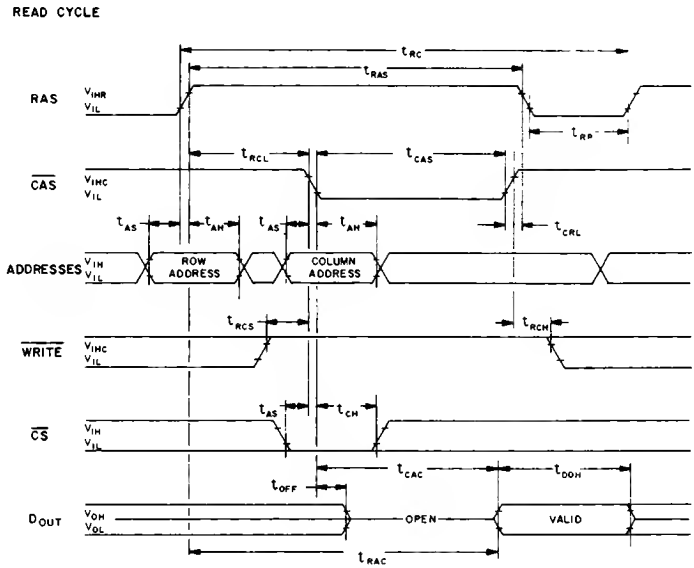
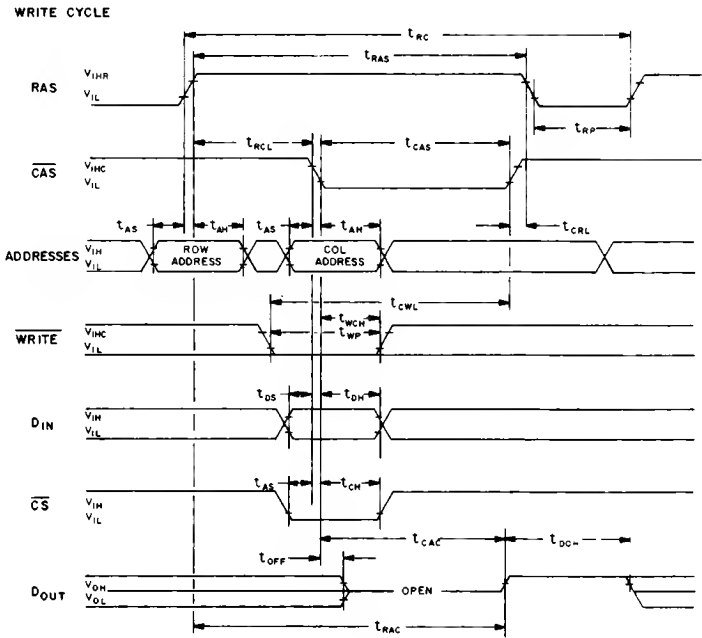
NOTES Continued

9. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I \Delta t}{\Delta V}$ with current equal to a constant 20mA.
10. A C measurements assume $t_T = 5ns$.
11. Assumes that $t_{RCL} + t_T \leq t_{RCL} (max)$.
12. Assumes that $t_{RCL} + t_T \geq t_{RCL} (max)$.
13. Measured with a load circuit equivalent to 1 TTL load and $C_L = 100pF$.
14. Operation within the $t_{RCL} (max)$ limit insures that $t_{RAC} (max)$ can be met. $t_{RCL} (max)$ is specified as a reference point only; if t_{RCL} is greater than the specified $t_{RCL} (max)$ limit, then access time is controlled exclusively by t_{CAC} and t_{RAS} . t_{RAC} and t_{RCL} will be longer by the amount $t_{RCL} + t_T$ exceeds $t_{RCL} (max)$.
15. V_{IHC} or V_{IHR} or V_{IH} and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IHR} or V_{IH} and V_{IL} .
16. These parameters are referenced to \overline{CAS} leading edge in random write cycles and to \overline{WRITE} leading edge in delayed write or read-modify-write cycles.
17. After the application of supply voltages or after extended periods of operation without clocks, the device must perform a minimum of one initialization cycles (any valid memory cycle containing both RAS and \overline{CAS}) prior to normal operation.

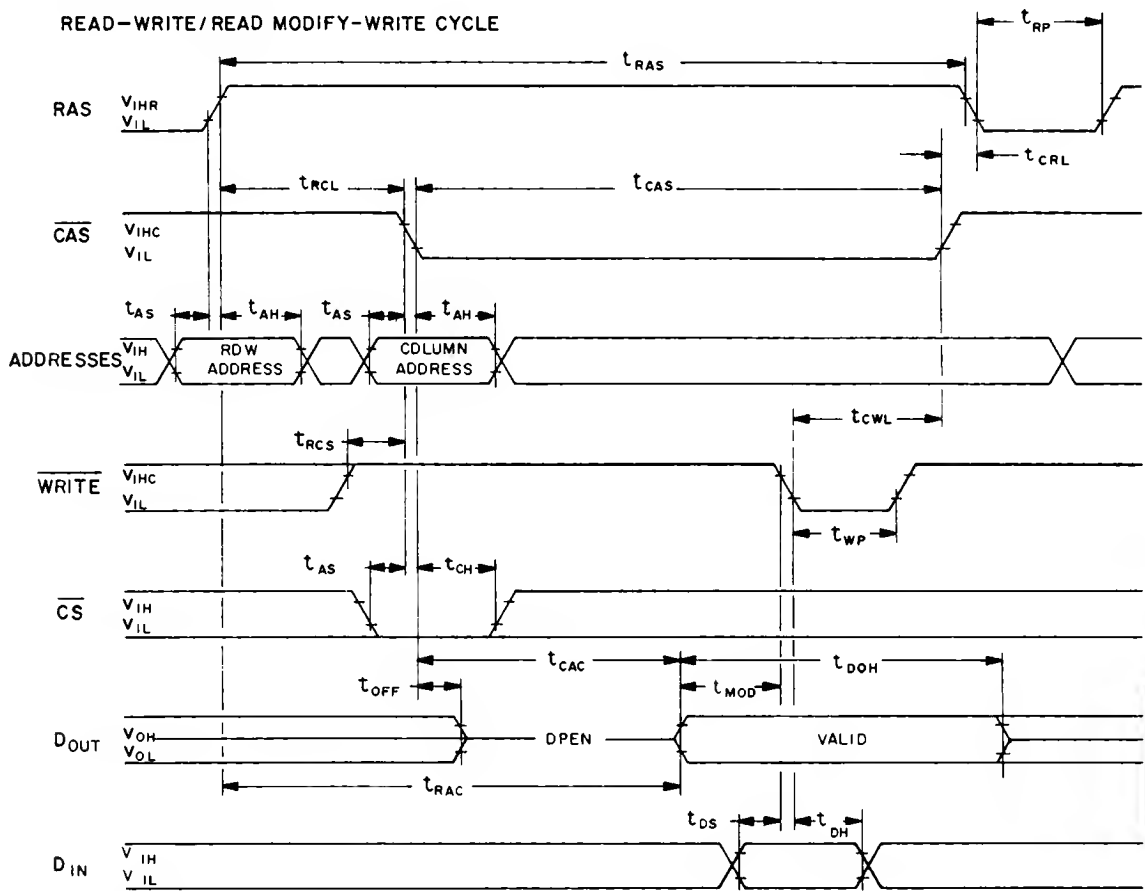
AC ELECTRICAL CHARACTERISTICS
 (0°C ≤ T_A ≤ + 70°C) (V_{DD} = 12.0V ± 5%, V_{CC} = 5.0V ± 10%, V_{SS} = 0V, V_{BB} = -5.0V ± 10%)

PARAMETER		TYP	MAX	UNITS	NOTES
C _{I1}	Input Capacitance (A ₀ – A ₅)	7	10	pF	9
C _{I2}	Input Capacitance (RAS, $\overline{\text{CAS}}$, D _{IN} , WRITE, CS)	5	7	pF	9
C _O	Output Capacitance (D _{OUT})	5	8	pF	7,9

TIMING WAVEFORMS

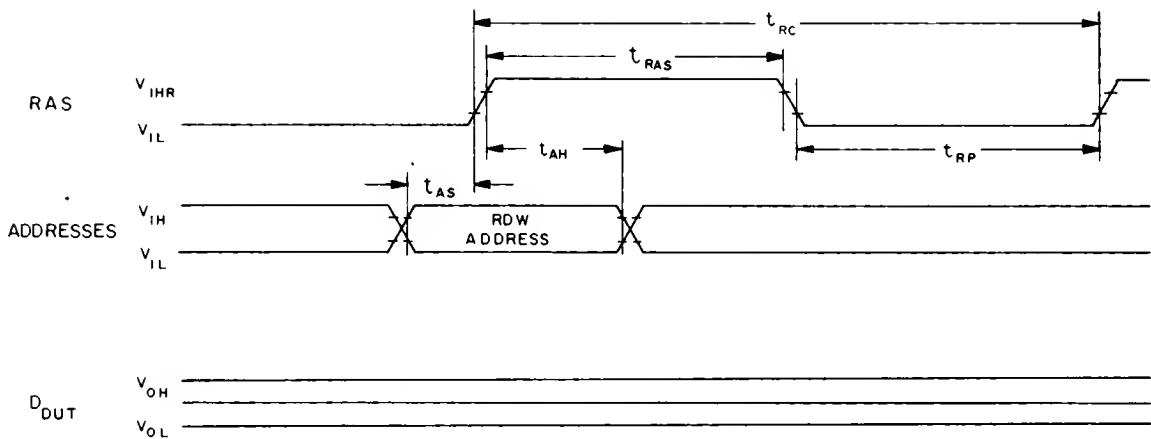


TIMING WAVEFORMS



DYNAMIC
RAMS

"RAS ONLY" REFRESH CYCLE



NOTE:

Prior to the first memory cycle following a period (beyond 2mS) of "RAS-only refresh, a memory cycle employing both RAS and CAS must be performed to insure proper device operation.

ADDRESSING

The 12 address bits required to decode one of the 4096 cell locations within the MK 4200 are multiplexed onto the 6 address inputs and latched into the on-chip address latches by externally applying a positive going MOS level clock and a negative going TTL level clock. The first clock, the Row Address Strobe (RAS), latches the 6 row address bits into the chip. The second clock, the Column Address Strobe (CAS), subsequently latches the 6 column address bits plus Chip Select (CS) into the chip. (Note that since the Chip Select signal is not required until CAS time, which is well into the memory cycle its decoding time does not add to system access or cycle time). Each of these signals, RAS and CAS, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the CAS clock sequence are inhibited until the occurrence of a delayed signal derived from the RAS clock chain. This "gated CAS" feature allows the CAS clock to be externally activated as soon as the Row Address Hold Time specification (t_{AH}) has been satisfied and the 6 address inputs have been changed from Row address to Column address information.

Note that $\overline{\text{CAS}}$ can be activated at any time after t_{AH} and it will have no effect on the worst case data access time (t_{RA}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing end points result from the internal gating of CAS which are called t_{RCL} (min) and t_{RCL} (max). No data storage or reading errors will result if CAS is applied to the MK 4200 at a point in time beyond the t_{RCL} (max) limit. However, access time will then be determined exclusively by the access time from CAS (t_{CAC}) rather than from RAS (t_{RA}), and access time from RAS will be lengthened by the amount that t_{RCL} exceeds the t_{RCL} (max) limit.

INPUT LEVELS

All inputs to the MK 4200 except address strobe (RAS) are TTL compatible. The RAS input has been specially designed so that very little steady state (DC) power is dissipated by the MK 4200 while in standby operation. In doing this, the RAS input requires a high level signal to activate the chip. The RAS input driver must be able to change the capacitance load of the RAS input from within 8 volt at V_{SS} (0V) to within 1 volt of V_{DD} (+12).

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of WRITE and CAS while RAS is active. The later of the signals (WRITE or CAS) to make its negative transition is the strobe for the Data In register. This permits several options in the write cycle timing. In a write cycle, if the WRITE input is brought low prior to CAS, the Data In is strobed by CAS, and the set-up and hold times are referenced to CAS. If the data input is not available at CAS time or if it is desired that the cycle be a read-write or read-modify-write cycle, the WRITE signal must be delayed until after CAS. In this "delayed write cycle" the data input set-up and hold times are referenced to the

negative edge of WRITE rather than to $\overline{\text{CAS}}$.

(To illustrate this feature, Data In is referenced to WRITE in the timing diagram depicting the read-modify-write cycle while the "early write" cycle diagram shows Data In referenced to CAS). Note that if the chip is unselected ($\overline{\text{CS}}$ high at CAS time) WRITE commands are not executed and, consequently, data stored in the memory is unaffected.

Data is retrieved from the memory in a read cycle by maintaining WRITE in the inactive or high state throughout the portion of the memory cycle in which CAS is active. Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT LATCH

Any change in the condition of the Data Out Latch is initiated by the CAS signal. The output buffer is not affected by memory (refresh) cycles in which only the RAS signal is applied to the MK 4200. Whenever CAS makes a negative transition, the output will go unconditionally open-circuited, independent of the state of any other input to the chip. If the cycle in progress is a read, read-modify-write, or a delayed write cycle and the chip is selected, then the output latch and buffer will again go active and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle in progress is a write cycle (WRITE active low before CAS goes low) and the chip is selected, then at access time the output latch and buffer will contain a logic 1. Once having gone active, the output will remain valid until the MK 4200 receives the next CAS negative edge. Intervening refresh cycles in which a RAS is received (but no CAS) will not cause valid data to be affected. Conversely, the output will assume the open-circuit state during any cycle in which the MK 4200 receives a CAS but no RAS signal (regardless of the state of any other inputs). The output will also assume the open-circuit state in normal cycles (in which both RAS and CAS signals occur) if the chip is unselected.

The three-state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The effective resistance to V_{CC} (logic 1 state) is 500 Ω maximum and 150 Ω typically. The resistance to V_{SS} (logic 0 state) is 200 Ω maximum and 100 Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4200 refresh operation. This allows all system logic except the RAS/CAS timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses within each 2 millisecond time interval. Any cycle in which a RAS signal occurs accomplishes a refresh operation. A read cycle will refresh the selected row, regardless of the Chip Select ($\overline{\text{CS}}$) input. A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to

prevent writing data into the selected cell.

For standby operation, a "RAS-only" cycle can be employed to refresh the MK 4200. However, if "RAS-only" refresh cycles (where RAS is the only signal applied to the chip) are continued for extended periods, the output buffer may eventually lose proper data and go open-circuit. Prior to the first memory cycle following a period (beyond 2ms) of "RAS-only" refresh, a memory cycle employing both RAS and CAS must be performed to precharge the internal circuitry. This "dummy cycle" allows the output buffer to regain activity and enables the device to perform a read or write cycle upon command.

POWER DISSIPATION/STANDBY MODE

Most of the circuitry used in the MK 4200 is dynamic and most of the power drawn is the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency rather than active duty cycle. Typically, the power is 120 mW at a 1 μ sec cycle rate for the MK 4200 with a maximum power of less than 450 mW at 375 nsec cycle time. To minimize the overall system power, the Row Address Strobe (RAS) should be decoded and supplied to only the selected chips. The CAS must be supplied to all chips (to turn off the unselected output). Those chips that did not receive a RAS, however, will not dissipate any power on the CAS edges, except for that required to turn off the outputs. If the RAS signal is decoded and supplied only to the selected chips, then the Chip Select (CS) input of all chips can be at a logic 0. The chips that receive a CAS but no RAS will be unselected (output open-circuited) regardless of the Chip Select input. For refresh cycles, however, either the CS input of all chips must be high or the CAS input must be

held high to prevent several "wire-ORed" outputs from turning on with opposing force.

The current waveforms for the current drawn from the VDD and VBB supplies are shown in Figure A. Since the current is pulsed, proper power distribution and bypassing techniques are required to maintain system power supply noise levels at an acceptable level. Low inductance supply lines for VDD and VSS are desirable. One 0.01 microfarad, low inductance, bypass capacitor per two MK 4200 devices and one 6.8 microfarad electrolytic capacitor per eight MK 4200 devices on each of the VDD and VBB supply lines is desirable.

POWER-UP

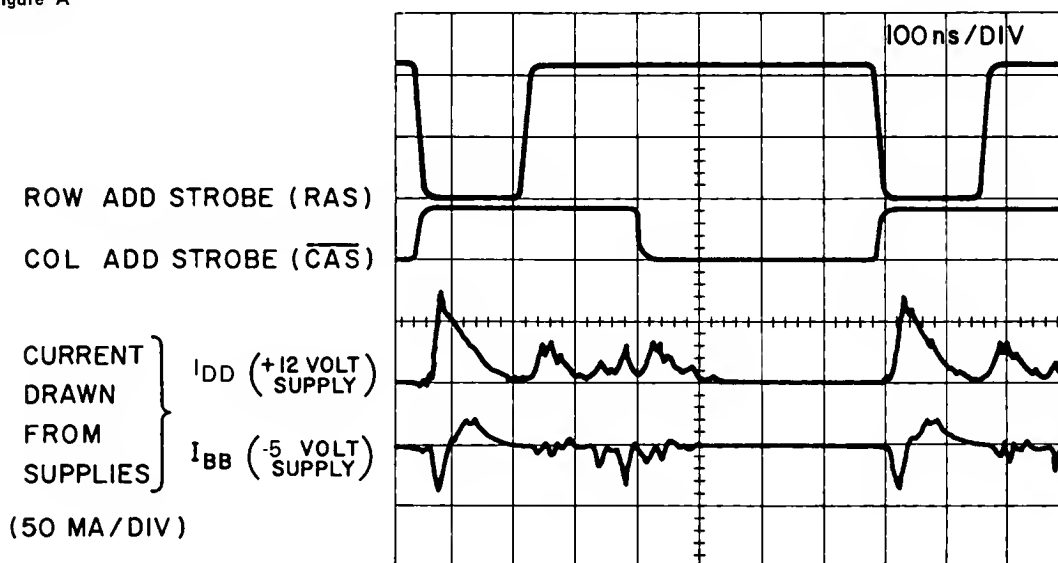
Under normal operating conditions the MK 4200 requires no particular power-up sequence. However, in order to achieve the most reliable performance from the MK 4200, proper consideration should be given to the VBB/VDD power supply relationship. The VBB supply is an extremely important "protective voltage" since it performs two essential functions within the device. It establishes proper junction isolation and sets field-effect thresholds, both thin field and thick field. Misapplication of VBB or device operation without the VBB supply can affect long term device reliability. For optimum reliability performance from the MK 4200, it is suggested that measures be taken to not have VDD (+12V) applied to the device for over five (5) seconds without the application of VBB (-5V).

After power is applied to the device, the MK 4200 requires at least one memory cycle (RAS/CAS) before proper device operation is achieved. A normal 64 cycle refresh with both RAS and CAS is adequate for this purpose.

DYNAMIC
RAMS

POWER SUPPLY CURRENT WAVEFORMS

Figure A



MOSTEK®

16,384 X 1-BIT DYNAMIC RAM

MK4116(J/N/E)-2/3

FEATURES

- Recognized industry standard 16-pin configuration from MOSTEK
- 150ns access time, 320ns cycle (MK 4116-2)
200ns access time, 375ns cycle (MK 4116-3)
- $\pm 10\%$ tolerance on all power supplies (+12V, $\pm 5V$)
- Low power: 462mW active, 20mW standby (max)
- Output data controlled by \overline{CAS} and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- Common I/O capability using "early write" operation
- Read-Modify-Write, \overline{RAS} -only refresh, and Page-mode capability
- All inputs TTL compatible, low capacitance, and protected against static charge
- 128 refresh cycles
- ECL compatible on VBB power supply (-5.7V)

DESCRIPTION

The MK 4116 is a new generation MOS dynamic random access memory circuit organized as 16,384 words by 1 bit. As a state-of-the-art MOS memory device, the MK 4116 (16K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving performance levels in speed and power previously seen only in MOSTEK's high performance MK 4027 (4K RAM).

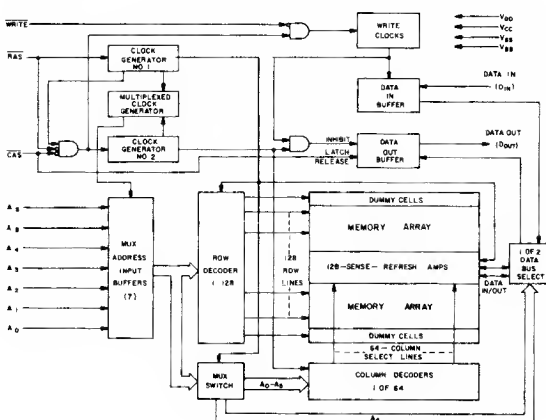
The technology used to fabricate the MK 4116 is MOSTEK's double-poly, N-channel silicon gate, POLY II[®] process. This process, coupled with the use of a single transistor dynamic storage cell, provides the maximum possible circuit density and reliability, while maintaining high performance

capability. The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the MK 4116 a truly superior RAM product.

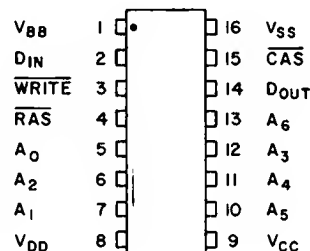
Multiplexed address inputs (a feature pioneered by MOSTEK for its 4K RAMs) permits the MK 4116 to be packaged in a standard 16-pin DIP. This recognized industry standard package configuration, while compatible with widely available automated testing and insertion equipment, provides highest possible system bit densities and simplifies system upgrade from 4K to 16K RAMs for new generation applications. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

DYNAMIC
RAMS

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A ₀ -A ₆	ADDRESS INPUTS	WRITE	READ/WRITE INPUT
\overline{CAS}	COLUMN ADDRESS STROBE	V _{BB}	POWER (-5V)
D _{IN}	DATA IN	V _{CC}	POWER (+5V)
D _{OUT}	DATA OUT	V _{DD}	POWER (+12V)
RAS	ROW ADDRESS STROBE	V _{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V _{BB}	−0.5V to +20V
Voltage on V _{DD} , V _{CC} supplies relative to V _{SS}	−1.0V to +15.0V
V _{BB} −V _{SS} (V _{DD} −V _{SS} > 0V)	0V
Operating temperature, T _A (Ambient)	0°C to + 70°C
Storage temperature (Ambient) Ceramic	−55°C to + 150°C
Storage temperature, (Ambient) Plastic	−55°C to +125°C
Short circuit output current	50mA
Power dissipation	1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

(0°C ≤ T_A ≤ 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V _{DD}	10.8	12.0	13.2	Volts	2
	V _{CC}	4.5	5.0	5.5	Volts	2,3
	V _{SS}	0	0	0	Volts	2
	V _{BB}	−4.5	−5.0	−5.7	Volts	2
Input High (Logic 1) Voltage, <u>RAS</u> , <u>CAS</u> , <u>WRITE</u>	V _{IHC}	2.4	—	7.0	Volts	2
Input High (Logic 1) Voltage, all inputs except <u>RAS</u> , <u>CAS</u> , <u>WRITE</u>	V _{IH}	2.2	—	7.0	Volts	2
Input Low (Logic 0) Voltage, all inputs	V _{IL}	−1.0	—	.8	Volts	2

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ± 10%; −5.7V ≤ V_{BB} ≤ −4.5V; V_{SS} = 0V)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT Average power supply operating current (<u>RAS</u> , <u>CAS</u> cycling; t _{RC} = t _{RC} Min)	I _{DD1}		35	mA	4
	I _{CC1}				5
	I _{BB1}		200	μA	
STANDBY CURRENT Power supply standby current (<u>RAS</u> = V _{IHC} , D _{OUT} = High Impedance)	I _{DD2}	−10	1.5	mA	
	I _{CC2}		10	μA	
	I _{BB2}		100	μA	
REFRESH CURRENT Average power supply current, refresh mode (<u>RAS</u> cycling, <u>CAS</u> = V _{IHC} ; t _{RC} = t _{RC} Min)	I _{DD3}	−10	25	mA	4
	I _{CC3}		10	μA	
	I _{BB3}		200	μA	
PAGE MODE CURRENT Average power supply current, page-mode operation (<u>RAS</u> = V _{IL} , <u>CAS</u> cycling; t _{PC} = t _{PC} Min)	I _{DD4}		27	mA	4
	I _{CC4}				5
	I _{BB4}		200	μA	
INPUT LEAKAGE Input leakage current, any input (V _{BB} = −5V, 0V ≤ V _{IN} ≤ +7.0V, all other pins not under test = 0 volts)	I _{I(L)}	−10	10	μA	
OUTPUT LEAKAGE Output leakage current (D _{OUT} is disabled, 0V ≤ V _{OUT} ≤ +5.5V)	I _{O(L)}	−10	10	μA	
OUTPUT LEVELS Output high (Logic 1) voltage (I _{OUT} = −5mA)	V _{OH}	2.4		Volts	3
	V _{OL}		0.4	Volts	

NOTES:

1. T_A is specified here for operation at frequencies to t_{RC} ≥ t_{RC} (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met. See figure 1 for derating curve.
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby

mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

4. I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. See figures 2,3, and 4 for I_{DD} limits at other cycle rates.
5. I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135 Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (6,7,8)
(0°C ≤ T_A ≤ 70°C)¹ (V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ± 10%, V_{SS} = 0V, V_{BB} = -5.7V ≤ V_{BB} ≤ -4.5V)

PARAMETER	SYMBOL	MK 4116-2		MK 4116-3		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Random read or write cycle time	t _{RC}	320		375		ns	9
Read-write cycle time	t _{RWC}	320		375		ns	9
Read modify write cycle time	t _{RMW}	320		405		ns	9
Page mode cycle time	t _{PC}	170		225		ns	9
Access time from RAS	t _{RAC}		150		200	ns	10,12
Access time from CAS	t _{CAC}		100		135	ns	11,12
Output buffer turn-off delay	t _{OFF}	0	40	0	50	ns	13
Transition time (rise and fall)	t _T	3	35	3	50	ns	8
RAS precharge time	t _{RP}	100		120		ns	
RAS pulse width	t _{RAS}	150	10,000	200	10,000	ns	
RAS hold time	t _{RSH}	100		135		ns	
CAS hold time	t _{CSH}	150		200		ns	
CAS pulse width	t _{CAS}	100	10,000	135	10,000	ns	
RAS to CAS delay time	t _{RCD}	20	50	25	65	ns	14
CAS to RAS precharge time	t _{CRP}	-20		-20		ns	
Row Address set-up time	t _{ASR}	0		0		ns	
Row Address hold time	t _{RAH}	20		25		ns	
Column Address set-up time	t _{ASC}	-10		-10		ns	
Column Address hold time	t _{CAH}	45		55		ns	
Column Address hold time referenced to RAS	t _{AR}	95		120		ns	
Read command set-up time	t _{RCS}	0		0		ns	
Read command hold time	t _{RCH}	0		0		ns	
Write command hold time	t _{WCH}	45		55		ns	
Write command hold time referenced to RAS	t _{WCR}	95		120		ns	
Write command pulse width	t _{WP}	45		55		ns	
Write command to RAS lead time	t _{RWL}	50		70		ns	
Write command to CAS lead time	t _{CWL}	50		70		ns	
Data-in set-up time	t _{DS}	0		0		ns	15
Data-in hold time	t _{DH}	45		55		ns	15
Data-in hold time referenced to RAS	t _{DHR}	95		120		ns	
CAS precharge time (for page-mode cycle only)	t _{CP}	60		80		ns	
Refresh period	t _{REF}		2		2	ms	
WRITE command set-up time	t _{WCS}	-20		-20		ns	16
CAS to WRITE delay	t _{CWD}	60		80		ns	16
RAS to WRITE delay	t _{RWD}	110		145		ns	16

NOTES (Continued)

6. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
7. AC measurements assume t_T = 5ns.
8. VIH (min) or VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Also transition times are measured between VIH or VIH and VIL.
9. The specifications for t_{RC} (min) t_{RMW} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
10. Assumes that t_{RCD} ≤ t_{RCD} (Max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
11. Assumes that t_{RCD} (max).
12. Measured with a load equivalent to 2 TTL loads and 100pF.
13. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

14. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
15. These parameters are referenced to CAS leading edge in early write cycles and to WRITE leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are restrictive operating parameters in read write and read modify write cycles only. If t_{WCS} ≥ t_{WCS} (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If t_{CWD} ≥ t_{CWD} (min) and t_{RWD} ≥ t_{RWD} (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
17. Effective capacitance calculated from the equation $C = \frac{1}{\Delta V} \Delta V$ with $\Delta = 3$ volts and power supplies at nominal levels.
18. CAS = VIH to disable DOUT.

AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{DD} = 12.0V ± 10%; V_{SS} = 0V; V_{BB} = -5.7V ≤ V_{BB} ≤ -4.5V)

PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance (A ₀ –A ₆), D _{IN}	C _{I1}	4	5	pF	17
Input Capacitance \overline{RAS} , \overline{CAS} , \overline{WRITE}	C _{I2}	8	10	pF	17
Output Capacitance (D _{OUT})	C _O	5	7	pF	17,18

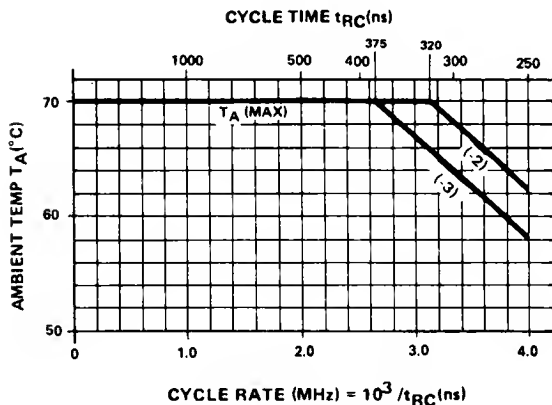


Fig. 1 Maximum ambient temperature versus cycle rate for extended frequency operation. T_A (max) for operation at cycling rates greater than 2.66 MHz ($t_{CYC} < 375$ ns) is determined by T_A (max) °C = 70 – 9.0 × (cycle rate MHz – 2.66) for -3. T_A (max) °C = 70 – 9.0 × cycle rate MHz – 3.125 MHz for -2 only.

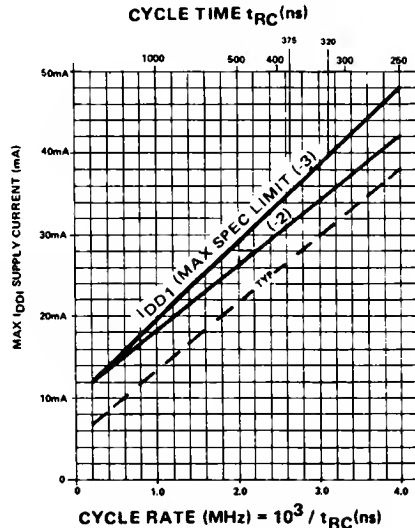


Fig. 2 Maximum I_{DD1} versus cycle rate for device operation at extended frequencies. I_{DD1} (max) curve is defined by the equation:

$$I_{DD1} \text{ (max) mA} = 10 + 9.4 \times \text{cycle rate [MHz]} \text{ for } -3$$

$$I_{DD1} \text{ (max) mA} = 10 + 8.0 \times \text{cycle rate [MHz]} \text{ for } -2$$

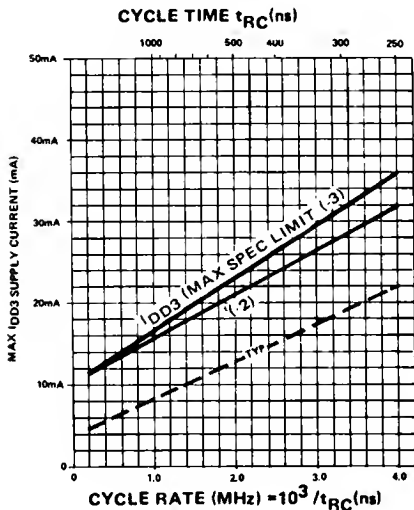


Fig. 3 Maximum I_{DD3} versus cycle rate for device operation at extended frequencies. I_{DD3} (max) curve is defined by the equation:

$$I_{DD3} \text{ (max) mA} = 10 + 6.5 \times \text{cycle rate [MHz]} \text{ for } -3$$

$$I_{DD3} \text{ (max) mA} = 10 + 5.5 \times \text{cycle rate [MHz]} \text{ for } -2$$

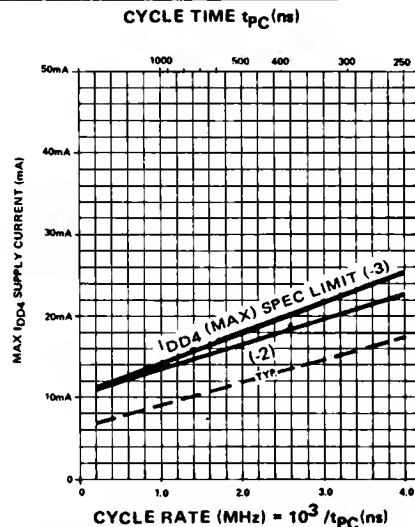
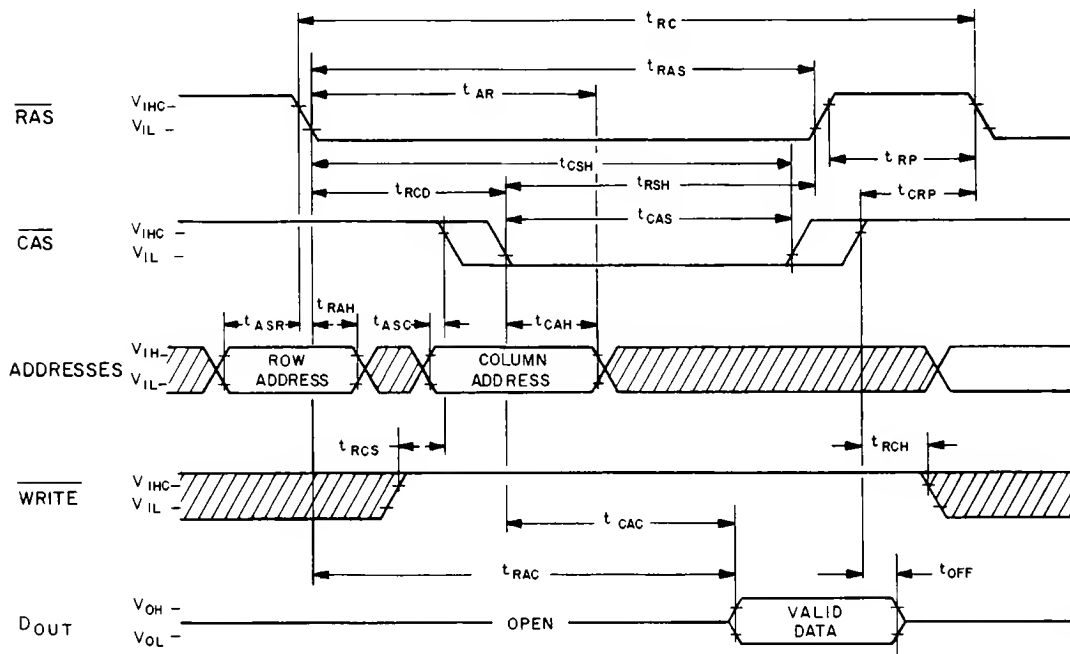


Fig. 4 Maximum I_{DD4} versus cycle rate for device operation in page mode. I_{DD4} (max) curve is defined by the equation:

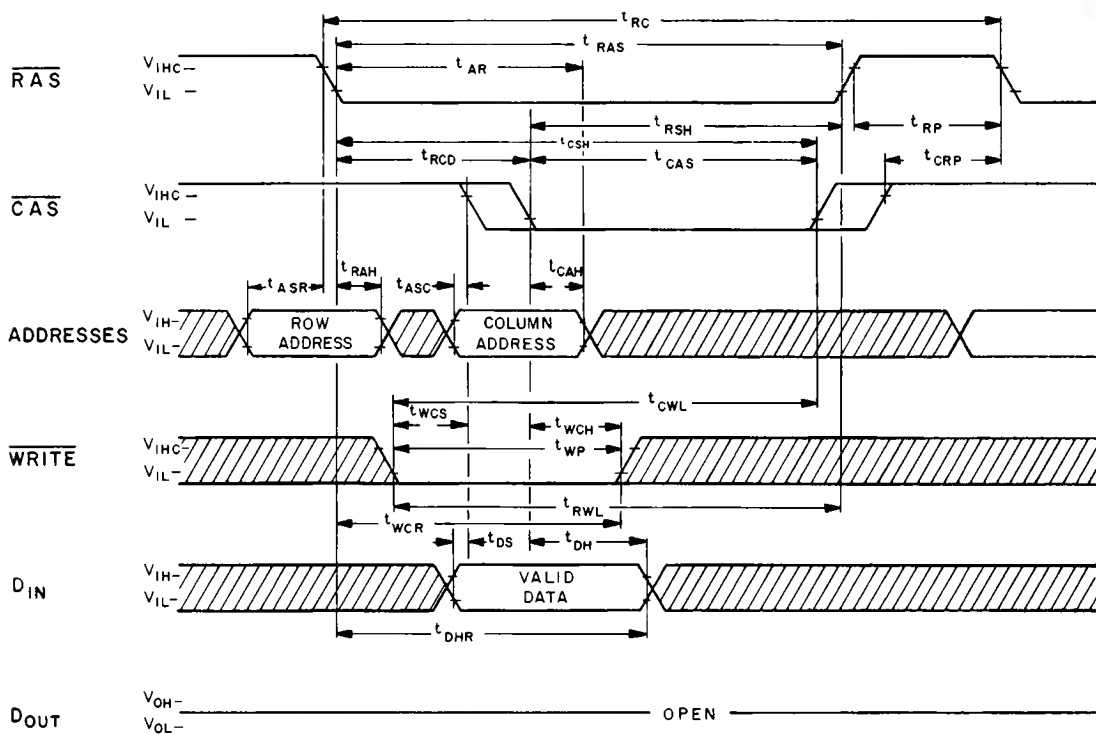
$$I_{DD4} \text{ (max) mA} = 10 + 3.75 \times \text{cycle rate [MHz]} \text{ for } -3$$

$$I_{DD4} \text{ (max) mA} = 10 + 3.2 \times \text{cycle rate [MHz]} \text{ for } -2$$

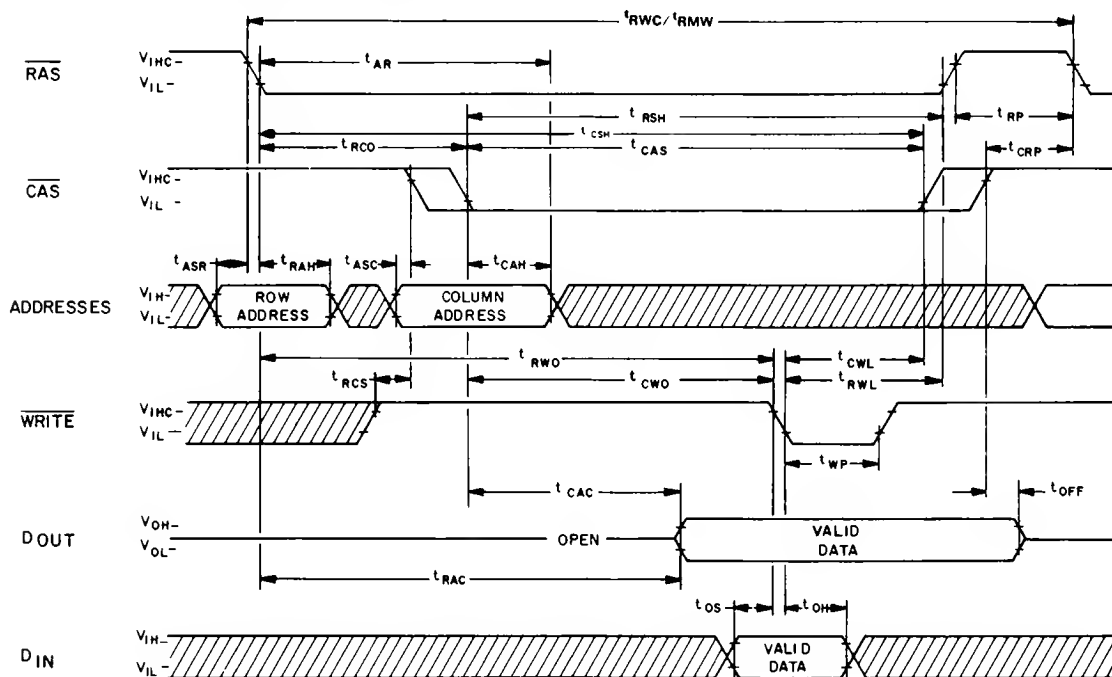
READ CYCLE



WRITE CYCLE (EARLY WRITE)

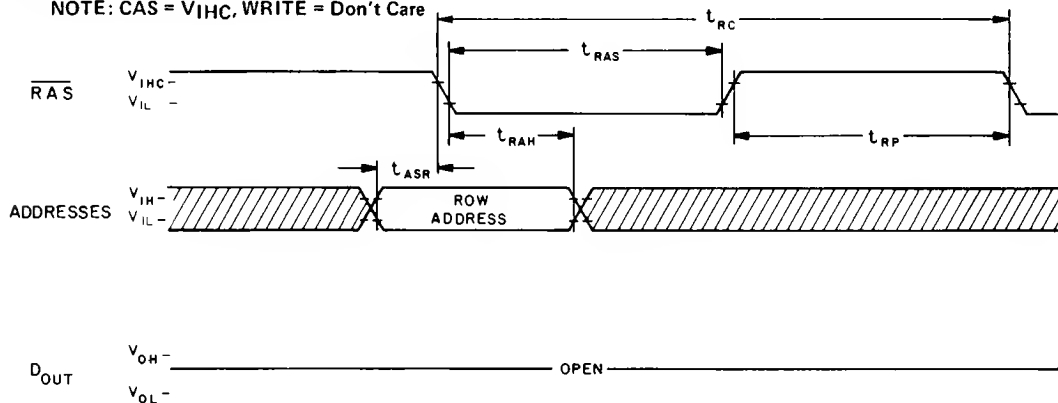


READ-WRITE/READ-MODIFY-WRITE CYCLE



"RAS-ONLY" REFRESH CYCLE

NOTE: $\overline{CAS} = V_{IH}$, WRITE = Don't Care



[illegible]

PAGE MODE WRITE CYCLE

The diagram illustrates the timing for a Page Mode Write Cycle. It shows five signal traces: $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, ADDRESSES, $\overline{\text{WRITE}}$, and D_{IN} . The $\overline{\text{RAS}}$ signal is active low and defines the overall write period t_{RAS} . The $\overline{\text{CAS}}$ signal is also active low and defines the column access time t_{CAS} . The ADDRESSES signal shows the sequence of Row Address (ROW ADD) and Column Address (COL ADD) pulses. The $\overline{\text{WRITE}}$ signal is active low and indicates the write operation. The D_{IN} signal shows the data being written, with valid data periods indicated by shaded boxes. Various timing parameters are labeled, including t_{AR} , t_{CSH} , t_{PC} , t_{RCD} , t_{CAS} , t_{CP} , t_{RSH} , t_{RP} , t_{CRP} , t_{RAH} , t_{CAH} , t_{ASC} , t_{ASR} , t_{WCH} , t_{CWL} , t_{WCR} , t_{WP} , t_{DS} , t_{DH} , t_{DHR} , t_{RWL} , and t_{DHR} .

DESCRIPTION (continued)

System oriented features include $\pm 10\%$ tolerance on all power supplies, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs (a common cause of soft errors), on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MK 4116 also incorporates several flexible timing/operating modes. In addition to the usual read, write, and read-modify-write cycles, the MK 4116 is capable of delayed write cycles, page-mode operation and RAS-only refresh. Proper control of the clock inputs (RAS, CAS and WRITE) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

ADDRESSING

The 14 address bits required to decode 1 of the 16,384 cell locations within the MK 4116 are multiplexed onto the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, the Row Address Strobe (RAS), latches the 7 row address bits into the chip. The second clock, the Column Address Strobe (CAS), subsequently latches the 7 column address bits into the chip. Each of these signals, RAS and CAS, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the CAS clock sequence are inhibited until the occurrence of a delayed signal derived from the RAS clock chain. This "gated CAS" feature allows the CAS clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Note that \overline{CAS} can be activated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing end-points result from the internal gating of CAS which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if CAS is applied to the MK 4116 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from CAS (t_{CAC}) rather than from RAS (t_{RAC}), and access time from RAS will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of WRITE and CAS while RAS is active. The later of the signals (WRITE or CAS) to make its negative transition is the strobe for the Data In (DIN) register. This permits several options in the write cycle timing. In a write cycle, if the WRITE input is brought low (active)

prior to \overline{CAS} , the DIN is strobed by \overline{CAS} and the set-up and hold times are referenced to CAS. If the input data is not available at CAS time or if it is desired that the cycle be a read-write cycle, the WRITE signal will be delayed until after CAS has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of WRITE rather than CAS. (To illustrate this feature, DIN is referenced to WRITE in the timing diagrams depicting the read-write and page-mode write cycles while the "early write" cycle diagram shows DIN referenced to CAS).

Data is retrieved from the memory in a read cycle by maintaining WRITE in the inactive or high state throughout the portion of the memory cycle in which CAS is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (DOUT) of the MK 4116 is the high impedance (open-circuit) state. That is to say, anytime CAS is at a high level, the DOUT pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. DOUT will remain valid from access time until CAS is taken back to the inactive (high level) condition.

If the memory cycle in progress is a read, read-modify write, or a delayed write cycle, then the data output will go from the high impedance state to the active condition, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. Once having gone active, the output will remain valid until CAS is taken to the precharge (logic 1) state, whether or not RAS goes into precharge.

If the cycle in progress is an "early-write" cycle (WRITE active before CAS goes active), then the output pin will maintain the high impedance state throughout the entire cycle. Note that with this type of output configuration, the user is given full control of the DOUT pin simply by controlling the placement of WRITE command during a write cycle, and the pulse width of the Column Address Strobe during read operations. Note also that even though data is not latched at the output, data can remain valid from access time until the beginning of a subsequent cycle without paying any penalty in overall memory cycle time (stretching the cycle).

This type of output operation results in some very significant system implications.

Common I/O Operation — If all write operations are handled in the "early write" mode, then DIN can be connected directly to DOUT for a common I/O data bus.

Data Output Control — DOUT will remain valid during a read cycle from t_{CAC} until CAS goes back to a high level (precharge), allowing data to be valid from one cycle up until a new memory cycle begins with no penalty in cycle time. This also makes the RAS/CAS clock timing relationship very flexible.

Two Methods of Chip Selection — Since DOUT

is not latched, $\overline{\text{CAS}}$ is not required to turn off the outputs of unselected memory devices in a matrix. This means that both $\overline{\text{CAS}}$ and/or $\overline{\text{RAS}}$ can be decoded for chip selection. If both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are decoded, then a two dimensional (X,Y) chip select array can be realized.

Extended Page Boundary — Page-mode operation allows for successive memory cycles at multiple column locations of the same row address. By decoding $\overline{\text{CAS}}$ as a page cycle select signal, the page boundary can be extended beyond the 128 column locations in a single chip. (See page-mode operation).

OUTPUT INTERFACE CHARACTERISTICS

The three state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The effective resistance to V_{CC} (logic 1 state) is $420\ \Omega$ maximum and $135\ \Omega$ typically. The resistance to V_{SS} (logic 0 state) is $95\ \Omega$ maximum and $35\ \Omega$ typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4116 refresh operation. This allows all system logic except the $\overline{\text{RAS}}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

PAGE MODE OPERATION

The "Page Mode" feature of the MK 4116 allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{\text{RAS}}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "page-mode" of operation will not dissipate the power associated with the negative going edge of $\overline{\text{RAS}}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

The page boundary of a single MK 4116 is limited to the 128 column locations determined by all combinations of the 7 column address bits. However, in system applications which utilize more than 16,384 data words, (more than one 16K memory block), the page boundary can be extended by using $\overline{\text{CAS}}$ rather than $\overline{\text{RAS}}$ as the chip select signal. $\overline{\text{RAS}}$ is applied to all devices to latch the row address into each device and then $\overline{\text{CAS}}$ is decoded and serves as a page cycle select signal. Only those devices which receive both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals will execute a read or write cycle.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "RAS-only" cycles. RAS-only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the IDD3 specification.

POWER CONSIDERATIONS

Most of the circuitry used in the MK 4116 is dynamic and most of the power drawn is the result of an address strobe edge. Consequently, the dynamic power is primarily a function of operating frequency rather than active duty cycle (refer to the MK 4116 current waveforms in figure 5). This current characteristic of the MK 4116 precludes inadvertent burn out of the device in the event that the clock inputs become shorted to ground due to system malfunction.

Although no particular power supply noise restriction exists other than the supply voltages remain within the specified tolerance limits, adequate decoupling should be provided to suppress high frequency noise resulting from the transient current of the device. This insures optimum system performance and reliability. Bulk capacitance requirements are minimal since the MK 4116 draws very little steady state (DC) current.

In system applications requiring lower power dissipation, the operating frequency (cycle rate) of the MK 4116 can be reduced and the (guaranteed maximum) average power dissipation of the device will be lowered in accordance with the IDD1 (max) spec limit curve illustrated in figure 2. **NOTE:** The MK 4116 family is guaranteed to have a maximum IDD1 requirement of 35mA @ 375ns cycle (320ns cycle for the -2) with an ambient temperature range from 0° to 70°C . A lower operating frequency, for example 1 microsecond cycle, results in a reduced maximum IDD1 requirement of under 20mA with an ambient temperature range from 0° to 70°C .

It is possible the MK4116 family (-2 and 3 speed selections for example) at frequencies higher than specified, provided all AC operating parameters are met. Operation at shorter cycle times ($< \text{t}_{RC}$ min) results in higher power dissipation and, therefore, a reduction in ambient temperature is required. Refer to Figure 1 for derating curve.

NOTE: Additional power supply tolerance has been included on the V_{BB} supply to allow direct interface capability with both -5V systems -5.2V ECL systems.

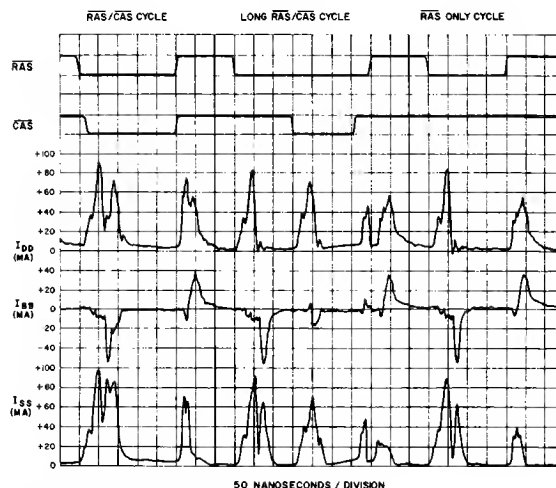


Fig. 5 Typical Current Waveforms

Although $\overline{\text{RAS}}$ and/or $\overline{\text{CAS}}$ can be decoded and used as a chip select signal for the MK 4116, overall system power is minimized if the Row Address Strobe ($\overline{\text{RAS}}$) is used for this purpose. All unselected devices (those which do not receive a $\overline{\text{RAS}}$) will remain in a low power (standby) mode regardless of the state of $\overline{\text{CAS}}$.

POWER UP

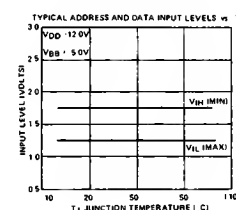
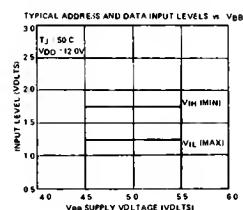
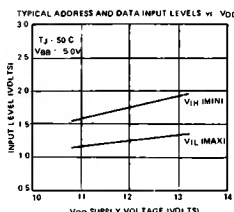
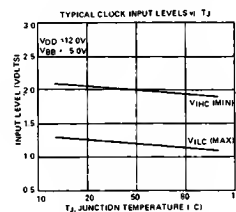
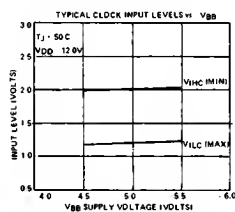
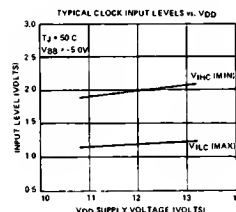
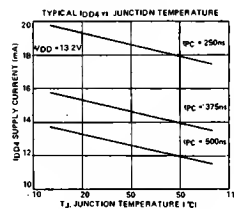
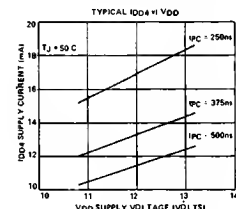
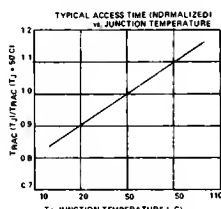
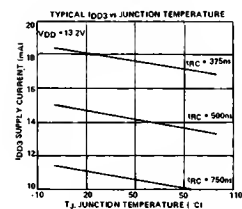
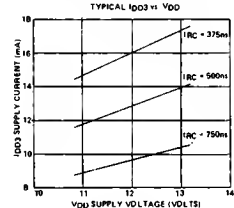
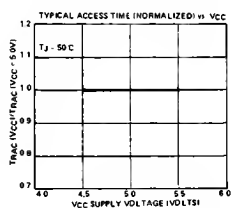
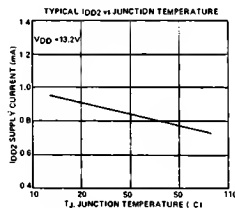
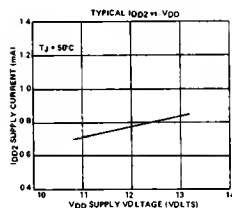
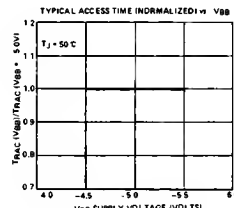
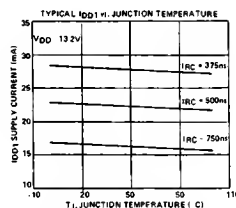
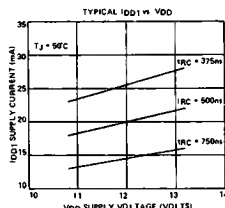
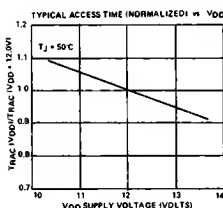
The MK 4116 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, MOSTEK recommends sequencing of power supplies

such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD} .

Under system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ to the inactive state (high level).

After power is applied to the device, the MK 4116 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

TYPICAL CHARACTERISTICS



FEATURES

- Recognized industry standard 16-pin configuration from MOSTEK
- 250ns access time, 410ns cycle
- $\pm 10\%$ tolerance on all power supplies (+12V, $\pm 5V$)
- Low power: 462mW active, 20mW standby (max)
- Output data controlled by \overline{CAS} and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary

DESCRIPTION

The MK 4116 is a new generation MOS dynamic random access memory circuit organized as 16,384 words by 1 bit. As a state-of-the-art MOS memory device, the MK 4116 (16K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving performance levels in speed and power previously seen only in MOSTEK's high performance MK 4027 (4K RAM).

The technology used to fabricate the MK 4116 is MOSTEK's double-poly, N-channel silicon gate, POLY II® process. This process, coupled with the use of a single transistor dynamic storage cell, provides the maximum possible circuit density and reliability, while maintaining high performance

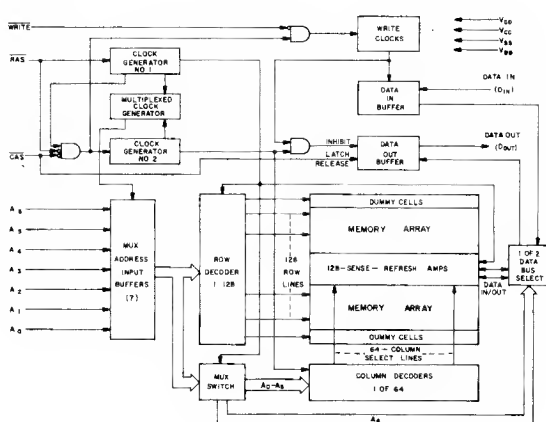
- Common I/O capability using "early write" operation
- Read-Modify-Write, \overline{RAS} -only refresh, and Page-mode capability
- All inputs TTL compatible, low capacitance, and protected against static charge
- 128 refresh cycles (2 msec refresh interval)
- ECL compatible on V_{BB} power supply (-5.7V)

capability. The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the MK 4116 a truly superior RAM product.

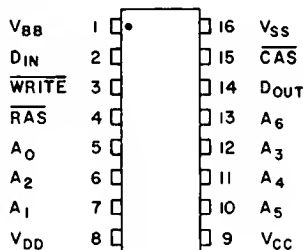
Multiplexed address inputs (a feature pioneered by MOSTEK for its 4K RAMs) permits the MK 4116 to be packaged in a standard 16-pin DIP. This recognized industry standard package configuration, while compatible with widely available automated testing and insertion equipment, provides highest possible system bit densities and simplifies system upgrade from 4K to 16K RAMs for new generation applications. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

DYNAMIC RAMS

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN FUNCTIONS

A_0-A_6	Address Inputs	WRITE	Read/Write Input
CAS	Column Address	V_{BB}	Power (-5V)
	Strobe	V_{CC}	Power (+5V)
DIN	Data In	V_{DD}	Power (+12V)
DOUT	Data Out	V_{SS}	Ground
RAS	Row Address Strobe		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB}	-0.5V to +20V
Voltage on V_{DD} , V_{CC} supplies relative to V_{SS}	-1.0V to +15.0V
$V_{BB}-V_{SS}$ ($V_{DD}-V_{SS}>0V$)	0V
Operating temperature, T_A (Ambient)	0°C to + 70°C
Storage temperature (Ambient) (Ceramic)	-65°C to + 150°C
Storage temperature (Ambient) (Plastic)	-55°C to + 125°C
Short circuit output current	50mA
Power dissipation	1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)¹

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	10.8	12.0	13.2	Volts	1
	V_{CC}	4.5	5.0	5.5	Volts	1,2
	V_{SS}	0	0	0	Volts	1
	V_{BB}	-4.5	-5.0	-5.7	Volts	1
Input High (Logic 1) Voltage, \overline{RAS} , \overline{CAS} , \overline{WRITE}	V_{IHC}	2.4	—	7.0	Volts	1
Input High (Logic 1) Voltage, all inputs except \overline{RAS} , \overline{CAS} , \overline{WRITE}	V_{IH}	2.2	—	7.0	Volts	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	—	.8	Volts	1

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C)¹ (V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ± 10%; -5.7V ≤ V_{BB} ≤ -4.5; V_{SS} = 0V)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT Average power supply operating current (\overline{RAS} , \overline{CAS} cycling; t_{RC} = 410ns)	I_{DD1}		35	mA	3
	I_{CC1}				4
	I_{BB1}		200	μA	
STANDBY CURRENT Power supply standby current (\overline{RAS} = V_{IHC} , D_{OUT} = High Impedance)	I_{DD2}	-10	1.5	mA	
	I_{CC2}		10	μA	
	I_{BB2}			μA	
REFRESH CURRENT Average power supply current, refresh mode (\overline{RAS} cycling, \overline{CAS} = V_{IHC} ; t_{RC} = 410ns)	I_{DD3}	-10	27	mA	3
	I_{CC3}		10	μA	
	I_{BB3}			μA	
PAGE MODE CURRENT Average power supply current, page-mode operation (\overline{RAS} = V_{IL} , \overline{CAS} cycling; t_{PC} = 275ns)	I_{DD4}		27	mA	3
	I_{CC4}				4
	I_{BB4}			μA	
INPUT LEAKAGE Input leakage current, any input (V_{BB} = -5V, 0V ≤ V_{IN} ≤ +7.0V, all other pins not under test = 0 volts)	$I_{I(L)}$	-10	10	μA	
OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V)	$I_{O(L)}$	-10	10	μA	
OUTPUT LEVELS Output high (Logic 1) voltage (I_{OUT} = -5mA)	V_{OH}	2.4		Volts	3
	V_{OL}		0.4	Volts	

NOTES:

- All voltages referenced to V_{SS} .
- Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh

operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (5.6,7)
 (0°C ≤ T_A ≤ 70°C) V_{DD} = 12.0V ±10%; V_{CC} = 5.0V ±10%; V_{SS} = 0V, -5.7V ≤ V_{BB} ≤ -4.5V)

PARAMETER	SYMBOL	MK4116-4		UNITS	NOTES
		MIN	MAX		
Random read or write cycle time	t _{RC}	410		ns	
Read-write cycle time	t _{RWC}	425		ns	
Read Modify Write	t _{RMW}	500		ns	
Page mode cycle time	t _{PC}	275		ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}		250	ns	8,10
Access time from $\overline{\text{CAS}}$	t _{CAC}		165	ns	9,10
Output buffer turn-off delay	t _{OFF}	0	60	ns	11
Transition time (rise and fall)	t _T	3	50	ns	7
$\overline{\text{RAS}}$ precharge time	t _{RP}	150		ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	250	10000	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	165		ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	165	10000	ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	250		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	35	85	ns	12
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	-20		ns	
Row Address set-up time	t _{ASR}	0		ns	
Row Address hold time	t _{RAH}	35		ns	
Column Address set-up time	t _{ASC}	-10		ns	
Column Address hold time	t _{CAH}	75		ns	
Column Address hold time referenced to $\overline{\text{RAS}}$	t _{AR}	160		ns	
Read command set-up time	t _{RCS}	0		ns	
Read command hold time	t _{RCH}	0		ns	
Write command hold time	t _{WCH}	75		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	t _{WCR}	160		ns	
Write command pulse width	t _{WP}	75		ns	
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	85		ns	
Write command to $\overline{\text{CAS}}$ lead time	t _{CWL}	85		ns	
Data-in set-up time	t _{DS}	0		ns	13
Data-in hold time	t _{DH}	75		ns	13
Data-in hold time referenced to $\overline{\text{RAS}}$	t _{DHR}	160		ns	
$\overline{\text{CAS}}$ precharge time (for page-mode cycle only)	t _{CP}	100		ns	
Refresh period	t _{REF}		2	ms	
$\overline{\text{WRITE}}$ command set-up time	t _{WCS}	-20		ns	14
$\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ delay	t _{CWD}	90		ns	14
$\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ delay	t _{RWD}	175		ns	14

3. I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. The maximum specified current values are for t_{RC}=410ns and t_{PC}=275ns. I_{DD} limit at other cycle rates are determined by the following equations:

I_{DD1} (max) [mA] = 10 + 10.25 × cycle rate [MHz]
 I_{DD3} (max) [mA] = 10 + 7 × cycle rate [MHz]
 I_{DD4} (max) [mA] = 10 + 4.7 × cycle rate [MHz]
4. I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135 typ) to data out. At all other times I_{CC} consists of leakage currents only.
5. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
6. AC measurements assume t_T=5ns.
7. V_{IHC} (min) or V_{IHL} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IHL} and V_{IL}.
8. Assumes that t_{RCD} ≤ t_{RCD} (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that t_{RCD} ≥ t_{RCD} (max).
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WRITE}}$ leading edge in delayed write or read-modify-write cycles.
14. t_{WCS}, t_{CWD} and t_{RWD} are restrictive operating parameters in read write and read modify write cycles only. If t_{WCS} ≥ t_{WCS} (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If t_{CWD} ≥ t_{CWD} (min) and t_{RWD} ≥ t_{RWD} (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
15. Effective capacitance calculated from the equation $C = \frac{I \Delta t}{\Delta v}$ with $\Delta v = 3$ volts and power supplies at nominal levels.
16. $\overline{\text{CAS}} = \text{V}_{\text{IHC}}$ to disable D_{OUT}.

AC ELECTRICAL CHARACTERISTICS**(0°C ≤ T_A ≤ 70°C) (V_{DD} = 12.0V ±10%; V_{SS} = 0V, -5.7V ≤ V_{BB} ≤ -4.5V)**

PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance (A ₀ –A ₆), D _{IN}	C _{I1}	4	5	pF	17
Input Capacitance $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, WRITE	C _{I2}	8	10	pF	17
Output Capacitance (D _{OUT})	C _O	5	7	pF	17,18

DESCRIPTION (continued)

System oriented features include ± 10% tolerance on all power supplies, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs (a common cause of soft errors), on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his

memory system. The MK 4116 also incorporates several flexible timing/operating modes. In addition to the usual read, write, and read-modify-write cycles, the MK 4116 is capable of delayed write cycles, page-mode operation and RAS-only refresh. Proper control of the clock inputs(RAS, CAS and WRITE) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

**SUPPLEMENTAL DATA SHEET TO BE USED IN
CONJUNCTION WITH MOSTEK MK4116(J/N/E)-2/3 DATA SHEET.**

PRELIMINARY

MOSTEK®

16,384 x 1-BIT DYNAMIC RAM

MK4516(N/E)-10/12/15

FEATURES

- ☐ Recognized industry standard 16-pin configuration from Mostek
- ☐ Single +5V ($\pm 10\%$) supply operation
- ☐ On chip substrate bias generator for optimum performance
- ☐ Active power 150mW maximum
Standby power 17mW maximum
- ☐ 100ns access time, 220ns cycle time (MK4516-10)
120ns access time, 250ns cycle time (MK4516-12)
150ns access time, 310ns cycle time (MK4516-15)
- ☐ Common I/O capability using "early write"
- ☐ Read, Write, Read-Write, Read-Modify-Write and Page-Mode capability
- ☐ All inputs TTL compatible, low capacitance, and are protected against static charge
- ☐ Scaled POLY 5 technology
- ☐ Pin compatible with the MK4164 (64K RAM)
- ☐ 128 refresh cycles (2msec)
- ☐ Offers two variations of hidden refresh
- ☐ Indefinite \overline{DOUT} hold using \overline{CAS} control

DESCRIPTION

The MK4516 is a single +5V power supply version of the industry standard MK4116, 16,384 x 1 bit dynamic RAM.

The high performance features of the MK4516 are achieved by state-of-the-art circuit design techniques as well as utilization of Mostek's "Scaled POLY 5" process technology. Features include access times starting where the current generation 16K RAMs leave off, TTL compatability, and +5V only operation.

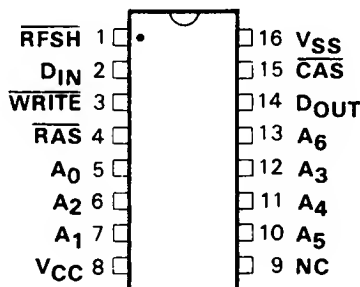
The MK4516 is capable of a variety of operations including READ, WRITE, READ-WRITE, READ-MODIFY-WRITE, PAGE MODE, and REFRESH. The output of the MK4516 can be held valid indefinitely by holding \overline{CAS} active low. This is quite useful since a refresh cycle can be performed while holding data valid from a previous cycle.

The MK4516 is designed to be compatible with the JEDEC standards for the 64K x 1 dynamic RAM. The MK4516 is intended to extend the life cycle of the 16K RAM, as well as create new applications due to its superior performance. The compatability with the MK4164 will also permit a common board design to service both the MK4516 and MK4164 (64K RAM) designs. The MK4516 will therefore permit a smoother transition to the 64K RAM as the industry standard MK4027 did for the MK4116.

The user, requiring only a small memory size, need no longer pay the three power supply penalty for achieving the economics of using dynamic RAM over static RAM when using this new generation device.

DYNAMIC
RAMS

PIN OUT



PIN FUNCTIONS

A_0 - A_6	Address Inputs	\overline{RAS}	Row Address Strobe
CAS	Col. Address Strobe	WRITE	Read/Write Input
DIN	Data In	RFSH	Refresh
DOUT	Data Out	VCC	Power (+5V)
		VSS	GND

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS}	-1.0V to +7.0V
Operating Temperature, T_A (Ambient)	0°C to +70°C
Storage Temperature (Ceramic)	-65°C to +150°C
Storage Temperature (Plastic)	-55°C to +125°C
Power Dissipation	1 Watt
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High (Logic 1) Voltage, All Inputs	2.4	—	$V_{CC}+1$	V	1
V_{IL}	Input Low (Logic 0) Voltage, All Inputs	-2.0	—	.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) V_{CC} = 5.0V ± 10%

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	OPERATING CURRENT t_{RC} = 220ns t_{RC} = 250ns t_{RC} = 310ns		27	mA	2
			25	mA	2
			23		2
I_{CC2}	STANDBY CURRENT Power supply standby current (RAS = V_{IH} , DOUT = High Impedance)		3	mA	2
$I_{1(L)}$	INPUT LEAKAGE Input leakage current, any input (0V ≤ V_{IN} ≤ +5.5V, all other pins not under test = 0 volts)	-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE Output leakage current (DOUT is disabled, 0V ≤ V_{OUT} ≤ +5.5V)	-10	10	μA	
V_{OH} V_{OL}	OUTPUT LEVELS	2.4	0.4	V V	
	Output High (Logic 1) voltage (I_{OUT} = -5mA) Output Low (Logic 0) voltage (I_{OUT} = 4.2mA)				

NOTES:

- All voltages referenced to V_{SS} .
- I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
- An initial pause of 100μs is required after power-up followed by any 8 RAS or RFSH cycles before proper device operation is achieved. If refresh counter is to be effective a minimum of 64 active RFSH initialization cycles is required. The internal refresh counter must be activated a minimum of 128 times every 2ms if the RFSH refresh function is used.
- AC characteristics assume t_r = 5ns
- V_{IH} min. and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} .
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- Load = 2TTL loads and 50pF.
- Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
- Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
- RFSH = V_{IH} , $\overline{\text{CAS}}$ = V_{IH} or V_{IL} , but is allowed to make an active to inactive transition during the RAS active time of RAS-only refresh cycle. WRITE = don't care. Data out depends on the state of CAS. If CAS = V_{IH} , data output is high impedance. If CAS = V_{IL} , the data output will contain data from the last valid read cycle.
- RAS = V_{IH} , $\overline{\text{CAS}}$ = V_{IH} or V_{IL} , but is allowed to make an active to inactive transition during the Pin 1 refresh cycle. ADDRESSES and WRITE = don't care. Data out depends on the state of $\overline{\text{CAS}}$. If $\overline{\text{CAS}}$ = V_{IH} , data output is high impedance. If CAS = V_{IL} , the data output will contain data from the last valid read cycle.

NOTES (Continued)

12. t_{OFF} max defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
13. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to \overline{CAS} leading edge in early write cycles and to \overline{WRITE} leading edge in delayed write or read-modify-write.
16. t_{WCS} , t_{CWD} , and t_{RWD} are restrictive operating parameters in READ/WRITE and READ/MODIFY/WRITE cycles only. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an EARLY WRITE cycle and the data output will remain

open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) the cycle is a READ/WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the condition of the data out (at excess time and until \overline{CAS} goes back to V_{IH}) is indeterminate.

17. If the RFSH function is not used, pin 1 may be left open (no connect).
18. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
19. If t_{CRP} is not satisfied then the following types of cycles will occur. a) A hidden REFRESH cycle can take place with the data valid from last read cycle as long as \overline{CAS} does not make an active to inactive transition. b) A RAS only cycle can also occur if \overline{CAS} makes an active to inactive transition beyond t_{CRP} min. The data out buffer will go to a high impedance mode after \overline{CAS} makes an inactive transition.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (3, 4, 5, 10, 11, 17, 18)
 $(0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}), V_{CC} = 5.0\text{V} \pm 10\%$

SYM	PARAMETER	MK4516-10		MK4516-12		MK4516-15		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random read or write cycle time	220		250		310		ns	6,7
t_{RMW}	Read modify write cycle time	260		295		365		ns	6,7
t_{PC}	Page mode cycle time	120		140		165		ns	6,7
t_{RAC}	Access time from \overline{RAS}		100		120		150	ns	7,8
t_{CAC}	Access time from \overline{CAS}		50		60		75	ns	7,9, 10,11
t_{OFF}	Output buffer turn-off delay	0	35	0	40		40	ns	12
t_T	Transition time (rise and fall)	3	50	3	50	3	50	ns	5
t_{RP}	\overline{RAS} precharge time	110		120		150		ns	
t_{RAS}	\overline{RAS} pulse width	100	10,000	120	10,000	150	10,000	ns	
t_{RSH}	\overline{RAS} hold time	50		60		75		ns	
t_{CSH}	\overline{CAS} hold time	100		120		150		ns	
t_{CAS}	\overline{CAS} pulse width	50	∞	60	∞	75	∞	ns	
t_{RCD}	\overline{RAS} to \overline{CAS} delay time	20	50	20	60	20	75	ns	13
t_{RRH}	Read command hold time referenced to \overline{RAS}	20		25		35		ns	14
t_{ASR}	Row Address set-up time	0		0		0		ns	
t_{RAH}	Row Address hold time	15		15		20		ns	
t_{ASC}	Column Address set-up time	0		0		0		ns	
t_{CAH}	Column Address hold time	15		20		25		ns	
t_{AR}	Column Address hold time referenced to \overline{RAS}	65		80		100		ns	
t_{RCS}	Read command set-up time	0		0		0		ns	
t_{RCH}	Read command hold time referenced to \overline{CAS}	0		0		0		ns	14
t_{WCH}	Write command hold time	35		40		50		ns	

DYNAMIC RAMS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYM	PARAMETER	MK4516-10		MK4516-12		MK4516-15		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t _{WCR}	Write command hold time referenced to $\overline{\text{RAS}}$	85		100		125		ns	
t _{WP}	Write command pulse width	30		35		45		ns	
t _{RWL}	Write command to $\overline{\text{RAS}}$ lead time	35		40		50		ns	
t _{CWL}	Write command to $\overline{\text{CAS}}$ lead time	35		40		50		ns	
t _{DS}	Data-in set-up time	0		0		0		ns	15
t _{DH}	Data-in hold time	35		40		45		ns	15
t _{DHR}	Data-in hold time referenced to $\overline{\text{RAS}}$	85		100		120		ns	
t _{CP}	$\overline{\text{CAS}}$ precharge time (for page-mode cycle only)	60		70		80		ns	
t _{REF}	Refresh period		2		2		2	ms	
t _{WCS}	WRITE command set-up time	0		0		0		ns	16
t _{CWD}	$\overline{\text{CAS}}$ to WRITE delay	50		60		75		ns	16
t _{RWD}	$\overline{\text{RAS}}$ to WRITE delay	100		120		150		ns	16
t _{FSR}	$\overline{\text{RFSH}}$ set-up time referenced to RAS	110		120		150		ns	
t _{RFD}	$\overline{\text{RAS}}$ to $\overline{\text{RFSH}}$ delay	110		120		150		ns	
t _{FC}	$\overline{\text{RFSH}}$ cycle time	220		250		310		ns	
t _{FP}	$\overline{\text{RFSH}}$ active time	100		120		150		ns	
t _{FHR}	$\overline{\text{RFSH}}$ hold time referenced to RAS	0		0		0		ns	
t _{FI}	$\overline{\text{RFSH}}$ inactive time	110		120		150		ns	
t _{FRD}	$\overline{\text{RFSH}}$ to $\overline{\text{RAS}}$ delay (Test mode write only)	50		50		50		ns	
t _{CPN}	$\overline{\text{CAS}}$ precharge time	25		30		40		ns	
t _{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	-20		-20		-20		ns	19

OPERATION

The 14 address bits required to decode 1 of the 16,384 cell locations within the MK4516 are multiplexed onto the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, Row Address Strobe ($\overline{\text{RAS}}$), latches the 7 row addresses into the chip. The high-to-low transition of the second clock, Column Address Strobe ($\overline{\text{CAS}}$), subsequently latches the 7 column addresses into the chip. Each of these signals, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way

that the address multiplexing operation is done outside of the critical timing path for read data access. The later events in the $\overline{\text{CAS}}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{\text{RAS}}$ clock chain. This "gated $\overline{\text{CAS}}$ " feature allows the $\overline{\text{CAS}}$ clock to be externally activated as soon as the Row Address Hold specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

The "gated $\overline{\text{CAS}}$ " feature permits $\overline{\text{CAS}}$ to be activated at any time after t_{RAH} and it will have no effect on the

OPERATION (Continued)

worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of $\overline{\text{CAS}}$ which are called $t_{\text{RCD}}(\text{min})$ and $t_{\text{RCD}}(\text{max})$. No data storage or reading errors will result if $\overline{\text{CAS}}$ is applied to the MK4516 at a point in time beyond the $t_{\text{RCD}}(\text{max})$ limit. However, access time will then be determined exclusively by the access time from $\overline{\text{CAS}}$ (t_{CAC}) rather than from $\overline{\text{RAS}}$ (t_{RAC}), and $\overline{\text{RAS}}$ access time will be lengthened by the amount that t_{RCD} exceeds the $t_{\text{RCD}}(\text{max})$ limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{\text{WRITE}}$ and $\overline{\text{CAS}}$ while $\overline{\text{RAS}}$ is active. The latter of $\overline{\text{WRITE}}$ or $\overline{\text{CAS}}$ to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{\text{WRITE}}$ input is brought low (active) prior to $\overline{\text{CAS}}$ being brought low (active), the D_{IN} is strobed by $\overline{\text{CAS}}$, and the Input Data set-up and hold times are referenced to $\overline{\text{CAS}}$. If the input data is not available at $\overline{\text{CAS}}$ time (late write) or if it is desired that the cycle be a read-write or read-modify-write cycle the $\overline{\text{WRITE}}$ signal should be delayed until after $\overline{\text{CAS}}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{\text{WRITE}}$ rather than $\overline{\text{CAS}}$.

Data is retrieved from the memory in a read cycle by maintaining $\overline{\text{WRITE}}$ in the inactive or high state throughout the portion of the memory cycle in which both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are low (active). Data read from the selected cell is available at the output port within the specified access time. The output data is the same polarity (not inverted) as the input data.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the MK4516 is the high impedance (open-circuit) state; anytime $\overline{\text{CAS}}$ is high (inactive) the D_{OUT} pin will be floating. Once the output data port has gone active, it will remain valid until $\overline{\text{CAS}}$ is taken to the precharge (inactive high) state. Note that $\overline{\text{CAS}}$ can be left active (low) indefinitely. This permits either $\overline{\text{RAS}}$ -only or $\overline{\text{RFSH}}$ refresh cycles to occur without invalidating D_{OUT} .

PAGE MODE OPERATION

The Page Mode feature of the MK4516 allows for successive memory operations at multiple column locations within the same row address. This is done by strobing the row address into the chip and maintaining the $\overline{\text{RAS}}$ signal low (active) throughout all successive

memory cycles in which the row address is common. The first access within a page mode operation will be available at t_{RAC} or t_{CAC} time, whichever is the limiting parameter. However, all successive accesses within the page mode operation will be available at t_{CAC} time (referenced to $\overline{\text{CAS}}$). With the MK4516, this results in as much as a 50% improvement in access times! Effective memory cycle times are also reduced when using page mode.

The page mode boundary of a single MK4516 is limited to the 128 column locations determined by all combinations of the 7 column address bits. Operations within the page boundary need not be sequentially addressed and any combination of read, write, and read-modify-write cycle are permitted within the page mode operation.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2ms interval. Although any normal memory cycle will perform the required refreshing, this function is easily accomplished by using either $\overline{\text{RAS}}$ -only or $\overline{\text{RFSH}}$ type refreshing.

$\overline{\text{RAS}}$ -ONLY REFRESH

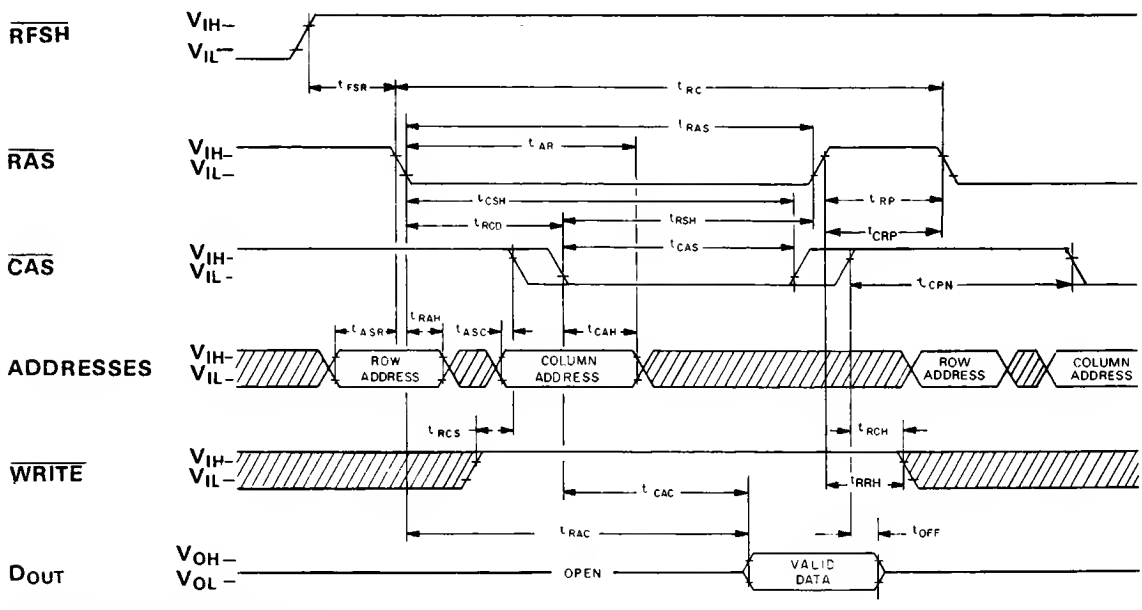
The $\overline{\text{RAS}}$ -only refresh cycle supported by the MK4516 requires that a 7 bit refresh address be valid at the device address inputs when $\overline{\text{RAS}}$ goes low (active). The state of the output data port during a $\overline{\text{RAS}}$ -only refresh is controlled by $\overline{\text{CAS}}$. If $\overline{\text{CAS}}$ is high (inactive) during the entire time that $\overline{\text{RAS}}$ is asserted, the output will remain in the high impedance state. If $\overline{\text{CAS}}$ is low (active) the entire time that $\overline{\text{RAS}}$ is asserted, the output port will remain in the same state that it was prior to the issuance of the $\overline{\text{RAS}}$ signal. This is useful for single step operation. If $\overline{\text{CAS}}$ makes a low-to-high transition during the $\overline{\text{RAS}}$ -only refresh cycle, the output data buffer will assume the high impedance state.

PIN 1 REFRESH

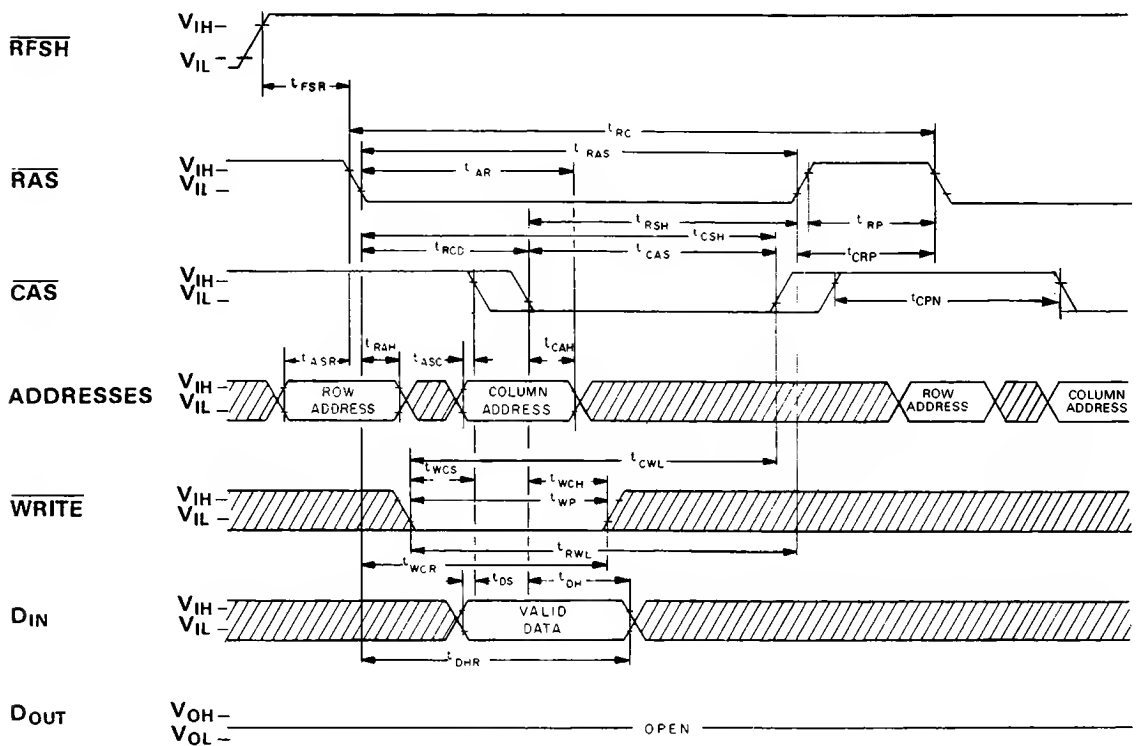
$\overline{\text{RFSH}}$ type refreshing available on the MK4516 offers an attractive alternate refresh method. When the signal on pin 1, $\overline{\text{RFSH}}$, is brought low during $\overline{\text{RAS}}$ inactive time ($\overline{\text{RAS}}$ high), an on-chip refresh counter is enabled and an internal refresh operation takes place. When $\overline{\text{RFSH}}$ is brought high (inactive) the internal refresh address counter is automatically incremented in preparation for the next refresh cycle. Data can be held valid from a previous cycle using $\overline{\text{CAS}}$ control during a $\overline{\text{RFSH}}$ type refresh cycle.

The internal refresh counter is a dynamic counter and requires refreshing. The 128 $\overline{\text{RFSH}}$ cycles every 2 milliseconds required to refresh the memory cells is adequate for this purpose. Only $\overline{\text{RFSH}}$ activated cycles affect the internal counter.

READ CYCLE



WRITE CYCLE (EARLY WRITE)

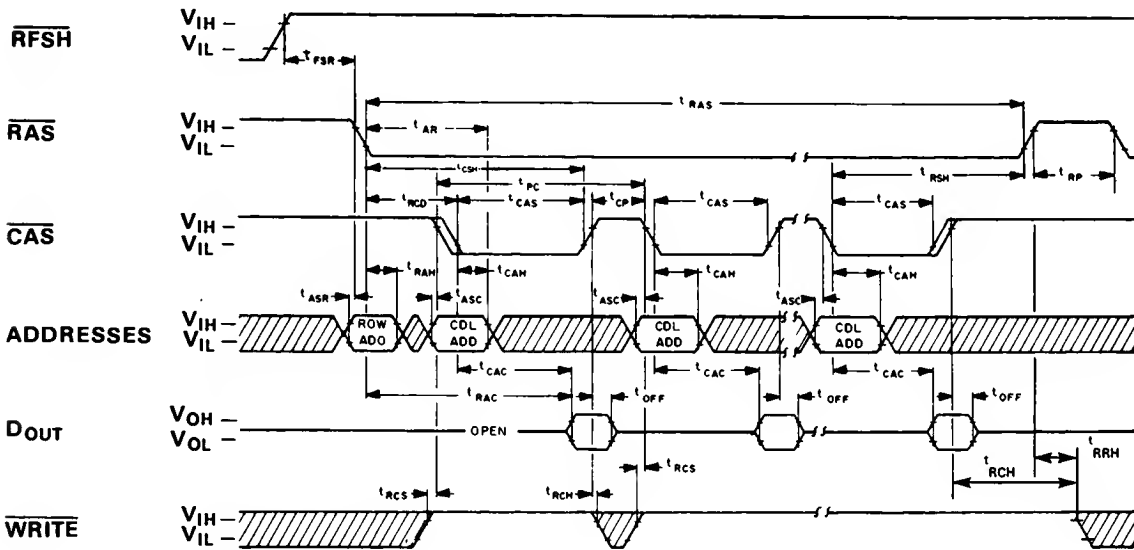


RFSH

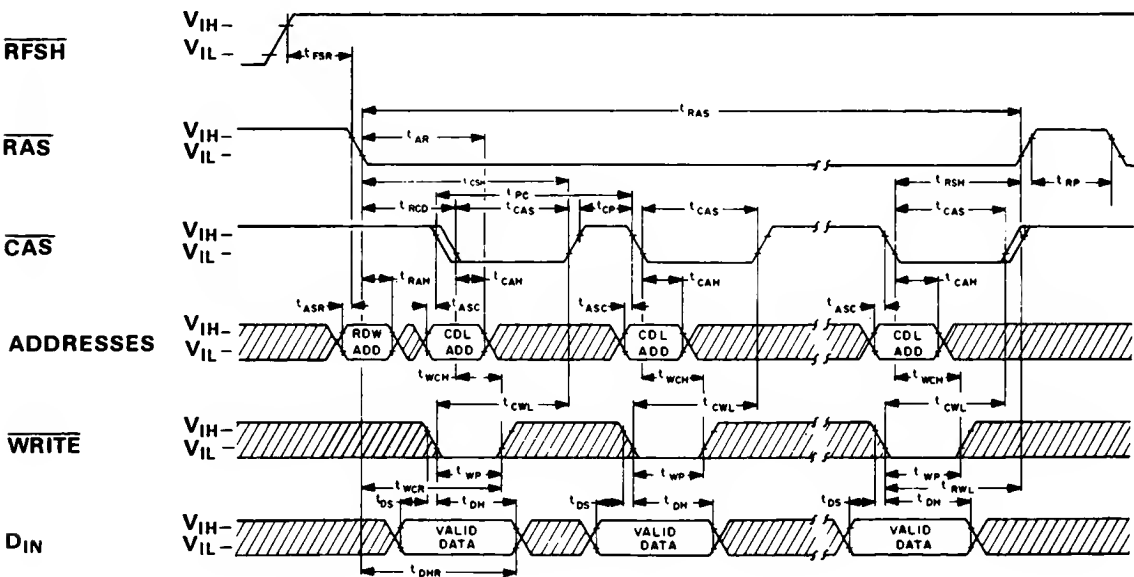


"RAS-ONLY" REFRESH CYCLE

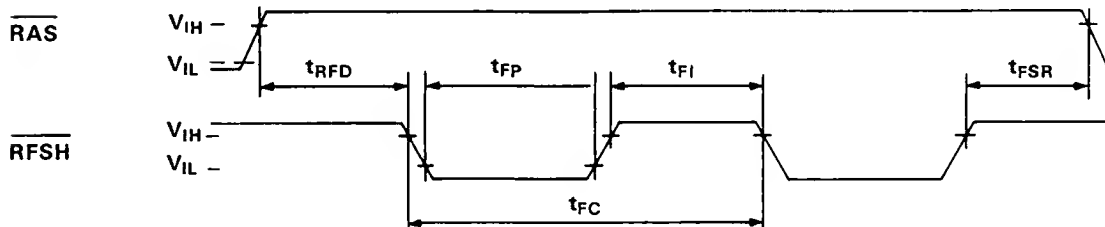
PAGE MODE READ CYCLE



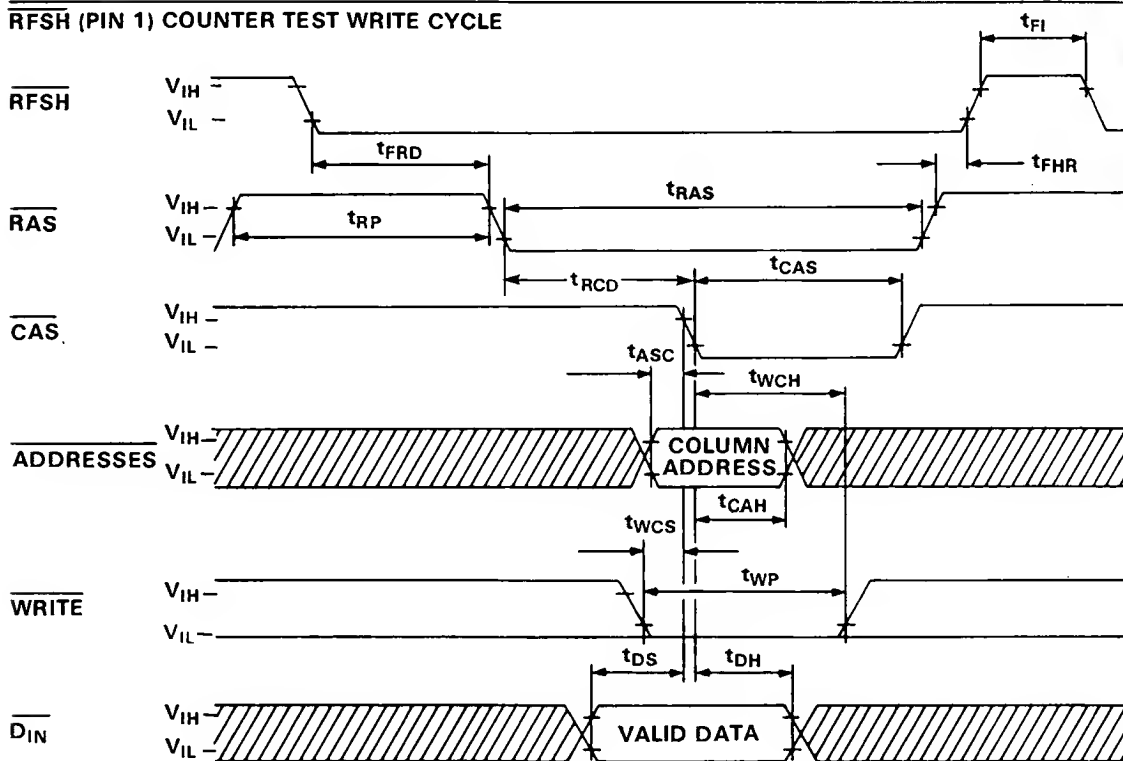
PAGE MODE WRITE CYCLE



RFSH (PIN 1) REFRESH CYCLE (SEE NOTE 11)



RFSH (PIN 1) COUNTER TEST WRITE CYCLE



DYNAMIC
RAMS

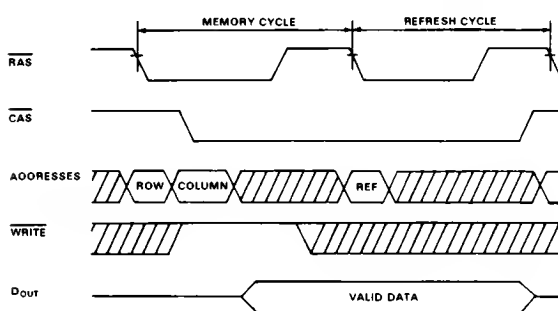
The use of $\overline{\text{RFSH}}$ mode for refreshing eliminates the need to generate refresh addresses externally.

Furthermore, when using $\overline{\text{RFSH}}$ refreshing, the address drivers, the $\overline{\text{CAS}}$ drivers, and $\overline{\text{WRITE}}$ drivers can be powered down during battery backup standby operation.

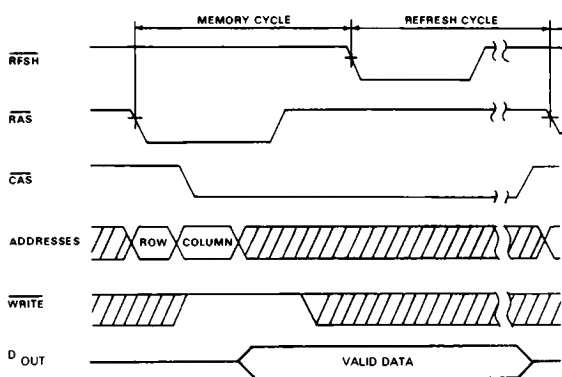
HIDDEN REFRESH

Either a $\overline{\text{RAS}}$ -only or $\overline{\text{RFSH}}$ type refresh cycle may take place while maintaining valid output data by extending the $\overline{\text{CAS}}$ active time from a previous memory read cycle. This feature is referred to as a hidden refresh. (See figures below.)

HIDDEN $\overline{\text{RAS}}$ -ONLY REFRESH CYCLE (SEE NOTE 10)



HIDDEN $\overline{\text{RFSH}}$ REFRESH CYCLE (SEE NOTE 11)



$\overline{\text{RFSH}}$ (PIN 1) TEST CYCLE

A special timing sequence using the Pin 1 counter test cycle provides a convenient method of verifying the functionality of the $\overline{\text{RFSH}}$ activated circuitry.

When $\overline{\text{RFSH}}$ is activated prior to and remains valid through a normal write cycle, the $\text{D}_{1\text{N}}$ is written into the memory location defined by the current contents of the on-chip refresh counter and the column address present at the external address pins during the high-to-low transition of $\overline{\text{CAS}}$. (See Pin 1 counter test write timing diagram.)

The following test procedure may be used to verify the functionality of the internal refresh counter. There are a multitude of patterns and sequences which may also be used to verify the $\overline{\text{RFSH}}$ feature. This test should be performed after it has been confirmed that the device can uniquely address all 16,384 storage locations.

SUGGESTED $\overline{\text{RFSH}}$ COUNTER TEST PROCEDURE

1. Initialize the on-chip refresh counter. 64 cycles are adequate for this purpose.
2. Write a test pattern of zeroes into the memory at a single column address and all row addresses by using 128 $\overline{\text{RFSH}}$ (pin 1) refresh counter test write cycles.
3. Verify the data written into the RAM by using the column address used in step 2 and sequence through all row address combinations by using conventional read cycles.
4. Compliment the test pattern and repeat steps 2 and 3.

MOSTEK®

32,768x1-BIT DYNAMIC RAM

MK4332(D)-3

FEATURES

- Utilizes two industry standard MK 4116 devices in an 18-pin package configuration
- 200ns access time, 375ns cycle (MK 4116-3)
- Separate RAS, CAS Clocks
- $\pm 10\%$ tolerance on all power supplies (+12V, +5V)
- Low power: 482mW active, 40mW standby (max)
- Output data controlled by $\overline{\text{CAS}}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- Common I/O capability using "early write" operation
- Read-Modify-Write, $\overline{\text{RAS}}$ -only refresh, and Page-mode capability
- All inputs TTL compatible, low capacitance, and protected against static charge
- 128 refresh cycles for each MK 4116 device in the dual density configuration
- Pin compatible to MK 4116 and MK 4164

DESCRIPTION

The MK 4332 is a new generation MOS dynamic random access memory circuit organized as 32,768 words by 1 bit. As a state-of-the-art MOS memory device, the MK4332 (32K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user.

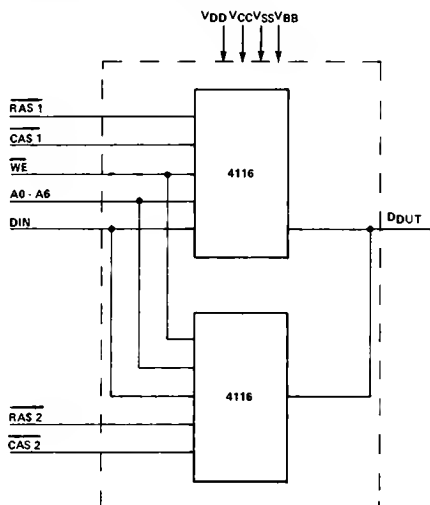
The technology used to fabricate the MK 4332 is MOSTEK's double-poly, N-channel silicon gate, POLY II[®] process. This process, coupled with the use of a single transistor dynamic storage cell, provides the maximum possible circuit density and reliability, while maintaining high performance capability. The use of dynamic circuitry throughout, including sense amplifiers, assures that power

dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the MK 4332 a truly superior RAM product.

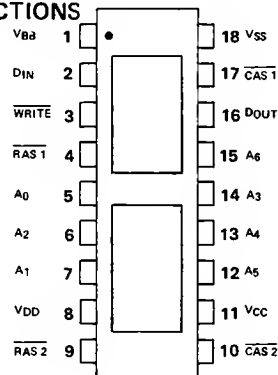
Multiplexed address inputs (a feature pioneered by MOSTEK for its 4K RAMS) permits the MK 4332 to be packaged in a standard 18-pin DIP. This standard package configuration, is compatible with widely available automated testing and insertion equipment, and it provides the highest possible system bit densities and simplifies system upgrade from 16K to 64K RAMs for new generation applications. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

DYNAMIC RAMS

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A0-A6	ADDRESS INPUTS
CAS	COLUMN ADDRESS STRDBE
DIN	DATA IN
DOUT	DATA OUT
RAS	RDW ADDRESS STRDBE
WRITE	READ/WRITE INPUT
VBB	POWER (-5V)
VCC	POWER (+5V)
VDD	POWER (+12V)
VSS	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB}	-0.5V to +20V	*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
Voltage on V_{DD} , V_{CC} supplies relative to V_{SS}	-1.0V to +15.0V	
$V_{BB}-V_{SS}$ ($V_{DD}-V_{SS}>0V$)	0V	
Operating temperature, T_A (Ambient)	0°C to +70°C	
Storage temperature (Ambient)	-65°C to +150°C	
Short circuit output current	50mA	
Power dissipation	1 Watt	

RECOMMENDED DC OPERATING CONDITIONS⁶

(0°C ≤ T_A ≤ 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	10.8	12.0	13.2	Volts	2
	V_{CC}	4.5	5.0	5.5	Volts	2,3
	V_{SS}	0	0	0	Volts	2
	V_{BB}	-4.5	-5.0	-5.7	Volts	2
Input High (Logic 1) Voltage, RAS, CAS, WRITE	V_{IHC}	2.4	—	7.0	Volts	2
Input High (Logic 1) Voltage, all inputs except RAS, CAS, WRITE	V_{IH}	2.2	—	7.0	Volts	2
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	—	.8	Volts	2

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) ($V_{DD} = 12.0V \pm 10\%$; $V_{CC} = 5.0V \pm 10\%$; -5.7V ≤ V_{BB} ≤ -4.5V; $V_{SS} = 0V$)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT Average power supply operating current (RAS, CAS cycling; $t_{RC} = t_{RC \text{ Min}}$)	I_{DD1}		36.5	mA	4,19
	I_{CC1}				5
	I_{BB1}		300	μA	19
STANDBY CURRENT Power supply standby current (RAS = V_{IHC} , $D_{OUT} = \text{High Impedance}$)	I_{DD2}	-20	3.0	mA	
	I_{CC2}		20	μA	
	I_{BB2}		200	μA	
REFRESH CURRENT Average power supply current, refresh mode (RAS cycling, CAS = V_{IHC} ; $t_{RC} = t_{RC \text{ Min}}$)	I_{DD3}	-20	26.5	mA	4, 19
	I_{CC3}		20	μA	
	I_{BB3}		300	μA	19
PAGE MODE CURRENT Average power supply current, page-mode operation (RAS = V_{IL} , CAS cycling; $t_{PC} = t_{PC \text{ Min}}$)	I_{DD4}		28.5	mA	4,19
	I_{CC4}				5
	I_{BB4}		300	μA	19
INPUT LEAKAGE Input leakage current, any input ($V_{BB} = -5V$, $0V \leq V_{IN} \leq +7.0V$, all other pins not under test = 0 volts)	$I_{I(L)}$	-20	20	μA	
OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, $0V \leq V_{OUT} \leq +5.5V$)	$I_{O(L)}$	-20	20	μA	
OUTPUT LEVELS Output high (Logic 1) voltage ($I_{OUT} = -5mA$)	V_{OH}	2.4		Volts	3
	V_{OL}		0.4	Volts	

NOTES:

- T_A is specified here for operation at frequencies to $t_{RC} \geq t_{RC \text{ (min)}}$. Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met. See figure 1 for derating curve.
- All voltages referenced to V_{SS} .
- Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
- I_{DD1} , I_{DD3} , and I_{DD4} depend on cycle rate. See figures 2,3, and 4 for I_{DD} limits at other cycle rates.
- I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135 μ typ) to data out. At all other times I_{CC} consists of leakage currents only.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (6,7,8)
 (0°C ≤ T_A ≤ 70°C)¹ (V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ± 10%, V_{SS} = 0V, -5.7V ≤ V_{BB} ≤ -4.5V)

PARAMETER	SYMBOL	MK 4332		UNITS	NOTES
		MIN	MAX		
Random read or write cycle time	t _{RC}	375		ns	9
Read-write cycle time	t _{RWC}	375		ns	9
Read modify write cycle time	t _{RMW}	405		ns	9
Page mode cycle time	t _{PC}	225		ns	9
Access time from $\overline{\text{RAS}}$	t _{RAC}		200	ns	10,12
Access time from $\overline{\text{CAS}}$	t _{CAC}		135	ns	11,12
Output buffer turn-off delay	t _{OFF}	0	50	ns	13
Transition time (rise and fall)	t _T	3	50	ns	8
$\overline{\text{RAS}}$ precharge time	t _{RP}	120		ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	200	10,000	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	135		ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	200		ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	135	10,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	25	65	ns	14
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	-20		ns	
Row Address set-up time	t _{ASR}	0		ns	
Row Address hold time	t _{RAH}	25		ns	
Column Address set-up time	t _{ASC}	-10		ns	
Column Address hold time	t _{CAH}	55		ns	
Column Address hold time referenced to $\overline{\text{RAS}}$	t _{AR}	120		ns	
Read command set-up time	t _{RCS}	0		ns	
Read command hold time	t _{RCH}	0		ns	
Write command hold time	t _{WCH}	55		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	t _{WCR}	120		ns	
Write command pulse width	t _{WP}	55		ns	
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	70		ns	
Write command to $\overline{\text{CAS}}$ lead time	t _{CWL}	70		ns	
Data-in set-up time	t _{DS}	0		ns	15
Data-in hold time	t _{DH}	55		ns	15
Data-in hold time referenced to $\overline{\text{RAS}}$	t _{DHR}	120		ns	
$\overline{\text{CAS}}$ precharge time (for page-mode cycle only)	t _{CP}	80		ns	
Refresh period	t _{REF}		2	ms	
$\overline{\text{WRITE}}$ command set-up time	t _{WCS}	-20		ns	16
$\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ delay	t _{CWD}	80		ns	16
$\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ delay	t _{RWD}	145		ns	16

NOTES (Continued)

- Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
- AC measurements assume t_T = 5ns.
- V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
- The specifications for t_{RC} (min), t_{RMW} (min) and t_{RPW} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- Assumes that t_{RCD} ≤ t_{RCD} (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
- Assumes that t_{RCD} ≥ t_{RCD} (max).
- Measured with a load equivalent to 2 TTL loads and 100pF.
- t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
- These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WRITE}}$ leading edge in delayed write or read-modify-write cycles.
- t_{WCS}, t_{CWD} and t_{RWD} are restrictive operating parameters in read write and read modify write cycles only. If t_{WCS} ≥ t_{WCS} (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If t_{CWD} ≥ t_{CWD} (min) and t_{RWD} ≥ t_{RWD} (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
- Effective capacitance calculated from the equation C = $\frac{\Delta I}{\Delta V}$ with ΔV = 3 volts and power supplies at nominal levels.
- $\overline{\text{CAS}}$ = V_{IHC} to disable D_{OUT}.
- One 16K RAM is active while the other is in standby mode.

AC ELECTRICAL CHARACTERISTICS

($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$) ($V_{DD} = 12.0\text{V} \pm 10\%$; $V_{SS} = 0\text{V}$; $-5.7\text{V} \leq V_{BB} \leq -4.5\text{V}$)

PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance (A_0 – A_6), D_{IN}	C_{I1}	8	10	pF	17
Input Capacitance \overline{RAS} , \overline{CAS}	C_{I2}	8	10	pF	17
Output Capacitance (D_{OUT})	C_O	10	14	pF	17, 18
Input Capacitance \overline{WRITE}	C_{I3}	16	20	pF	17

AC Characteristics and Timing Diagrams of MK4116-3.

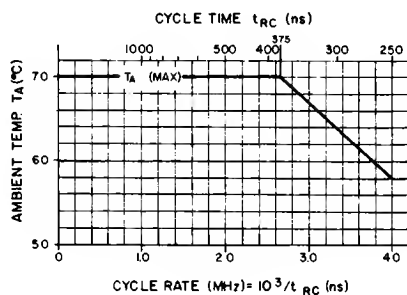


Fig. 1 Maximum ambient temperature versus cycle rate for extended frequency operation. T_A (max) for operation at cycling rates greater than 2.66 MHz ($t_{CYC} < 375\text{ns}$) is determined by T_A (max) $^{\circ}\text{C} = 70 - 9.0 \times (\text{cycle rate MHz} - 2.66)$ for -3.

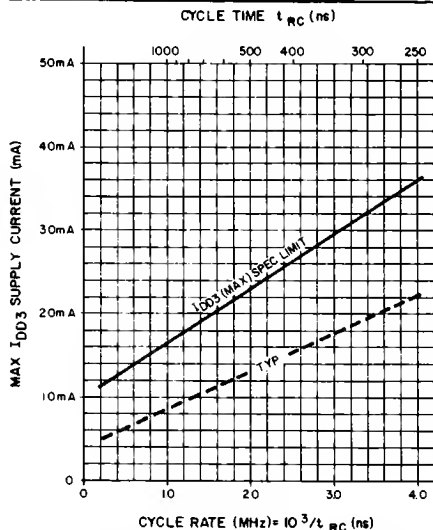


Fig. 3 Maximum I_{DD3} versus cycle rate for device operation at extended frequencies. I_{DD3} (max) curve is defined by the equation:

$$I_{DD3}(\text{max}) \text{ mA} = 10 + 6.5 \times \text{cycle rate [MHz]} \text{ for } -3$$

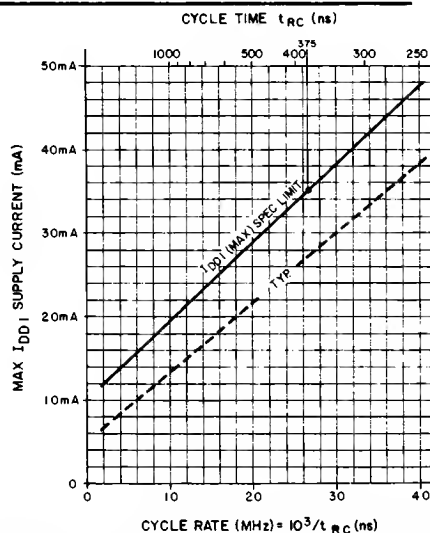


Fig. 2 Maximum I_{DD1} versus cycle rate for device operation at extended frequencies. I_{DD1} (max) curve is defined by the equation:

$$I_{DD1}(\text{max}) \text{ mA} = 10 + 9.4 \times \text{cycle rate [MHz]} \text{ for } -3$$

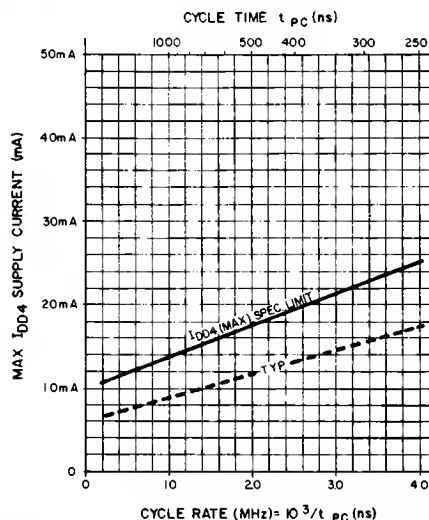
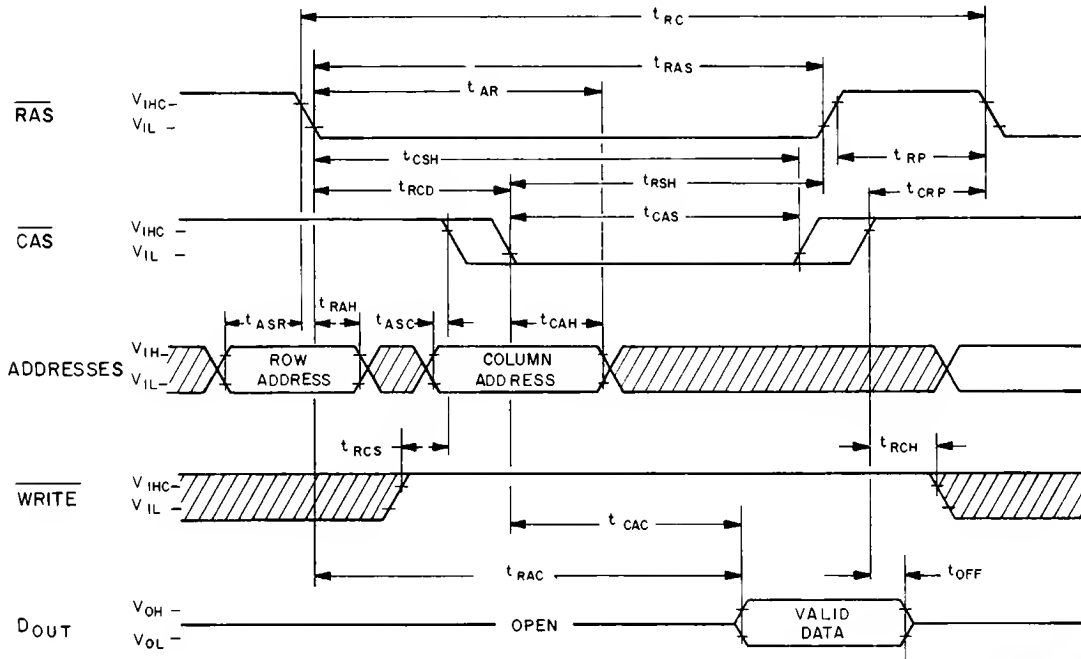


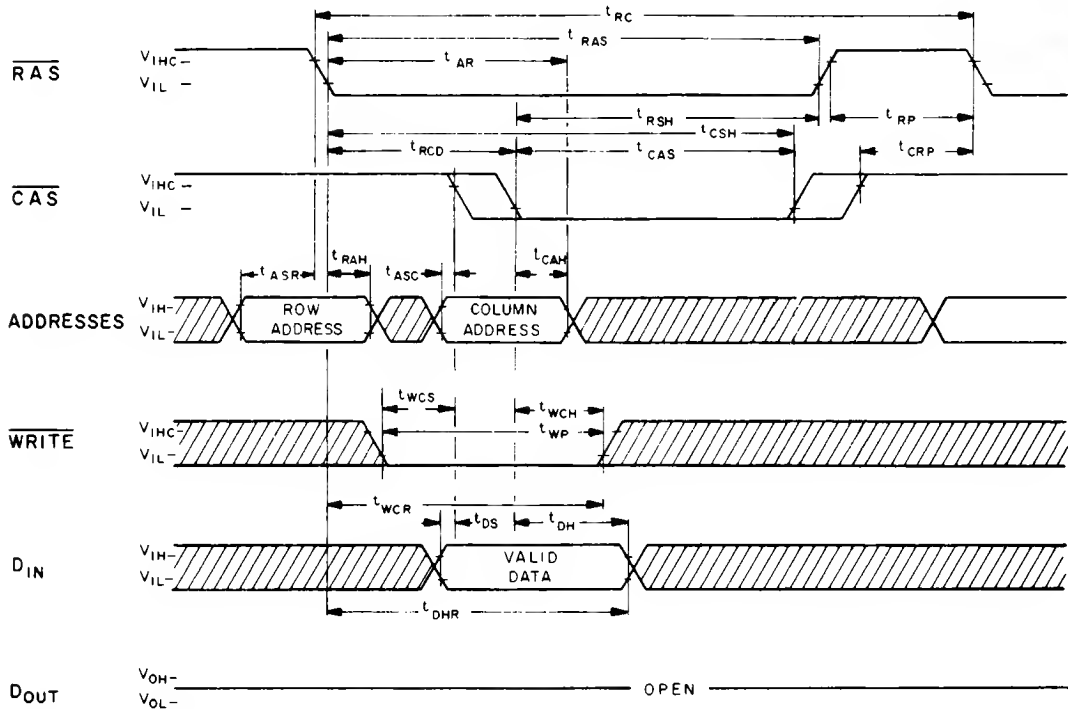
Fig. 4 Maximum I_{DD4} versus cycle rate for device operation in page mode. I_{DD4} (max) curve is defined by the equation:

$$I_{DD4}(\text{max}) \text{ mA} = 10 + 3.75 \times \text{cycle rate [MHz]} \text{ for } -3$$

READ CYCLE

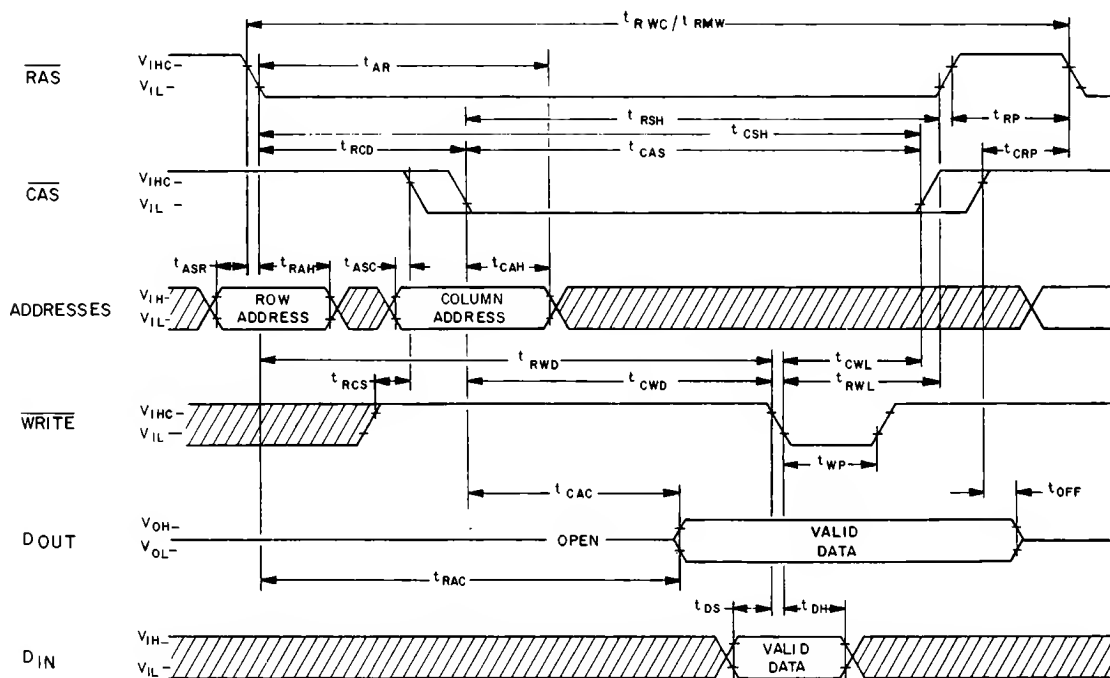


WRITE CYCLE (EARLY WRITE)



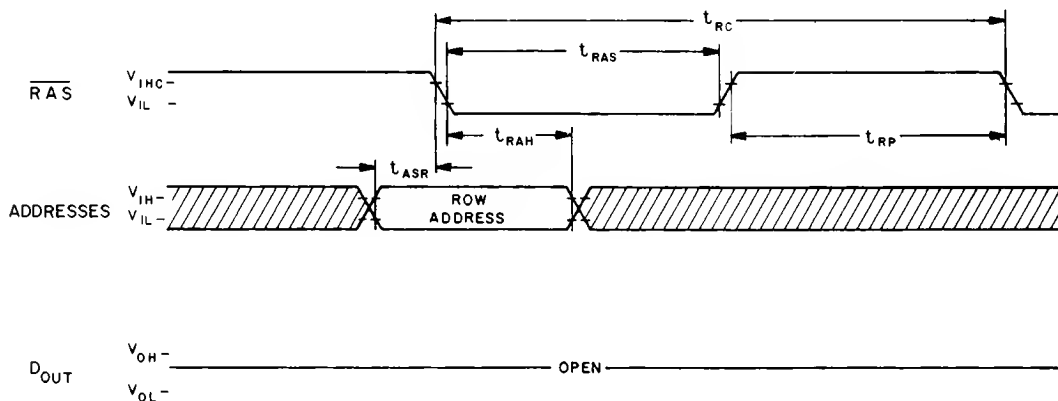
DYNAMIC
RAMS

READ-WRITE/READ-MODIFY-WRITE CYCLE

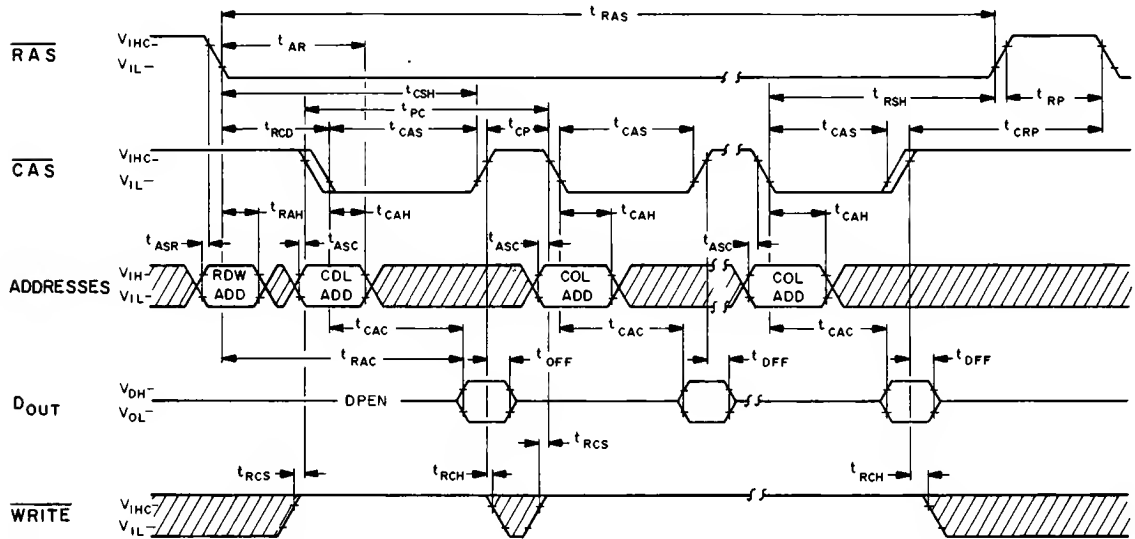


"RAS-ONLY" REFRESH CYCLE

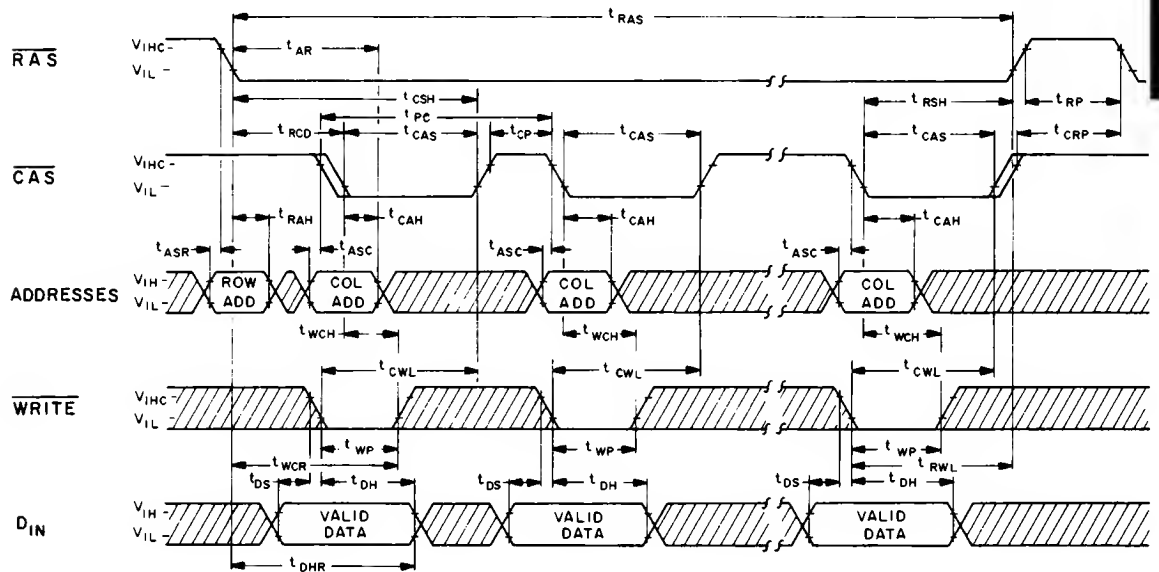
NOTE: $\overline{CAS} = V_{IH}$, $\overline{WRITE} = \text{Don't Care}$



PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



DYNAMIC
RAMS

DESCRIPTION (continued)

System oriented features include $\pm 10\%$ tolerance on all power supplies, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs (a common cause of soft errors), on-chip address and data registers which eliminate the need for interface registers, and two chip select methods. The MK 4332 also incorporates several flexible timing/operating modes. In addition to the usual read, write, and read-modify-write cycles, the MK 4332 is capable of delayed write cycles, page-mode operation and RAS-only refresh. Proper control of the clock inputs (RAS, CAS and WRITE) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

ADDRESSING

User access of a unique memory location is accomplished by multiplexing 14 address bits onto 7 address inputs and by proper control of the RAS and CAS clocks in a manner identical to operation of the MK 4116 in a memory array board. The 14 address bits required to decode 1 of the 16,384 cell locations within each MK 4116 are multiplexed onto the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, the Row Address Strobe (RAS), latches the 7 row address bits into the chip. The second clock, the Column Address Strobe (CAS), subsequently latches the 7 column address bits into the chip. Each of these signals, RAS and CAS, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the CAS clock sequence are inhibited until the occurrence of a delayed signal derived from the RAS clock chain. This "gated CAS" feature allows the CAS clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Note that CAS can be activated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing end-points result from the internal gating of CAS which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if CAS is applied to the MK 4332 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from CAS (t_{CAC}) rather than from RAS (t_{RAC}), and access time from RAS will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of WRITE and CAS while RAS is active. The later of the signals (WRITE or CAS) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits

several options in the write cycle timing. In a write cycle, if the WRITE input is brought low (active) prior to \overline{CAS} , the D_{IN} is strobed by \overline{CAS} , and the set-up and hold times are referenced to CAS. If the input data is not available at CAS time or if it is desired that the cycle be a read-write cycle, the WRITE signal will be delayed until after CAS has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of WRITE rather than CAS. (To illustrate this feature, D_{IN} is referenced to WRITE in the timing diagrams depicting the read-write and page-mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to CAS).

Data is retrieved from the memory in a read cycle by maintaining WRITE in the inactive or high state throughout the portion of the memory cycle in which CAS is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the MK 4332 is the high impedance (open-circuit) state. That is to say, anytime CAS is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until CAS is taken back to the inactive (high level) condition.

Since the outputs to both 16K devices are tied together, care must be taken with the timing relationships of the two devices. Both devices cannot be activated at the same time as a data output conflict can occur.

If the memory cycle in progress is a read, read-modify write, or a delayed write cycle, then the data output will go from the high impedance state to the active condition, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. Once having gone active, the output will remain valid until CAS is taken to the precharge (logic 1) state, whether or not RAS goes into precharge.

If the cycle in progress is an "early-write" cycle (WRITE active before CAS goes active), then the output pin will maintain the high impedance state throughout the entire cycle. Note that with this type of output configuration, the user is given full control of the D_{OUT} pin simply by controlling the placement of WRITE command during a write cycle, and the pulse width of the Column Address Strobe during read operations. Note also that even though data is not latched at the output, data can remain valid from access time until the beginning of a subsequent cycle without paying any penalty in overall memory cycle time (stretching the cycle).

This type of output operation results in some very significant system implications.

Common I/O Operation — If all write operations are handled in the "early write" mode, then D_{IN} can be connected directly to D_{OUT} for a common I/O data bus.

Data Output Control — D_{OUT} will remain valid during a read cycle from t_{CAC} until \overline{CAS} goes back to a high level (precharge), allowing data to be valid from one cycle up until a new memory cycle begins

with no penalty in cycle time. This also makes the RAS/CAS clock timing relationship very flexible.

Two Methods of Chip Selection — Since DOUT is not latched, CAS is not required to turn off the outputs of unselected memory devices in a matrix. This means that both CAS and/or RAS can be decoded for chip selection. If both RAS and CAS are decoded, then a two dimensional (X,Y) chip select array can be realized.

Extended Page Boundary — Page-mode operation allows for successive memory cycles at multiple column locations of the same row address. By decoding CAS as a page cycle select signal, the page boundary can be extended beyond the 128 column locations in a single chip. (See page-mode operation).

OUTPUT INTERFACE CHARACTERISTICS

The three state data output buffer presents the data output pin with a low impedance to VCC for a logic 1 and a low impedance to VSS for a logic 0. The effective resistance to VCC (logic 1 state) is 420 Ω maximum and 135 Ω typically. The resistance to VSS (logic 0 state) is 95 Ω maximum and 35 Ω typically. The separate VCC pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the VCC pin may have power removed without affecting the MK 4332 refresh operation. This allows all system logic except the RAS timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

PAGE MODE OPERATION

The "Page Mode" feature of the MK 4332 allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the RAS signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "page-mode" of operation will not dissipate the power associated with the negative going edge of RAS. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

The page boundary of a single MK 4116 is limited to the 128 column locations determined by all combinations of the 7 column address bits. However, the page boundary of the MK4332 can be extended by using CAS rather than RAS as the chip select signal. RAS is applied to all devices to latch the row address into each device and then CAS is decoded and serves as a page cycle select signal. Only those devices which receive both RAS and CAS signals will execute a read or write cycle.

REFRESH

Refresh of the MK4116 is accomplished by performing a memory cycle at each of the 128 row addresses within each 2 millisecond time interval. Each MK4116 in the MK4332 Assembly must receive all 128 refresh cycles within the 2ms time interval in order to completely refresh all 32,768 memory cells.

Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "RAS-only" cycles. RAS-only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the IDD3 specification.

POWER CONSIDERATIONS

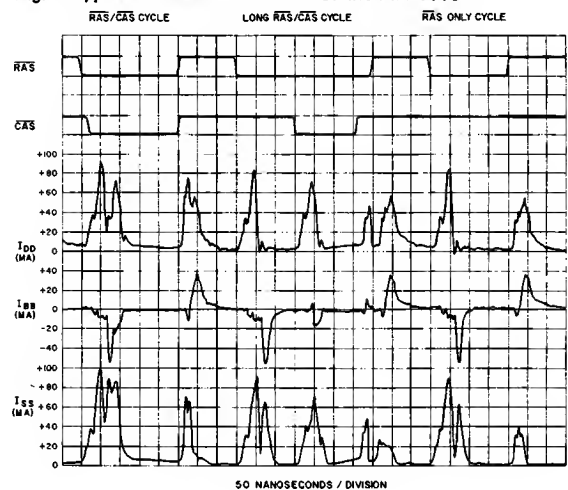
Most of the circuitry used in the MK 4332 is dynamic and most of the power drawn is the result of an address strobe edge. Consequently, the dynamic power is primarily a function of operating frequency rather than active duty cycle (refer to the MK 4116 current waveforms in figure 5). This current characteristic of the MK 4332 precludes inadvertent burn out of the device in the event that the clock inputs become shorted to ground due to system malfunction.

Although no particular power supply noise restriction exists other than the supply voltages remain within the specified tolerance limits, adequate decoupling should be provided to suppress high frequency noise resulting from the transient current of the device. This insures optimum system performance and reliability. Bulk capacitance requirements are minimal since the MK 4332 draws very little steady state (DC) current.

In system applications requiring lower power dissipation, the operating frequency (cycle rate) of the MK 4332 can be reduced and the (guaranteed maximum) average power dissipation of the device will be lowered in accordance with the IDD1 (max) spec limit curve illustrated in figure 2. NOTE: The MK 4332 family is guaranteed to have a maximum IDD1 requirement of 36.5mA @ 375ns cycle with an ambient temperature range from 0° to 70° C. A lower operating frequency, for example 1 microsecond cycle, results in a reduced maximum IDD1 requirement of under 20mA with an ambient temperature range from 0° to 70° C.

NOTE: Additional power supply tolerance has been included on the VBB supply to allow direct interface capability with both -5V systems -5.2V ECL systems.

Fig. 5 Typical Current Waveforms for the MK 4116



Although $\overline{\text{RAS}}$ and/or $\overline{\text{CAS}}$ can be decoded and used as a chip select signal for the MK 4116, overall system power is minimized if the Row Address Strobe ($\overline{\text{RAS}}$) is used for this purpose. All unselected devices (those which do not receive a $\overline{\text{RAS}}$) will remain in a low power (standby) mode regardless of the state of $\overline{\text{CAS}}$.

POWER UP

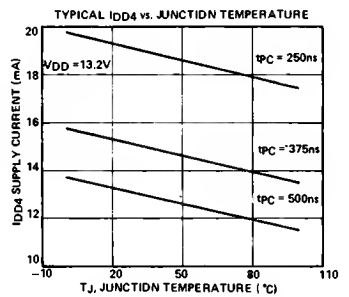
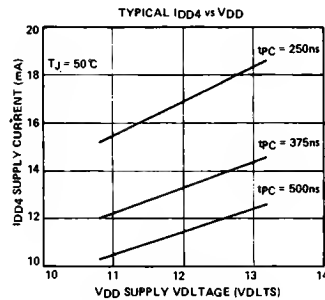
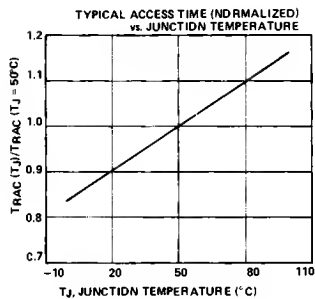
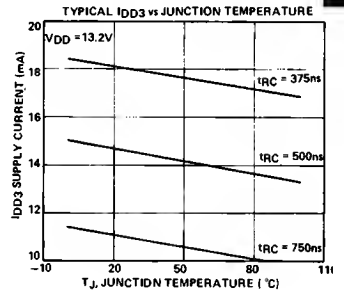
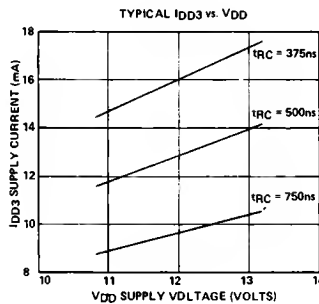
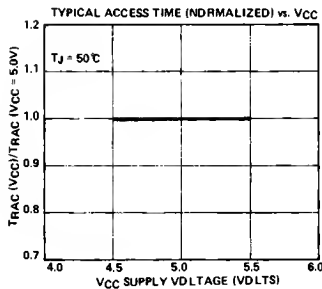
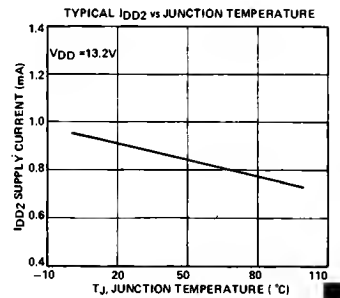
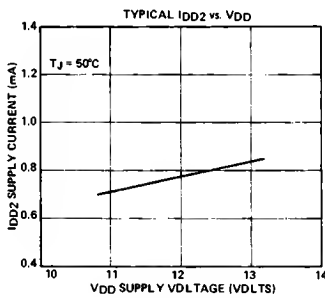
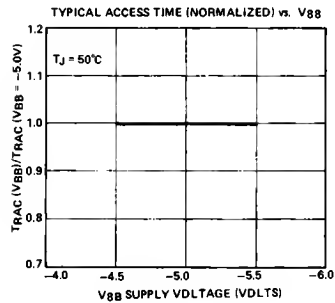
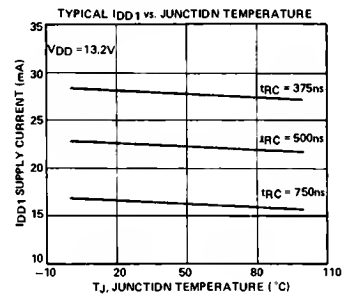
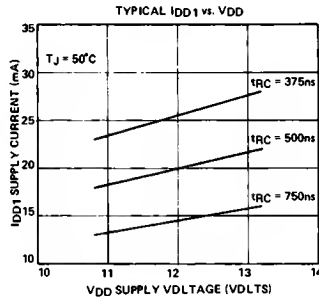
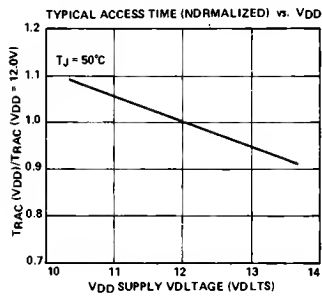
The MK 4332 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, MOSTEK recommends sequencing of power supplies

such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD} .

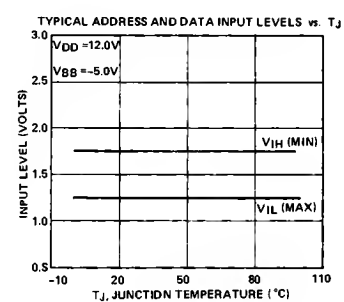
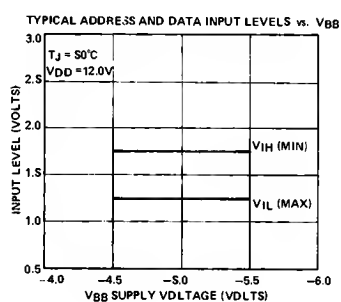
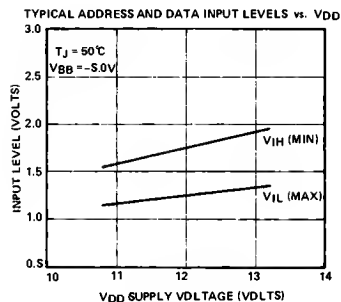
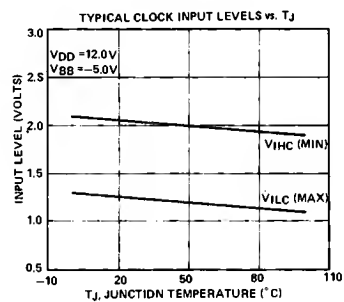
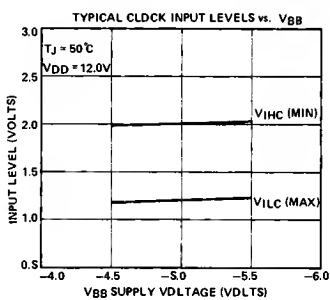
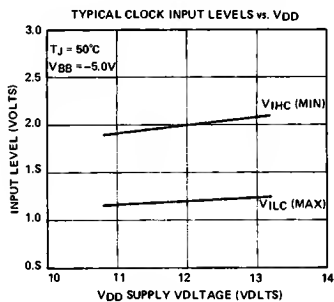
Under system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ to the inactive state (high level).

After power is applied to the device, the MK 4332 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose. Each MK 4116 device must receive the 8 initialization cycles.

TYPICAL CHARACTERISTICS OF THE MK 4116



DYNAMIC
RAMS



PRELIMINARY

MOSTEK®

65,536 x 1-BIT DYNAMIC RAM

MK4164(N/E)-12/15

FEATURES

- Recognized industry standard 16-pin configuration from Mostek
- Single +5V ($\pm 10\%$) supply operation
- On chip substrate bias generator for optimum performance
- Low power: 330mW active, max
22mW standby, max
- 120ns access time, 265ns cycle time (MK4164-12)
150ns access time, 325ns cycle time (MK4164-15)
- Indefinite $\overline{D_{OUT}}$ hold using \overline{CAS} control

DESCRIPTION

The MK4164 is the new generation dynamic RAM, organized 65,536 words by 1 bit, it is the successor to the industry standard MK4116. The MK4164 utilizes Mostek's Scaled Poly 5 process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Performance previously unachieved will be the standard for this new generation device. The use of dynamic circuitry throughout, including the 512 sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or internal and external operating margins. Refresh characteristics have been chosen to maximize yield (low cost to user) while maintaining compatibility between dynamic RAM generations.

Multiplexed address inputs (a feature dating back to the industry standard, MK4096, 1973) permits the MK4164 to be packaged in a standard 16-pin DIP with only 15 pins required for basic functionality. Mostek is utilizing this spare pin for a new refresh feature. The MK4164 is designed to be compatible with the JEDEC standards for the 64K x 1 dynamic RAM. The compatibility with the MK4516 (16K) will also permit a common board design to service both the MK4516 and MK4164 designs.

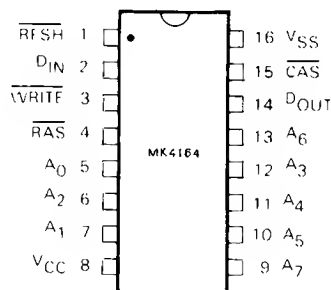
The output of the MK4164 can be held valid indefinitely by holding \overline{CAS} active low. This is quite useful since a refresh cycle can be performed while holding data valid from a previous cycle.

- Common I/O capability using "early write"
- Read, Write, Read-Write, Read-Modify-Write and Page-Mode capability
- All inputs TTL compatible, low capacitance, and are protected against static charge
- Scaled POLY 5 technology
- Pin compatible with the MK4516 (16K RAM)
- 128 refresh cycles (2msec)
Pin 9 is not needed for refresh
- Offers two variations of hidden refresh

The 64K RAM from Mostek is the culmination of several years of circuit and process development, proven in predecessor products.

DYNAMIC
RAMS

PIN OUT



PIN FUNCTIONS

A_0 A_7	Address Inputs	\overline{RAS}	Row Address Strobe
\overline{CAS}	Column Address Strobe	\overline{WRITE}	Read Write Input
D_{IN}	Data In	\overline{RFSH}	Refresh
D_{OUT}	Data Out	V_{CC}	Power ($\pm 5V$)
		V_{SS}	GND

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS}	-1.0V to +7.0V
Operating Temperature, T_A (Ambient)	0°C to +70°C
Storage Temperature (Ceramic)	-65°C to +150°C
Storage Temperature (Plastic)	-55°C to +125°C
Power Dissipation	1 Watt
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High (Logic 1) Voltage, All Inputs	2.4	—	$V_{CC}+1$	V	1
V_{IL}	Input Low (Logic 0) Voltage, All Inputs	-2.0	—	.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ± 10%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	OPERATING CURRENT $t_{RC} = 265\text{ns}$		60	mA	2
I_{CC2}	STANDBY CURRENT Power supply standby current ($\overline{RAS} = V_{IH}$, $D_{OUT} = \text{High Impedance}$)		4	mA	2
$I_{1(L)}$	INPUT LEAKAGE Input leakage current, any input (0V ≤ V_{IN} ≤ +5.5V, all other pins not under test = 0 volts)	-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V)	-10	10	μA	
V_{OH} V_{OL}	OUTPUT LEVELS Output High (Logic 1) voltage ($I_{OUT} = -5\text{mA}$) Output Low (Logic 0) voltage ($I_{OUT} = 4.2\text{mA}$)	2.4	0.4	V V	

NOTES:

1. All voltages referenced to V_{SS} .
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
3. An initial pause of 100μs is required after power-up followed by an 8 \overline{RAS} or \overline{RFSH} cycles before proper device operation is achieved. If refresh counter is to be effective a minimum of 64 active \overline{RFSH} initialization cycles is required. The internal refresh counter must be activated a minimum of 128 times every 2ms if the \overline{RFSH} refresh function is used.
4. AC characteristics assume $t_r = 5\text{ns}$.
5. V_{IH} min. and V_{IL} max. are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} .
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Load = 2 TTL loads and 50 pF.
8. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
10. $\overline{RFSH} = V_{IH}$ or V_{IL} , but is allowed to make an active to inactive transition during the \overline{RAS} active time of \overline{RAS} - only refresh cycle. $\overline{WRITE} = \text{don't care}$. Data out depends on the state of \overline{CAS} . If $\overline{CAS} = V_{IH}$, data output is high impedance. If $\overline{CAS} = V_{IL}$, the data output will contain data from the last valid read cycle.
11. $\overline{RAS} = V_{IH}$. $\overline{CAS} = V_{IH}$ or V_{IL} , but is allowed to make an active to inactive transition during the Pin 1 refresh cycle. $\overline{ADDRESSES}$ and $\overline{WRITE} = \text{don't care}$. Data out depends on the state of \overline{CAS} . If $\overline{CAS} = V_{IH}$, data output is high impedance. If $\overline{CAS} = V_{IL}$, the data output will contain data from the last valid read cycle.

NOTES Continued:

12. t_{OFF} max defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
13. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to \overline{CAS} leading edge in early write cycles and to \overline{WRITE} leading edge in delayed write or read-modify-write cycles.

16. t_{WCS} , t_{CWD} , and t_{RWD} are restrictive operating parameters in READ/WRITE and READ/MODIFY/WRITE cycles only. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) the cycle is a READ/WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the condition of the data out (at access time and until \overline{CAS} goes back to V_{IH}) is indeterminate.
17. If the \overline{RFSH} function is not used, pin 1 may be left open (no connect).
18. The transition time specification applies for all inputs signals. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(3,4,5,10,11,17,18) ($0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$), $V_{CC} = 5.0\text{V} \pm 10\%$

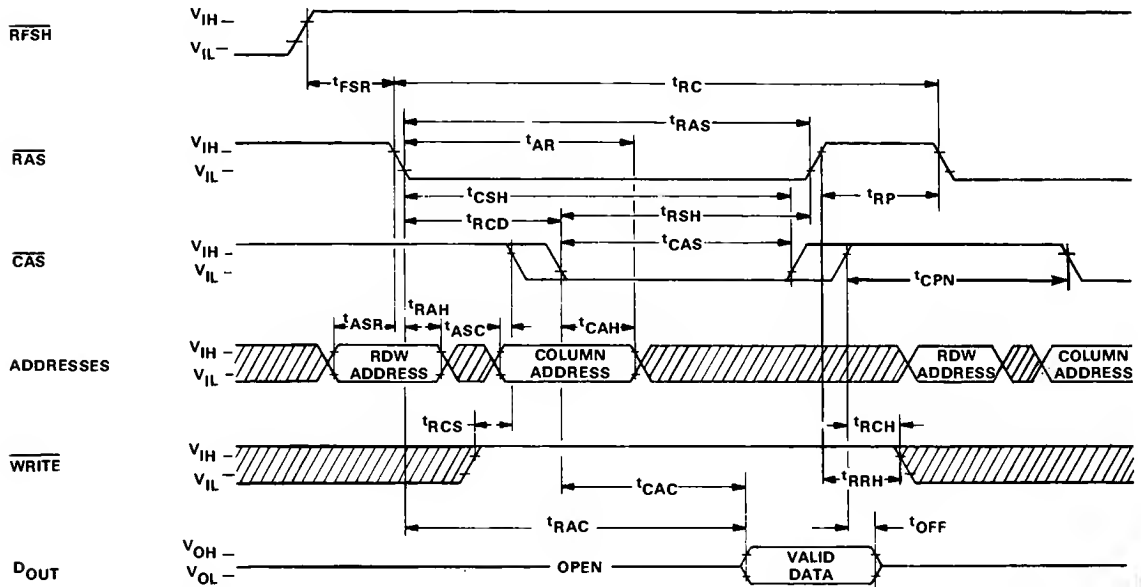
SYM	PARAMETER			MK4164-12		MK4164-15		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random read or write cycle time			265		325		ns	6,7
t_{RMW}	Read modify write cycle time			310		380		ns	6,7
t_{PC}	Page mode cycle time			140		165		ns	6,7
t_{RAC}	Access time from \overline{RAS}				120		150	ns	7,8
t_{CAC}	Access time from \overline{CAS}				60		75	ns	7,9
t_{OFF}	Output buffer turn-off delay			0	35	0	40	ns	12
t_T	Transition time (rise and fall)			3	50	3	50	ns	5,18
t_{RP}	\overline{RAS} precharge time			135		165		ns	
t_{RAS}	\overline{RAS} pulse width			120	10,000	150	10,000	ns	
t_{RSH}	\overline{RAS} hold time			60		75		ns	
t_{CSH}	\overline{CAS} hold time			120		150		ns	
t_{CAS}	\overline{CAS} pulse width			60	∞	75	∞	ns	
t_{RCD}	\overline{RAS} to \overline{CAS} delay time			20	60	20	75	ns	13
t_{RRH}	Read command hold time referenced to \overline{RAS}			25		30		ns	14
t_{ASR}	Row address set-up time			0		0		ns	
t_{RAH}	Row address hold time			15		20		ns	
t_{ASC}	Column address set-up time			0		0		ns	
t_{CAH}	Column address hold time			20		45		ns	
t_{AR}	Column address hold time referenced to \overline{RAS}			80		120		ns	
t_{RCS}	Read command set-up time			0		0		ns	
t_{RCH}	Read command hold time referenced to \overline{CAS}			0		0		ns	14
t_{WCH}	Write command hold time			40		50		ns	

DYNAMIC
RAMS

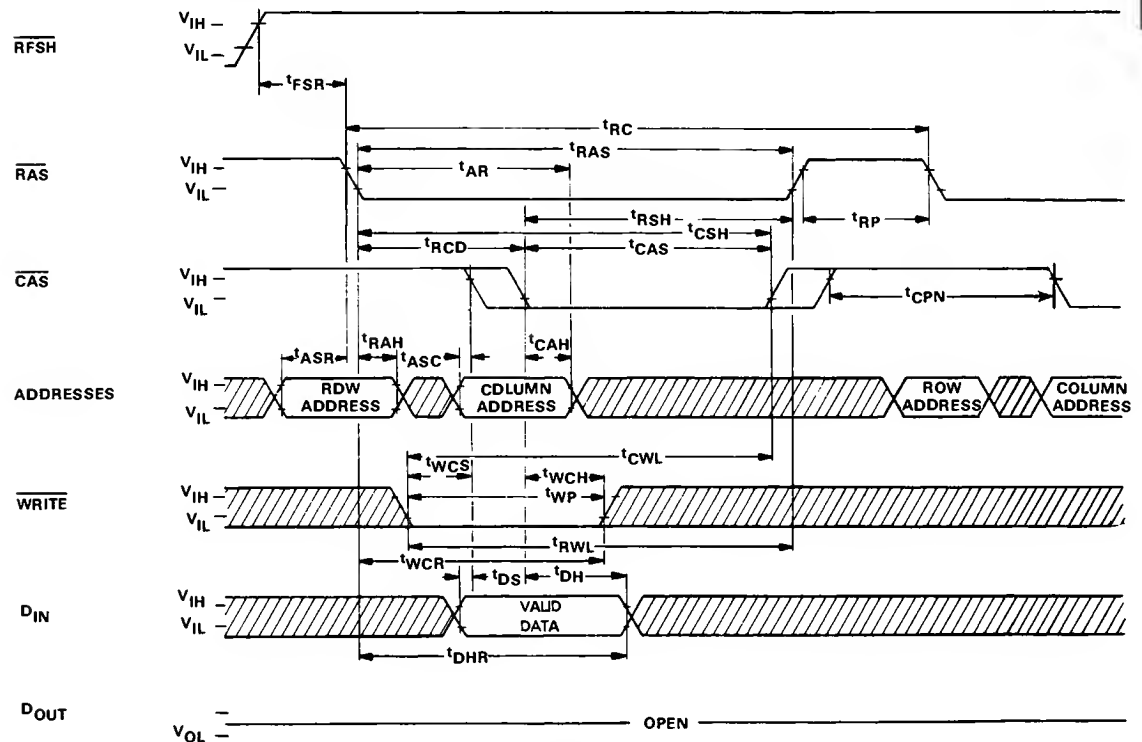
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)
(3,4,5,10,11,17,18) ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$), $V_{CC} = 5.0\text{V} \pm 10\%$

SYM	PARAMETER			MK4164-12		MK4164-15		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WCR}	Write command hold time referenced to $\overline{\text{RAS}}$			100		125		ns	
t_{WP}	Write command pulse width			35		45		ns	
t_{RWL}	Write command to $\overline{\text{RAS}}$ lead time			40		50		ns	
t_{CWL}	Write command to $\overline{\text{CAS}}$ lead time			40		50		ns	
t_{DS}	Data-in set-up time			0		0		ns	15
t_{DH}	Data-in hold time			40		45		ns	15
t_{DHR}	Data-in hold time referenced to $\overline{\text{RAS}}$			100		125		ns	
t_{CP}	$\overline{\text{CAS}}$ precharge time (for page-mode cycle only)			70		80		ns	
t_{REF}	Refresh Period				2		2	ms	
t_{WCS}	WRITE command set-up time			0		0		ns	16
t_{CWD}	$\overline{\text{CAS}}$ to WRITE delay			60		75		ns	16
t_{RWD}	$\overline{\text{RAS}}$ to WRITE delay			120		150		ns	16
t_{FSR}	$\overline{\text{RFSH}}$ set-up time referenced to $\overline{\text{RAS}}$			135		165		ns	
t_{RFD}	$\overline{\text{RAS}}$ to $\overline{\text{RFSH}}$ delay			135		165		ns	
t_{FC}	$\overline{\text{RFSH}}$ cycle time			265		325		ns	
t_{FP}	$\overline{\text{RFSH}}$ active time			120		150		ns	
t_{FI}	$\overline{\text{RFSH}}$ inactive time			135		165		ns	
t_{CPN}	$\overline{\text{CAS}}$ precharge time			30		40		ns	

READ CYCLE

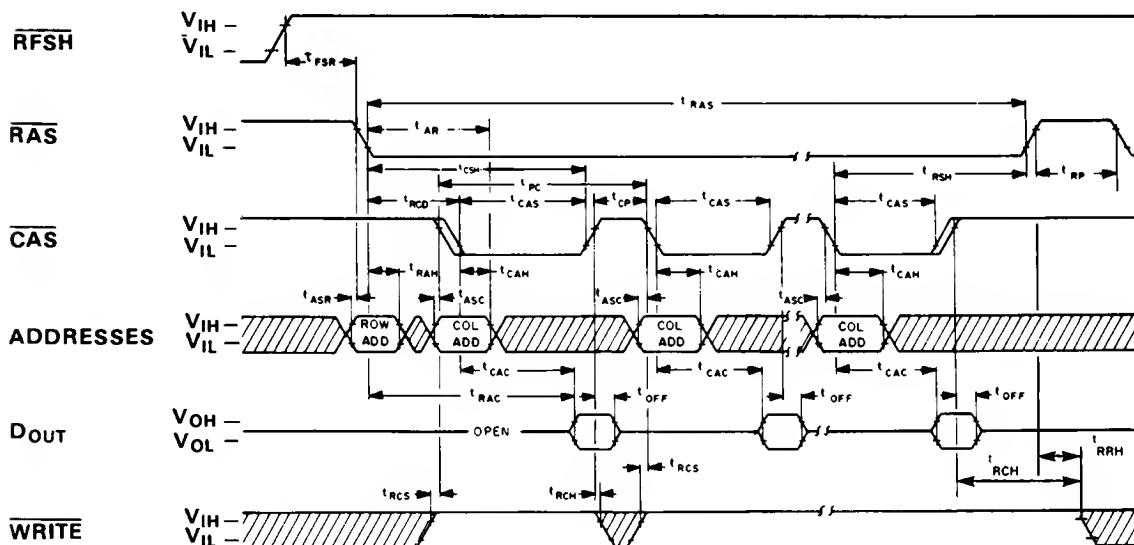


WRITE CYCLE (EARLY WRITE)

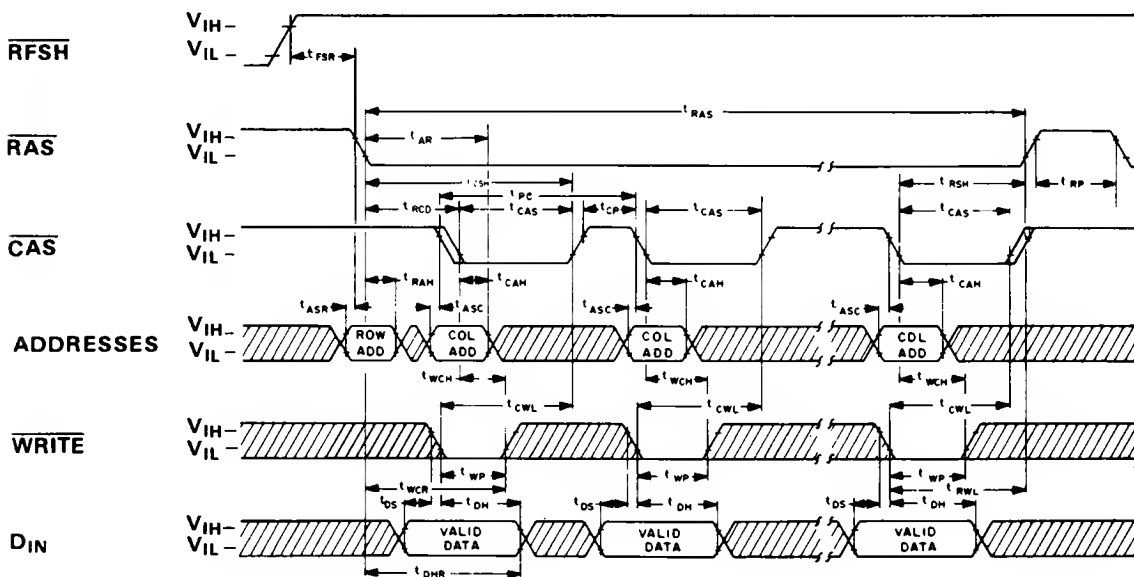


DYNAMIC
RAMS

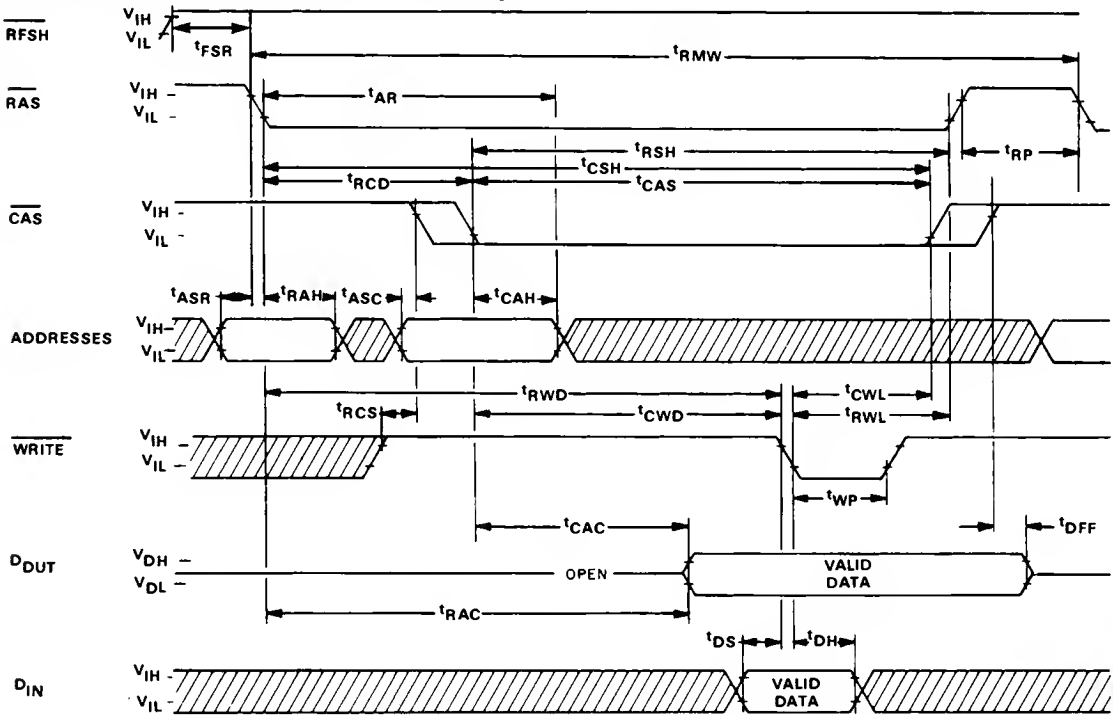
PAGE MODE READ CYCLE



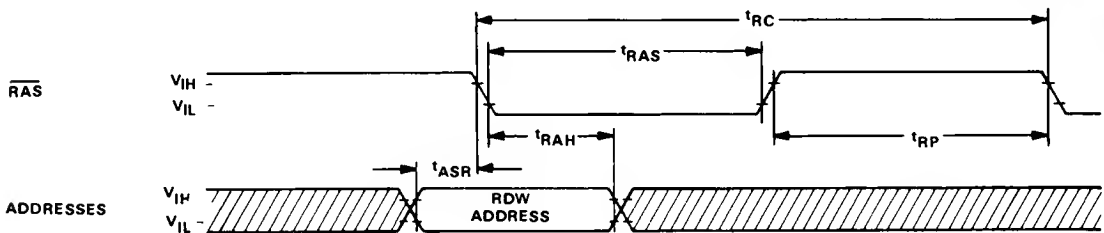
PAGE MODE WRITE CYCLE



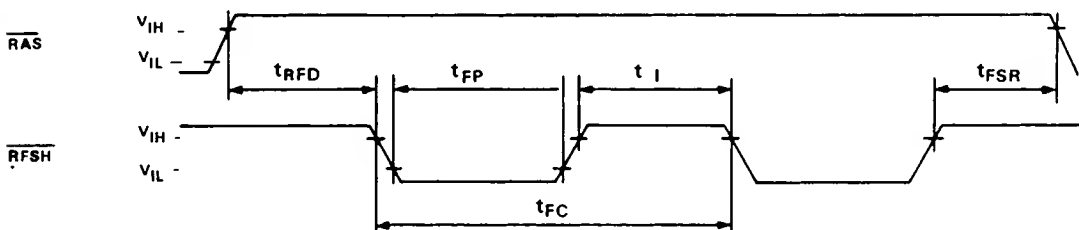
READ—WRITE/READ—MODIFY—WRITE CYCLE



"RAS—ONLY" REFRESH CYCLE (SEE NOTE 10)



RFSH (PIN 1) REFRESH CYCLE (SEE NOTE 11)



OPERATION

The 16 address bits required to decode 1 of the 65,536 cell locations within the MK4164 are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, Row Address Strobe (RAS), latches the 8 row addresses into the chip. The high-to-low transition of the second clock, Column Address Strobe (CAS), subsequently latches the 8 column addresses into the chip. Each of these signals, RAS and CAS, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical timing path for read data access. The later events in the CAS clock sequence are inhibited until the occurrence of a delayed signal derived from the RAS clock chain. The "gated CAS" feature allows the CAS clock to be externally activated as soon as the Row Address Hold specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

The "gated CAS" feature permits CAS to be activated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of CAS which are called $t_{RCD}(\min)$ and $t_{RCD}(\max)$. No data storage or reading errors will result if CAS is applied to the MK4164 at a point in time beyond the $t_{RCD}(\max)$ limit. However, access time will then be determined exclusively by the access time from CAS (t_{CAS}) rather than from RAS (t_{RAS}), and RAS access time will be lengthened by the amount that t_{RCD} exceeds the $t_{RCD}(\max)$ limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of WRITE and CAS while RAS is active. The latter of WRITE or CAS to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the WRITE input is brought low (active) prior to CAS being brought low (active), the D_{IN} is strobed by CAS, and the Input Data set-up and hold times are referenced to CAS. If the input data is not available at CAS time (late write) or if it is desired that the cycle be a read-write or read-modify-write cycle the WRITE signal should be delayed until after CAS has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of WRITE rather than CAS.

Data is retrieved from the memory in a read cycle by maintaining WRITE in the inactive or high state throughout the portion of the memory cycle in which both the RAS and CAS are low (active). Data read from the selected cell is available at the output port within the specified access time. The output data is the same polarity (not inverted) as the input data.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the MK4164 is the high impedance (open-circuit) state; anytime CAS is high (inactive) the D_{OUT} pin will be floating. Once the output data port has gone active, it will remain valid until CAS is taken to the precharge (inactive high) state. Note that CAS can be left active (low) indefinitely. This permits either RAS-only or RFSH refresh cycles to occur without invalidating D_{OUT} .

PAGE MODE OPERATION

The Page Mode feature of the MK4164 allows for successive memory operations at multiple column locations within the same row address. This is done by strobing the row address into the chip and maintaining the RAS signal low (active) throughout all successive memory cycles in which the row address is common. The first access within a page mode operation will be available at t_{RAC} or t_{CAC} time, whichever is the limiting parameter. However, all successive accesses within the page mode operation will be available at t_{CAC} time (referenced to CAS). With the MK4164, this results in as much as a 50% improvement in access times! Effective memory cycle times are also reduced when using page mode.

The page mode boundary of a single MK4164 is limited to the 256 column locations determined by all combinations of the 8 column address bits. Operations within the page boundary need not be sequentially addressed and any combination of read, write, and read-modify-write cycles are permitted within the page mode operation.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2ms interval. Although any normal memory cycle will perform the required refreshing, this function is easily accomplished by using either RAS-only or RFSH type refreshing.

RAS-ONLY REFRESH

The RAS-only refresh cycle supported by the MK4164 requires that a 7 bit refresh address be valid at the

device address inputs when RAS goes low (active). The state of the output data port during a RAS-only refresh is controlled by CAS. If CAS is high (inactive) during the entire time that RAS is asserted, the output will remain in the high impedance state. If CAS is low (active) the entire time that RAS is asserted, the output port will remain in the same state that it was prior to the issuance of the RAS signal. This is useful for single step operation. If CAS makes a low-to-high transition during the RAS-only refresh cycle, the output data buffer will assume the high impedance state.

PIN 1 REFRESH

RFSH type refreshing available on the MK4164 offers an attractive alternate refresh method. When the signal on pin 1, RFSH, is brought low during RAS inactive time (RAS high), an on-chip refresh counter is enabled and an internal refresh operation takes place. When RFSH is brought high (inactive) the internal refresh address counter is automatically incremented in preparation for the next refresh cycle. Data can be held valid from a previous cycle using CAS control during a RFSH type refresh cycle.

The internal refresh counter is a dynamic counter and requires refreshing. The 128 RFSH cycles every 2 milliseconds required to refresh the memory cells is adequate for this purpose. Only RFSH activated cycles affect the internal counter.

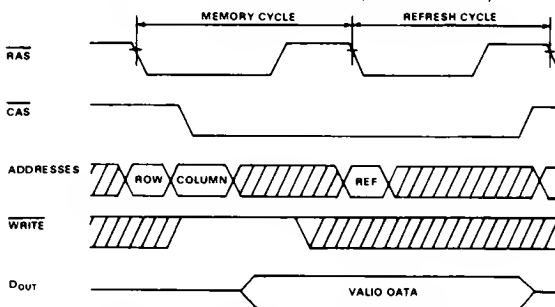
The use of RFSH mode for refreshing eliminates the need to generate refresh addresses externally. Furthermore, when using RFSH refreshing, the address drivers, the CAS drivers, and WRITE drivers can be powered down during battery backup standby operation.

HIDDEN REFRESH

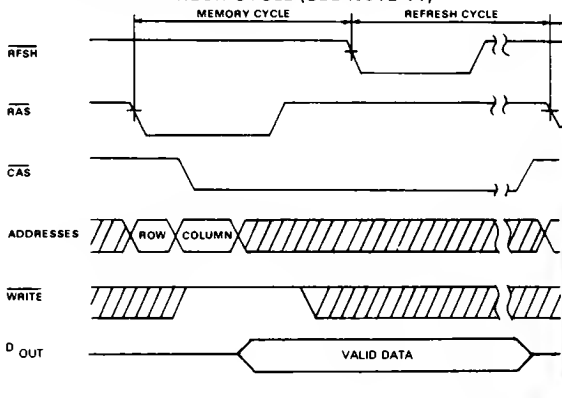
Either a RAS-only or RFSH type refresh cycle may take place while maintaining valid output data by extending the CAS active time from a previous memory read cycle.

This feature is referred to as a hidden refresh. (See figures below.)

HIDDEN $\overline{\text{RAS}}$ -ONLY REFRESH CYCLE (SEE NOTE 10)



HIDDEN RFSH REFRESH CYCLE (SEE NOTE 11)



DYNAMIC
RAMS

RFSH (PIN 1) TEST CYCLE

A special timing sequence using the PIN 1 counter test cycle provides a convenient method of verifying the functionality of the RFSH activated circuitry.

This special test sequence will be announced at a later date.

1980 MEMORY DATA BOOK

I	Table of Contents	TABLE OF CONTENTS
II	Order Information Packaging	ORDER PKG INFORM
III	Sales Office Locations	SALES OFFICES
IV	Read Only Memory	ROMS
V	Dynamic Random Access Memory	DYNAMIC RAMS
VI	Static Random Access Memory	STATIC RAMS
VII	Pseudostatic Random Access Memory	PSEUDO RAMS
VIII	Military/Hi-Rel	MILITARY/ HI-REL
IX	Military/Hi-Rel Products	MILITARY/ HI-REL PRODUCTS

PRELIMINARY

MOSTEK®

4K x 1-BIT STATIC RAM MK2147(J)-55/70/85

FEATURES

- ☐ Scaled Poly 5™ technology
- ☐ Industry standard 18-pin dip configuration
- ☐ High performance

			Power Supply Current	
Part Number	Access Time	Cycle Time	Max. Active	Max. Standby
MK2147-55	55ns	55ns	180mA	30mA
MK2147-70	70ns	70ns	160mA	20mA
MK2147-85	85ns	85ns	160mA	20mA

- ☐ Address Activated™ static memory—no clock or timing strobe required
- ☐ Access time equal cycle time
- ☐ Chip select power down feature
- ☐ Single +5V (±10%) power supply
- ☐ On-chip substrate bias generator
- ☐ All inputs are low capacitance and TTL compatible
- ☐ Three-state TTL compatible output

DESCRIPTION

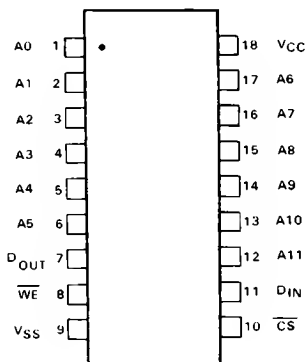
The MK2147 uses MOSTEK's Scaled Poly 5™ process and advanced circuit design techniques to package 4096 words by 1-bit of static RAM on a single chip requiring a single +5 volt supply. The MK2147 is functionally equivalent and pin compatible with the established industry standard 18-pin high performance 4K x 1 static RAM.

MOSTEK's Address Activated™ circuit design technique is utilized to achieve high performance, low

power, and easy user implementation. The device has a $V_{IH} = 2.0V$, $V_{IL} = 0.8V$, $V_{OH} = 2.4V$, and $V_{OL} = 0.4V$ making it totally compatible with all TTL family devices. The MK2147 has a chip select power down feature which automatically reduces the power dissipation when the chip select, \overline{CS} , is brought inactive (high).

The MK2147 is designed for memory applications that require high bit densities, fast access, and short cycle times. The MK2147 offers the user a high density cost effective alternative to bipolar and previous generation N-MOS fast memory.

PIN CONNECTION



PIN NAMES

A0 - A11	ADDRESS INPUTS
\overline{CS}	CHIP SELECT
DIN	DATA INPUT
DOUT	DATA OUTPUT
VSS	GROUND
VCC	POWER (+5V)
\overline{WE}	WRITE ENABLE

TRUTH TABLE

CS	WE	MODE	OUTPUT	POWER
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	DOUT	Active

STATIC
RAMS

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to VSS	-1.5V to +7.0V
Temperature Under Bias	-10°C to +85°C
Storage temperature (Ambient) (Ceramic)	-65°C to +150°C
D.C. output current	20mA
Power dissipation	1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹

(0 ≤ TA ≤ 70°C)**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V _{CC}	Supply Voltage	4.5	5.0	5.5	Volts	1
V _{SS}	Supply Voltage	0	0	0	Volts	1
V _{IH}	Logic "1" Voltage All Inputs	2.0		V _{CC} + 1	Volts	1
V _{IL}	Logic "0" Voltage All Inputs	-1.0		0.8	Volts	1

DC ELECTRICAL CHARACTERISTICS¹

(0°C ≤ TA ≤ +70°C) ** (V_{CC} = 5.0 volts ±10%)

		MK2147-55		MK2147-70		MK2147-85			
	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
I _{CC}	Operating Current		180		160		160	mA	Out-put Open
I _{SB}	Standby Current		30		20		20	mA	
I _{PO}	Peak Power-on Current		70		50		30	mA	14
I _L	Input Leakage Current (Any Input)		10		10		10	μA	2
I _{OL}	Output Leakage Current		50		50		50	μA	2
V _{OH}	Output Logic "1" Voltage I _{OUT} = -4mA	2.4		2.4		2.4		V	
V _{OL}	Output Logic "0" Voltage I _{OUT} = 8mA		0.4		0.4		0.4	V	

AC ELECTRICAL CHARACTERISTICS¹

(0° C ≤ TA ≤ + 70° C)** (V_{CC} = +5.0 volts ±10%)

	PARAMETER	TYP	MAX	NOTES
C _{IN}	Input Capacitance		5Pf	12
C _{OUT}	Output Capacitance		7Pf	12, 13

**The operating ambient temp. range is guaranteed with transverse air flow exceeding 400 Linear feet per minute.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS^{3,4}
(0°C ≤ TA ≤ 70°C) (VCC = 5.0 volts ± 10%)**

SYMBOL	PARAMETER	MK2147-55		MK2147-70		MK2147-85		UNIT	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX		
tRC	Read Cycle Time	55		70		85		ns	
tAA	Address Access Time		55		70		85	ns	5
tCSA1	Chip Select Access Time		55		70		85	ns	5,7
tCSA2	Chip Select Access Time		65		80		85	ns	5,8
tOH	Output Hold From Address Change	5		5		5		ns	
tLZ	Chip Selection to Output Low Z	10		10		10		ns	
tHZ	Chip Deselection to Output High Z	0	40	0	40	0	40	ns	6
tPU	Chip Selection to Power Up Time	0		0		0		ns	
tPD	Chip Deselection to Power Down		30		30		30	ns	
tWC	Write Cycle Time	55		70		85		ns	
tCW	Chip Select to End of Write	45		55		65		ns	
tAW	Address Valid to End of Write	45		55		65		ns	
tAS	Address Setup Time	0		0		0		ns	
tWP	Write Pulse Width	35		40		45		ns	
tWR	Write Recovery Time	10		15		20		ns	
tDW	Data Valid to End of Write	25		30		30		ns	
tDH	Data Hold Time	10		10		10		ns	
tWZ	Write Enable to Output in High Z	0	30	0	35	0	40	ns	6
tOW	Output Active From End of Write	0		0		0		ns	

STATIC
RAMS

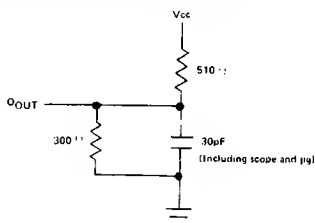
NOTES:

1. All voltages referenced to VSS.
2. Measured with $0 \leq V_I \leq 5V$ and output deselected.
3. AC measurements assume $t_T = 10ns$, levels VSS to 3.5V
4. Input and output timing reference levels are at 1.5V.
5. Measured with a load as shown in Figure 1.
6. tHZ and tWZ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. Chip deselected for greater than 55ns prior to selection.

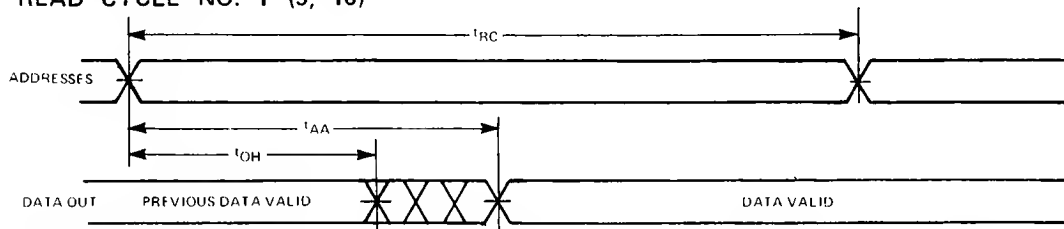
8. Chip deselected for a finite time that is less than 55ns prior to selection. (If the deselect time is 0ns, the chip is by definition selected and access occurs according to Read Cycle No. 1).
9. WE is high for Read Cycles.
10. Device is continuously selected $\overline{CS} \leq V_{IL}$
11. Addresses valid prior to or coincident with \overline{CS} transition low.
12. Effective capacitance calculated from the equation $C = \frac{I \Delta t}{\Delta V}$ with $\Delta V = 3$ volts and power supplies at nominal levels.
13. Output buffer is deselected.
14. VCC = VSS to VCC min.
CS = lower of VCC or VIH min.

OUTPUT LOAD

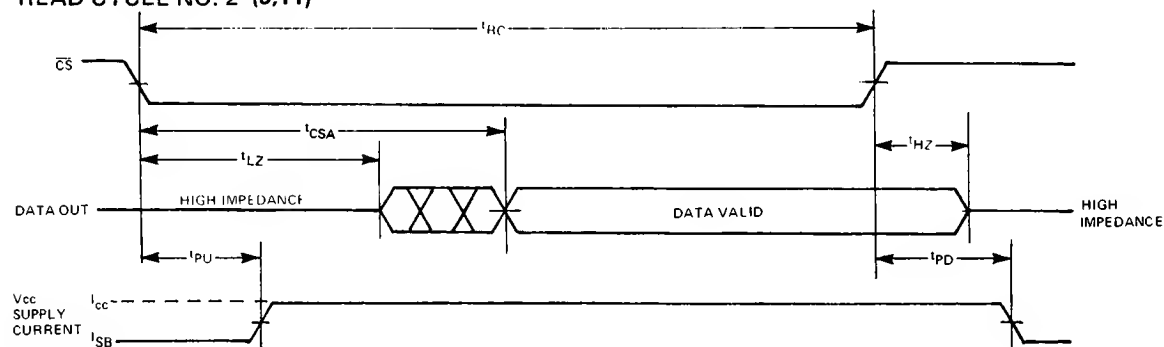
Figure 1



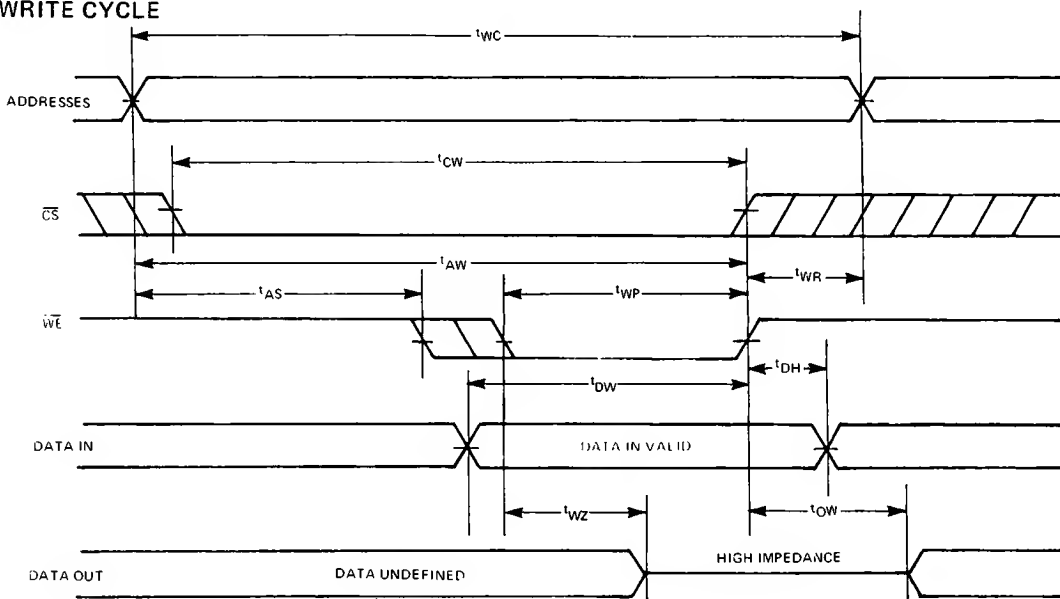
READ CYCLE NO. 1 (9, 10)



READ CYCLE NO. 2 (9,11)



WRITE CYCLE



MOSTEK®

4096x1-BIT STATIC RAM MK4104(J/N/E) Series

FEATURES

- ☐ Combination static storage cells and dynamic control circuitry for truly high performance
- ☐ Standby Power Dissipation less than 28 mW (at $V_{CC} = 5.5V$)
- ☐ Single +5V Power Supply ($\pm 10\%$ tolerance)
- ☐ Fully TTL Compatible
 - Fanout: 2 – Standard TTL
 - 2 – Schottky TTL
 - 12 – Low Power Schottky TTL
- ☐ Standard 18-pin DIP
- ☐ Low Active Power Dissipation: 150mW (Max)
- ☐ Battery backup mode (3V/10mW on -33, -34 and -35)

DESCRIPTION

The MOSTEK MK 4104 is a high performance static random access memory organized as 4096 one bit words. The MK 4104 combines the best characteristics of static and dynamic memory techniques to achieve a TTL compatible, 5 volt only, high performance, low power memory device. It utilizes advanced circuit design concepts and an innovative state-of-the-art N-channel silicon gate process specially tailored to provide static data storage with the performance (speed and power) of dynamic RAMs. Since the storage cell is static the device may be stopped indefinitely with the \overline{CE} clock in the off (Logic 1) state.

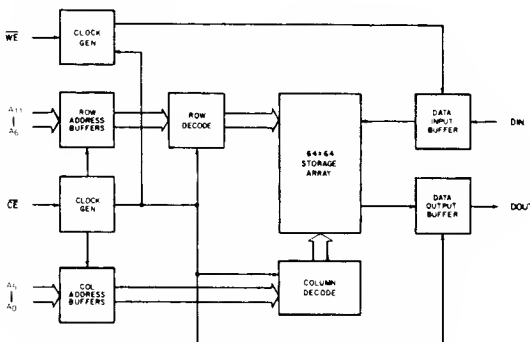
All input levels, including write enable (\overline{WE}) and chip enable (\overline{CE}) are TTL compatible with a one level of

2.2 volts and a zero level of 0.8 volts. This gives the system designer for a logic "1" state, at least 200mV of noise margin when driven by standard TTL and a minimum of 500mV when used with high performance Schottky TTL. These margins are wider than on most TTL compatible MOS memories available. The push-pull output (no pull-up resistor required) delivers a one level of 2.4V minimum and a zero level of .4 volts maximum. The output has a fanout of 2 standard TTL loads or 12 low power Schottky loads.

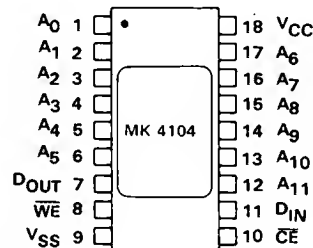
The RAM employs an innovative static cell which occupies a mere 2.75 square mils ($\frac{1}{2}$ the area of previous cells) and dissipates power levels comparable

STATIC
RAMS

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0 - A_{11}	Address Inputs	V_{SS}	Ground
\overline{CE}	Chip Enable	V_{CC}	Power (+5V)
D_{IN}	Data Input	\overline{WE}	Write Enable
D_{OUT}	Data Output		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V _{SS}	–1.0V to +7.0V
Operating Temperature T _A (Ambient)	0° C to +70° C
Storage Temperature (Ambient) (Ceramic)	–65° C to +150° C
Storage Temperature (Ambient) (Plastic)	–55° C to +125° C
Power Dissipation	1 Watt
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS⁶

(0° C ≤ T_A ≤ +70° C)

	PARAMETER	MK4104 Series			UNITS	NOTES
		MIN	TYP	MAX		
V _{CC}	Supply Voltage	4.5	5.0	5.5	Volts	1
V _{SS}	Supply Voltage	0	0	0	Volts	1
V _{IH}	Logic "1" Voltage All Inputs	2.2		7.0	Volts	1
V _{IL}	Logic "0" Voltage All Inputs	–1.0		.8	Volts	1

DC ELECTRICAL CHARACTERISTICS¹

(0° C ≤ T_A ≤ +70° C) (V_{CC} = 5.0 volts ± 10%)

	PARAMETER	MIN	MAX	UNITS	NOTES
I _{CC1}	Average V _{CC} Power Supply Current		27	mA	2
I _{CC2}	Standby V _{CC} Power Supply Current		5	mA	3
I _{IL}	Input Leakage Current (Any Input)	–10	10	μA	4
I _{OL}	Output Leakage Current	–10	10	μA	3, 5
V _{OH}	Output Logic "1" Voltage I _{OUT} = –500μA	2.4		Volts	
V _{OL}	Output Logic "0" Voltage I _{OUT} = 5mA		0.4	Volts	

AC ELECTRICAL CHARACTERISTICS¹

(0° C ≤ T_A ≤ +70° C) (V_{CC} = + 5.0 volts ± 10%)

	PARAMETER	TYP	MAX	NOTES
C _I	Input Capacitance	4pF	6pF	14
C _O	Output Capacitance	6pF	7pF	14

NOTES:

- All voltages referenced to V_{SS}.
- I_{CC1} is related to precharge and cycle times. Guaranteed maximum values for I_{CC1} may be calculated by:

$$I_{CC1} \text{ (ma)} = (5t_p + 15(t_C - t_p) + 4720) \div t_C$$
 where t_p and t_C are expressed in nanoseconds. Equation is referenced to the -3 device, other devices derate to the same curve. Data outputs open.
- Output is disabled (open circuit), \overline{CE} is at logic 1.
- All device pins at 0 volts except pin under test at 0 ≤ V_{IN} ≤ 5.5 volts. (V_{CC} = 5V)
- 0V ≤ V_{OUT} ≤ 5.5V. (V_{CC} = 5V)
- During power up, \overline{CE} and \overline{WE} must be at V_{IH} for minimum of 2ms after V_{CC} reaches 4.5V, before a valid memory cycle can be accomplished.
- Measured with load circuit equivalent to 2 TTL loads and CL = 100 pF.
- If \overline{WE} follows \overline{CE} by more than t_{WGS} then data out may not remain open circuited.
- Determined by user. Total cycle time cannot exceed t_{CE} max.
- Data-in set-up time is referenced to the later of the two falling clock edges \overline{CE} or \overline{WE} .
- AC measurements assume t_T = 5ns. Timing points are taken at .8V and 2.0V on inputs and .8V and 2.0V on the output. Transition times are also taken between these levels.
- t_C = t_{CE} + t_p + 2t_T.
- The true level of the output in the open circuit condition will be determined totally by output load conditions. The output is guaranteed to be open circuit within t_{OFF}.
- Effective capacitance calculated from the equation $C = \frac{\Delta t}{\Delta V}$ with ΔV equal to 3V and V_{CC} nominal.
- t_{RMW} = t_{AC} + t_{WPL} + t_p + 3t_T + t_{MOD}

$(0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}) \quad (V_{CC} = +5.0 \text{ volts} \pm 10\%)^1$

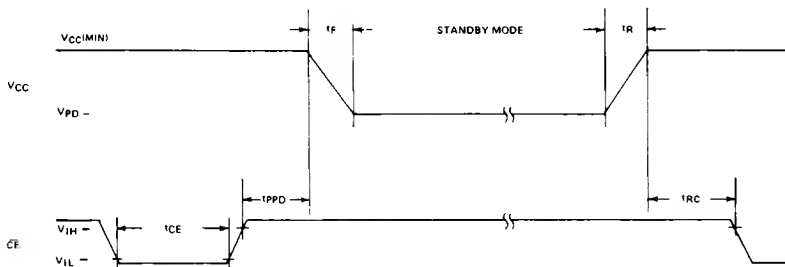
SYMBOL	PARAMETER	MK4104-3/33		MK4104-4/34		MK4104-5/35		MK4104-6		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
tC	Read or Write Cycle Time	310		385		460		535		ns	12
tAC	Random Access		200		250		300		350		7
tCE	Chip Enable Pulse Width	200	10,000	250	10,000	300	10,000	350	10,000		
tP	Chip Enable Precharge Time	100		125		150		175			
tAH	Address Hold Time	110		135		165		190			
tAS	Address Set-Up Time	0		0		0		0			
tOFF	Output Buffer Turn-Off Delay	0	50	0	65	0	75	0	100		13
tRS	Read Command Set-Up Time	0		0		0		0			8
tWS	Write Enable Set-Up Time	-20		-20		-20		-20			8
tDHC	Data Input Hold Time Referenced to \overline{CE}	170		210		250		285			
tDHW	Data Input Hold Time Referenced to \overline{WE}	70		90		105		125			
tWW	Write Enabled Pulse Width	60		75		90		105			
tMOD	Modify Time	0	10,000	0	10,000	0	10,000	0	10,000		9
tWPL	\overline{WE} to \overline{CE} Precharge Lead Time	70		85		105		120			10
tDS	Data Input Set-Up Time	0		0		0		0			
tWH	Write Enable Hold Time	150		185		225		260			
tT	Transition Time	5	50	5	50	5	50	5	50		
tRMW	Read-Modify-Write Cycle Time	385		475		570		660			16

STANDBY CHARACTERISTICS

 $(T_A = 0^\circ\text{C to } 70^\circ\text{C})$

SYMBOL	PARAMETER	MK4104-33		MK4104-34		MK4104-35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
V _{PD}	V _{CC} In Standby	3.0		3.0		3.0		Volts
I _{PD}	Standby Current		3.3		3.3		3.3	mA
t _F	Power Supply Fall Time	100		100		100		μsec
t _R	Power Supply Rise Time	100		100		100		μsec
t _{CE}	Chip Enable Pulse Width	200		250		300		μsec
t _{PPD}	Chip Enable Precharge To Power Down Time	100		125		150		nsec
V _{IH}	Min CE High "1" Level	2.2		2.2		2.2		Volts
t _{RC}	Standby Recovery Time	500		500		500		μsec

POWER DOWN WAVEFORM



to CMOS. The static cell eliminates the need for refresh cycles and associated hardware thus allowing easy system implementation.

ation, needed for Z80 interfacing, without external circuitry.

The MK4104-3X series has the added capability of retaining data in a reduced power mode. V_{CC} maybe lowered to 3V with a guaranteed power dissipation of only 10mW maximum. This makes the MK4104 ideal for those applications requiring data retention at the lowest possible power as in battery operation.

Reliability is greatly enhanced by the low power dissipation which causes a maximum junction rise of only at 8°C at 1.86 Megahertz operation. The MK 4104 was designed for the system designer and user who require the highest performance available along with MOSTEK's proven reliability.

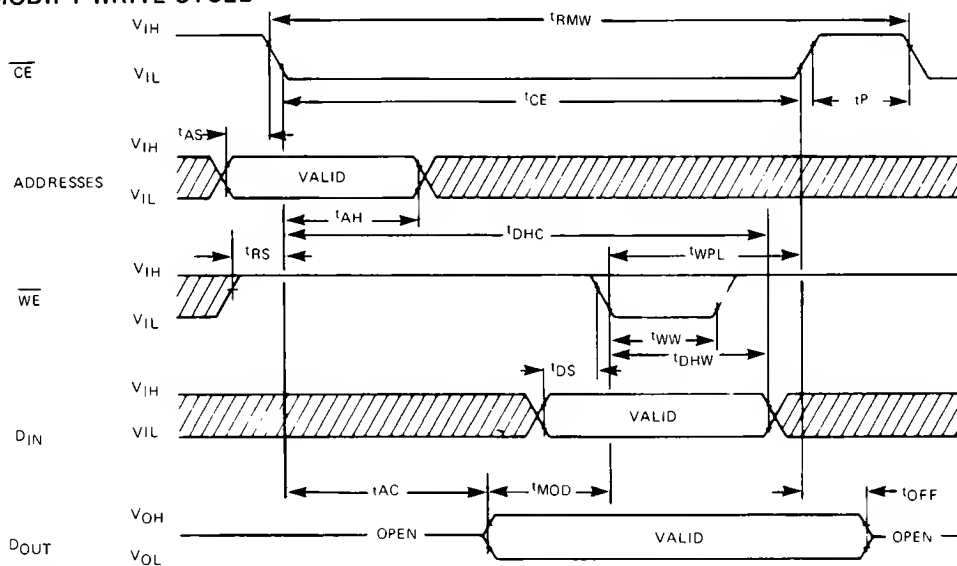
The diagram illustrates the timing relationships for the AD cycle. The signals shown are:

- CE**: Chip Enable, which transitions from high (V_{IH}) to low (V_{IL}) and back to high. The total duration of the low pulse is t_C . The time from the falling edge of CE to the start of valid data is t_{CE} . The time from the rising edge of CE to the end of valid data is t_P .
- ADDRESSES**: The address bus, which becomes valid (V_{IH} to V_{IL}) at time t_{AS} after the falling edge of CE. It remains valid for a duration t_{AH} after the rising edge of CE.
- WE**: Write Enable, which transitions from high (V_{IH}) to low (V_{IL}) and back to high. The time from the falling edge of WE to the start of valid data is t_{RS} .
- DIN**: Data Input, which is valid during the entire duration of the AD cycle.
- DOUT**: Data Output, which is in a high-impedance state (V_{OH} to V_{OL}) until t_{AC} after the falling edge of CE. It then becomes valid and remains valid for a duration t_{OFF} after the rising edge of CE.

The timing diagram illustrates the relationship between several control and data signals for the 28C01B EPROM. The signals shown are:

- CE** (Chip Enable): Transitions from high (V_{IH}) to low (V_{IL}) and back to high. Key timing parameters include t_C (total pulse width), t_{CE} (time from falling edge to output enable), and t_P (output delay after CE returns high).
- ADDRESSES**: A bus signal that becomes valid during the low pulse of CE. Timing parameters include t_{AS} (address setup time), t_{AH} (address hold time), and t_{WS} (write setup time).
- WE** (Write Enable): Transitions from high (V_{IH}) to low (V_{IL}) and back to high. Timing parameters include t_{WH} (write pulse width), t_{WPL} (write pulse period), and t_{DHC} (data hold time after write).
- DIN** (Data In): Becomes valid during the low pulse of CE. Timing parameters include t_{DS} (data setup time) and t_{DHW} (data hold time).
- DOUT** (Data Out): Shows output levels V_{OH} (high) and V_{OL} (low), and an "OPEN" state during the high pulse of CE.

READ-MODIFY-WRITE CYCLE



OPERATION

READ CYCLE

The circuit offers one bit of the possible 4096 by decoding the 12 address bits presented at the inputs. The address bits are strobed into the chip by the negative-going edge of the Chip Enable (\overline{CE}) clock. A read cycle is accomplished by holding the 'write enable' (\overline{WE}) input at a high level (V_{IH}) while clocking the \overline{CE} input to a low level (V_{IL}). At access time (t_{AC}) valid data will appear at the output. The output is unlatched by a positive transition of \overline{CE} and therefore will be open circuited (high impedance state) from the previous cycle to access time and will go open again at the end of the present cycle when \overline{CE} goes high.

Once the address hold time has been satisfied, the addresses may be changed for the next cycle.

WRITE CYCLE

Data that is to be written into a selected cell is strobed into the chip on the later occurring negative edge of \overline{CE} or \overline{WE} . If the negative transition of \overline{WE} occurs prior to the leading edge of \overline{CE} as in an "early" write cycle then the \overline{CE} input serves as the strobe for data-in. If \overline{CE} leading edge occurs prior to the leading edge of \overline{WE} as in a read-modify-write cycle then data-in is strobed by the \overline{WE} input. Due to the internal timing generator, two independent timing parameters must be satisfied for DI hold time, these are, t_{DHW} and t_{DHC} . For a R/W or RMW cycle t_{DHC} is automatically satisfied making t_{DHW} the more restrictive parameter. For a write only cycle either parameter can be more restrictive depending on the position of \overline{WE} relative to \overline{CE} . In any event both parameters must be satisfied.

In an 'early' write cycle the output will remain in an open or high impedance state. In a read-modify

write operation the output will go active through the modify and write period until \overline{CE} goes to precharge. If the cycle is such that \overline{WE} goes active after \overline{CE} but before valid data appears on the output (prior to t_{AC}) then the output may not remain open. However, if data-in is valid on the leading edge of \overline{WE} , and \overline{WE} occurs prior to the positive transition of \overline{CE} by the minimum lead time t_{WPL} , then valid data will be written into the selected cell. The Data in hold time parameters t_{DHW} and t_{DHC} must be satisfied.

READ-MODIFY-WRITE CYCLE

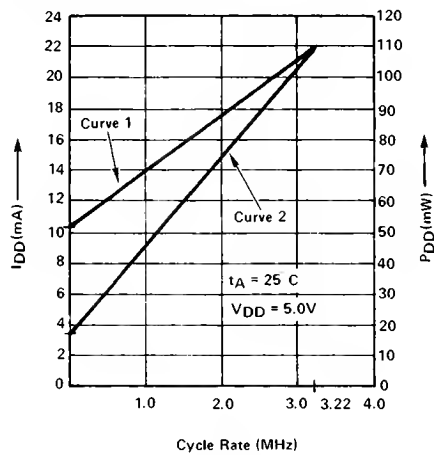
The read-modify-write (RMW) cycle is no more than an extension of the read and write cycles. Data is read at access time, modified during a period determined by the user and the same or new data written between \overline{WE} active (low) and the rising edge of \overline{CE} (t_{WPL}). Data out will remain valid until the rising edge of \overline{CE} . A minimum RMW cycle time can be approximated by the following equation (t_{RMW} = RMW cycle time and t_P = \overline{CE} precharge time).

$$t_{RMW} = t_{AC} + t_{MOD} + t_{WPL} + t_P + 3t_{\tau}$$

POWER DOWN MODE

In power down data may be retained indefinitely by maintaining V_{CC} at +3V. However, prior to V_{CC} going below V_{CC} minimum ($\leq 4.5V$) \overline{CE} must be taken high ($V_{IH} = 2.2V$) and held for a minimum time period t_{PPD} and maintained at V_{IH} for the entire standby period. After power is returned to V_{CC} min or above, \overline{CE} must be held high for a minimum of t_{RC} in order that the device may operate properly. See power down waveforms herein. Any active cycle in progress prior to power down must be completed so that t_{CE} min is not violated.

OPERATING POWER VS CYCLE TIME



Characterization data plot of frequency vs power dissipation for a typical MK4104 device.

Curve 1 - Clock on time (low level) is bottom scale minus 100 NSEC

Curve 2 - Clock off time (high level) is bottom scale minus 200 NSEC

MK4118(P/J/N) Series

FEATURES

□ Address Activated™ Interface combines benefits of Edge Activated™ and fully static operation

□ High performance

Part Number	Access Time	Cycle Time
MK4118-1	120 nsec	120 nsec
MK4118-2	150 nsec	150 nsec
MK4118-3	200 nsec	200 nsec
MK4118-4	250 nsec	250 nsec

□ Single +5 volt power supply

□ TTL compatible I/O

Fanout: 2 - Standard TTL
2 - Schottky TTL
12 - Low power Schottky TTL

□ Low Power - 400mw Active

□ \overline{CE} , \overline{OE} , and \overline{LATCH} functions for flexible system operation

□ Pin compatible with Mostek's BYTEWYDE™ memory family

DESCRIPTION

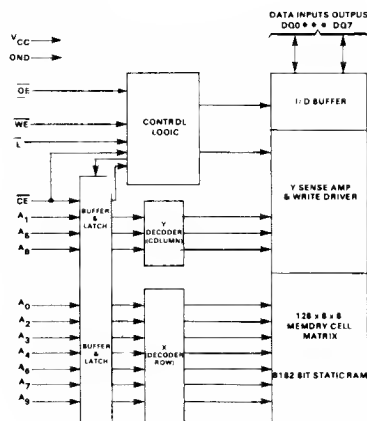
The MK4118 uses Mostek's Poly R N-Channel Silicon Gate process and advanced circuit design techniques to package 8192 bits of static RAM on a single chip. Mostek's Address Activated™ circuit design technique is utilized to achieve high performance, low power, and easy user implementation. The device has a $V_{IH} = 2.2$, $V_{IL} = 0.8V$, $V_{OH} = 2.4$, $V_{OL} = 0.4V$ making it totally compatible with all TTL family devices.

The MK4118 is designed for all wide word memory applications. The MK4118 provides the user with a

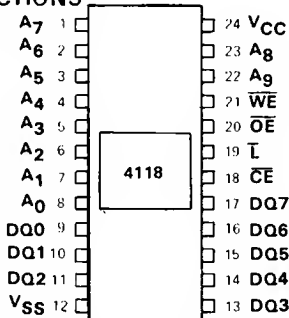
high-density, cost-effective 1K x 8-bit Random Access Memory. Fast Output Enable (\overline{OE}) and Chip Enable (\overline{CE}) controls are provided for easy interface in micro-processor or other bus-oriented systems. The MK4118 features a flexible Latch (\overline{L}) function to permit latching of the address and \overline{CE} status at the user's option. Common data and address bus operation may be performed at the system level by utilizing the \overline{L} and \overline{OE} functions for the MK4118. The latch function may be bypassed by merely tying the latch pin to V_{CC} , providing fast ripple-through operation.

STATIC
RAMS

BLOCK DIAGRAM



PIN CONNECTIONS



PIN NAMES

A0-A9	Address Inputs	\overline{WE}	Write Enable
\overline{CE}	Chip Enable	\overline{OE}	Output Enable
V_{SS}	Ground	\overline{L}	Latch
V_{CC}	Power (+5V)	DQ0 - DQ7	Data In/ Data Out

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS}	-0.5V to +7.0V
Operating Temperature T_A (Ambient)	0°C to +70°C
Storage Temperature (Ambient) (Ceramic)	-65°C to +150°C
Storage Temperature (Ambient) (Plastic)	-55°C to +125°C
Power Dissipation	1 Watt
Short Circuit Output Current	20mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS³

(0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2		7.0	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3		0.8	V	1

DC ELECTRICAL CHARACTERISTICS^{1,3}

(0°C ≤ T_A ≤ +70°C) (V_{CC} = 5.0 volts ± 5%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current (Active)		80	mA	7
I_{CC2}	Average V_{CC} Power Supply Current (Standby)		60	mA	5
I_{IL}	Input Leakage Current (Any Input)	-10	10	μA	2
I_{OL}	Output Leakage Current	-10	10	μA	2
V_{OH}	Output Logic "1" Voltage $I_{OUT} = -1$ mA	2.4		V	
V_{OL}	Output Logic "0" Voltage $I_{OUT} = 4$ mA		0.4	V	

AC ELECTRICAL CHARACTERISTICS^{1,3}

(0°C ≤ T_A ≤ +70°C) (V_{CC} = +5.0 volts ± 5%)

SYM	PARAMETER	TYP	MAX	NOTES
C_I	Capacitance on all pins except I/O	4pF		4
$C_{I/O}$	Capacitance on I/O pins	10pF		4

NOTES:

1. All voltages reference to V_{SS} .
2. Measured with $0 \leq V_I \leq 5$ V and outputs deselected ($V_{CC} = 5$ V).
3. A minimum of 2msec time delay is required after application of V_{CC} (+5V) before proper device operation can be achieved.
4. Effective capacitance calculated from the equation $C = I \frac{\Delta t}{\Delta V}$ with $\Delta V = 3$ V and V_{CC} nominal.
5. Standby mode is defined as condition with addresses, latch and \overline{WE} remain unchanged.
6. AC timing measurements made with 2 TTL loads plus 100pF.
7. I_{CC} active measured with outputs open.

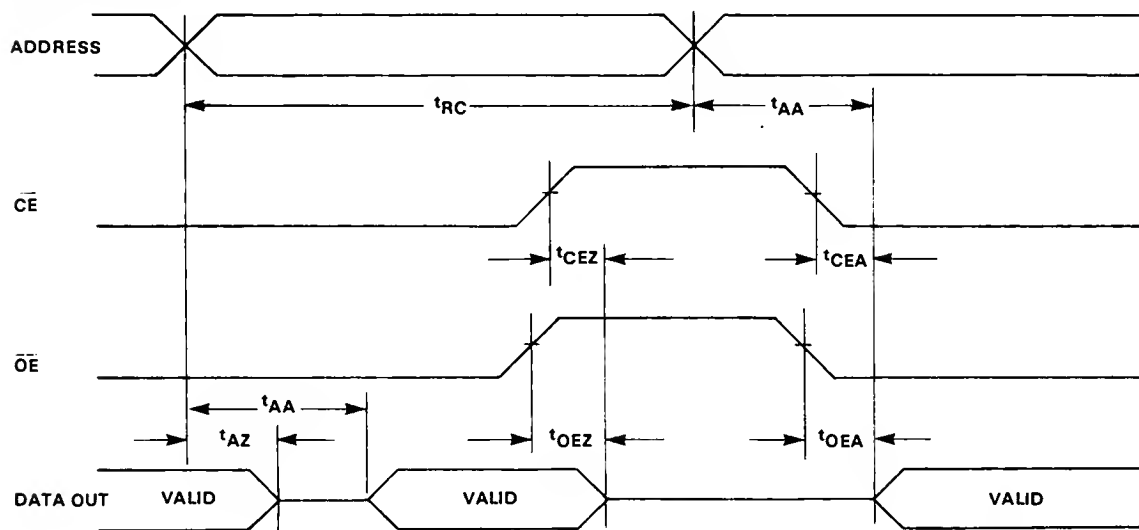
ELECTRICAL CHARACTERISTICS^a(0°C ≤ T_A ≤ 70°C and V_{CC} = 5.0 volts ± 5%)

SYM	PARAMETER	MK4118-1		MK4118-2		MK4118-3		MK4118-4		UNIT	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t _{RC}	Read Cycle Time	120		150		200		250		ns	
t _{AA}	Address Access Time		120		150		200		250	ns	
t _{CEA}	Chip Enable Access Time		60		75		100		125	ns	
t _{CEZ}	Chip Enable Data Off Time	0	60	0	75	0	100	0	125	ns	
t _{OEa}	Output Enable Access Time		60		75		100		125	ns	
t _{OEZ}	Output Enable Data Off Time	0	60	0	75	0	100	0	125	ns	
t _{AZ}	Address Data Off Time	10		10		10		10		ns	
t _{ASL}	Address to Latch Setup Time	10		10		10		20		ns	
t _{AHL}	Address From Latch Hold Time	40		50		65		80		ns	
t _{CEL}	\overline{CE} to Latch Setup Time	0		0		0		0		ns	
t _{CHL}	\overline{CE} From Latch Hold Time	40		50		65		80		ns	
t _{LA}	Latch Off Access Time		155		200		260		320	ns	
t _{WC}	Write Cycle Time	120		150		200		250		ns	
t _{ASW}	Address To Write Setup Time	0		0		0		0		ns	
t _{AHW}	Address From Write Hold Time	40		50		65		80		ns	
t _{CEW}	\overline{CE} To Write Setup Time	0		0		0		0		ns	
t _{CHW}	\overline{CE} From Write Hold Time	40		50		65		80		ns	
t _{DSW}	Data To Write Setup Time	20		30		40		50		ns	
t _{DHW}	Data From Write Hold Time	20		30		40		50		ns	
t _{WD}	Write Pulse Duration	35		50		60		70		ns	
t _{LDH}	Latch Duration, High	35	DC	50	DC	60	DC	70	DC	ns	
t _{LDL}	Latch Duration, Low		DC		DC		DC		DC	ns	
t _{WEZ}	Write Enable Data Off Time	0	60	0	75	0	100	0	125	ns	
t _{LZ}	Latch Data Off Time	10		10		10		10		ns	
t _{WPL}	Write Pulse Lead Time	75		90		130		170		ns	

STATIC
RAMS

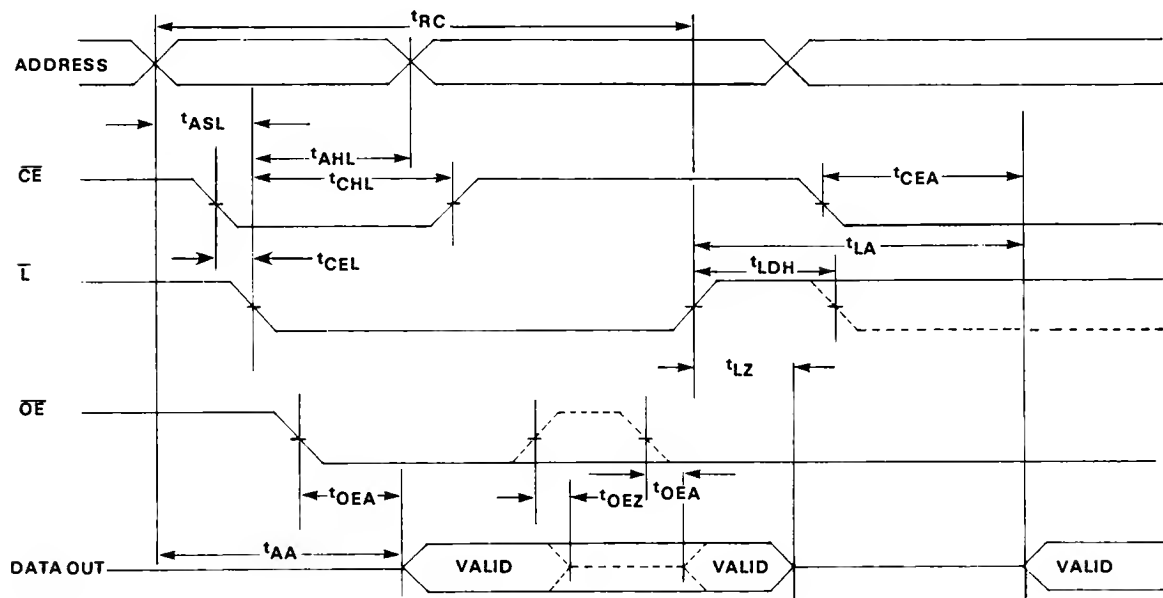
STATIC READ CYCLE

$\overline{WE} = \overline{L} = \text{HIGH}$



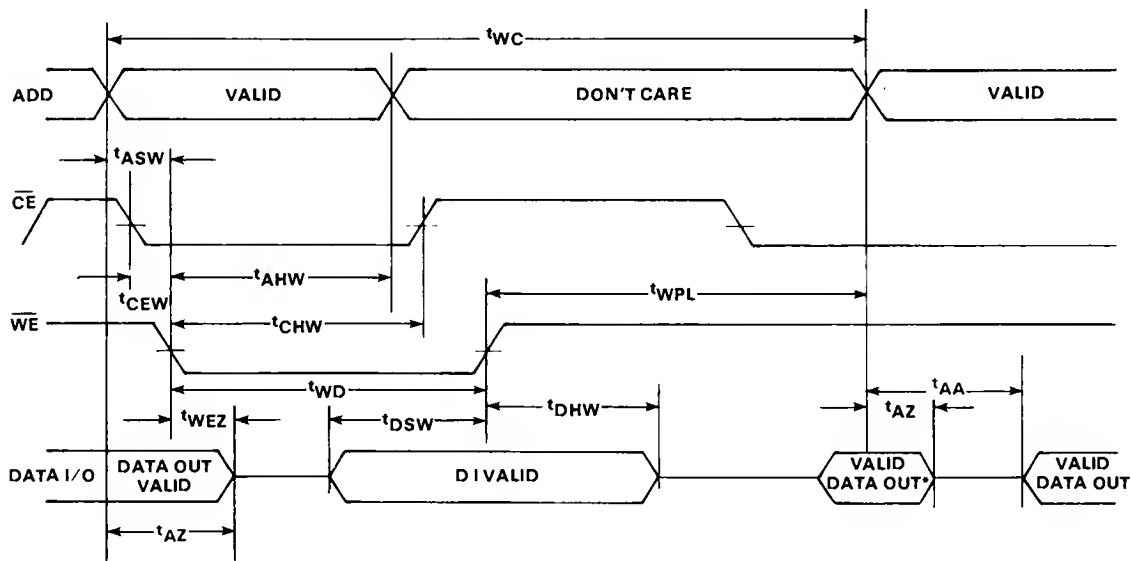
LATCHED READ CYCLE

$\overline{WE} = \text{HIGH}$



WRITE CYCLE

OE = LOW, \overline{L} = HIGH



OPERATION

READ MODE

The MK4118 is in the READ MODE whenever the Write Enable control input (\overline{WE}) is in the high state. The state of the 8 data I/O signals is controlled by the Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) control signals. The READ MODE memory cycle may be either STATIC (ripple-through) or LATCHED, depending on user control of the Latch Input Signal (\overline{L}).

STATIC READ CYCLE

In the STATIC READ CYCLE mode of operation, the MK4118 provides a fast address ripple-through access of data from 8 of 8192 locations in the static storage array. Thus, the unique address specified by the 10 Address Inputs (A_n) define which 1 of 1024 bytes of data is to be accessed. The STATIC READ CYCLE is defined by $\overline{WE} = \overline{L} = \text{High}$.

A transition on any of the 10 address inputs will disable the 8 Data Output Drivers after t_{AZ} . Valid Data will be available to the 8 Data Output Drivers with t_{AA} after all address input signals are stable, and the data will be output under control of the Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) signals.

LATCHED READ CYCLE

The LATCHED READ CYCLE is also defined by the Write

Enable control input (\overline{WE}) being in the high state, and it is synchronized by proper control of the Latch (\overline{L}) input.

As the Latch control input (\overline{L}) is taken low, Address (A_n) and Chip Enable (\overline{CE}) inputs that are stable for the specified set-up and hold times are latched internally. Data out corresponding to the latched address will be supplied to the Data Output drivers. The output drivers will be enabled to drive the Output Data Bus under control of the Output Enable (\overline{OE}) and latched Chip Enable (\overline{CE}) inputs.

Taking the latch input high begins another read cycle for the memory locations specified by the address then appearing on the Address Input (A_n). Returned the latch control to the low state latches the new Address and Chip Enable inputs internally for the remainder of the LATCHED READ CYCLE.

NOTE: If the 'LATCH' function is not used pin 19 (\overline{L}) must be tied high (V_{IH} min).

WRITE MODE

The MK4118 is in the WRITE MODE whenever the Write Enable (\overline{WE}) and Chip Enable (\overline{CE}) control inputs are in the low state. The status of the 8 output buffers during a write cycle is explained below.

WRITE MODE (Cont'd)

The WRITE cycle is initiated by the \overline{WE} pulse going low provided that \overline{CE} is also low. The leading edge of the \overline{WE} pulse is used to latch the status of the address bus. \overline{CE} if active (Low) will also be latched. NOTE: \overline{WE} is gated by \overline{CE} . If \overline{CE} goes low after \overline{WE} , the Write Cycle will be initiated by \overline{CE} , and all timing will be referenced to that edge. \overline{CE} and the Addresses will then be latched, and the cycle must be terminated by \overline{WE} going high. The output bus if not already disabled will go to the high Z state t_{WEZ} after \overline{WE} . The latch signal, if at a logic high, will have no impact on the WRITE cycle. If latch is brought from a logic high to low prior to \overline{WE} going active then the address inputs and \overline{CE} will be latched. NOTE: The Latch control (\overline{L}) will latch \overline{CE} independent

of the state, whereas \overline{WE} will latch \overline{CE} only when in the low state. Once latched, \overline{CE} and the address inputs may be removed after the required hold times have been met.

Data in must be valid t_{DSW} prior to the low-to-high transition of \overline{WE} . The Data in lines must remain stable for t_{DHW} after \overline{WE} goes inactive. The write control of the MK4118 disables the data out buffers during the write cycle; however, output enable (\overline{OE}) should be used to disable the data out buffers to prevent bus contention between the input data and data that would be output upon completion of the write cycle.

MK4801A(P/J/N) Series

FEATURES

- Static operation
- Organization: 1K x 8 bit RAM JEDEC pinout
- Pin compatible with Mostek's BYTEWYDE™ memory family
- 24/28 pin ROM/PROM compatible pin configuration
- \overline{CE} and \overline{OE} functions facilitate bus control

- High performance

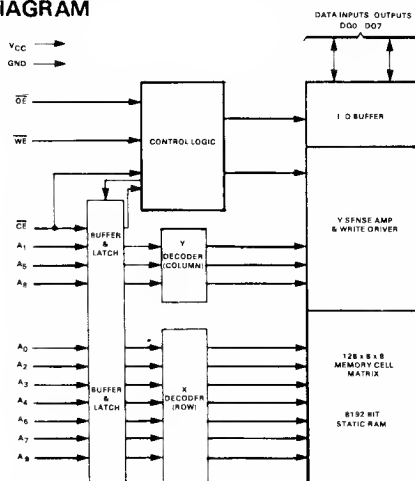
Part No.	Access Time	R/W Cycle Time
MK4801A-55	55 nsec	55/65 nsec
MK4801A-70	70 nsec	70/80 nsec
MK4801A-90	90 nsec	90/100 nsec

DESCRIPTION

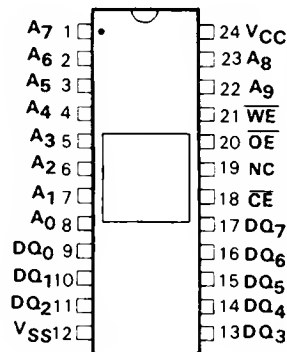
The MK4801A uses Mostek's Scaled POLY 5™ process and advanced circuit design techniques to package 8,192 bits of static RAM on a single chip. Static operation is achieved with high performance and low power dissipation by utilizing Address Activated™ circuit design techniques.

The MK4801A excels in high speed memory applications where the organization requires relatively shallow depth with a wide word format. The MK4801A presents the user a high density cost effective alternative to bipolar and previous generation N-MOS fast memory.

BLOCK DIAGRAM



PIN CONNECTIONS



TRUTH TABLE

\overline{CE}	\overline{OE}	\overline{WE}	Mode	DQ
V_{IH}	X	X	Deselect	High Z
V_{IL}	X	V_{IL}	Write	D_{IN}
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
V_{IL}	V_{IH}	V_{IH}	Read	High Z

X = Don't Care

PIN NAMES

A_0-A_9	Address Inputs	\overline{WE}	Write Enable
\overline{CE}	Chip Enable	\overline{OE}	Output Enable
V_{SS}	Ground	NC	No Connection
V_{CC}	Power (+5V)	DQ_0-DQ_7	Data In/ Data Out

STATIC
RAMS

MK4802(P/J/N) Series

FEATURES

- Static operation
- Organization: 2K x 8 bit RAM JEDEC pinout
- Pin compatible with Mostek's BYTEWYDE™ memory family
- Double density version of the MK4118 1K x 8 static RAM
- 24/28 pin ROM/PROM compatible pin configuration
- \overline{CE} and \overline{OE} functions facilitate bus control

- High performance

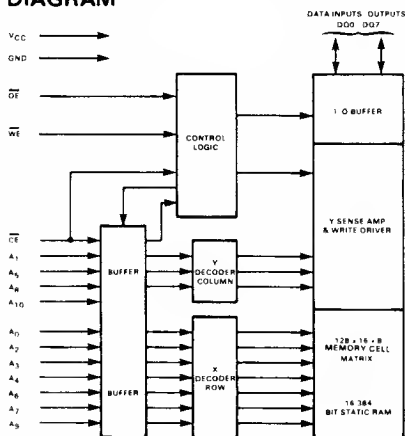
Part No.	Access Time	R/W Cycle Time
MK4802-70	70 nsec	70/80 nsec
MK4802-90	90 nsec	90/100 nsec

DESCRIPTION

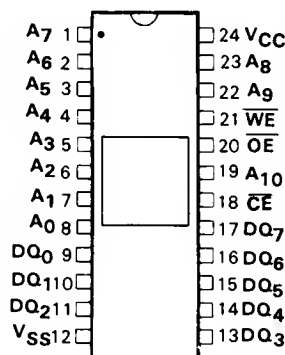
The MK4802 uses Mostek's Scaled POLY 5™ process and advanced circuit design techniques to package 16,384 bits of static RAM on a single chip. Static operation is achieved with high performance and low power dissipation by utilizing Address Activated™ circuit design techniques.

The MK4802 excels in high speed memory applications where the organization requires relatively shallow depth with a wide word format. The MK4802 presents the user a high density cost effective alternative to bipolar and previous generation N-MOS fast memory. The slower MK4802-3* provides even greater economies with performance suitable for microprocessor memory requirements.

BLOCK DIAGRAM



PIN CONNECTIONS



STATIC
RAMS

TRUTH TABLE

\overline{CE}	\overline{OE}	\overline{WE}	Mode	DQ
V_{IH}	X	X	Deselect	High Z
V_{IL}	X	V_{IL}	Write	D_{IN}
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
V_{IL}	V_{IH}	V_{IH}	Read	High Z

X - Don't Care

*See MK4802-3 Supplement Data Sheet

PIN NAMES

A_0 - A_{10}	Address Inputs	V_{CC}	Power (+5V)
\overline{CE}	Chip Enable	\overline{WE}	Write Enable
V_{SS}	Ground	\overline{OE}	Output Enable
DQ_0 - DQ_7	Data In/Data Out		

1980 MEMORY DATA BOOK

I	Table of Contents	TABLE OF CONTENTS
II	Order Information Packaging	ORDER PKG INFORM
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VII	Pseudostatic Random Access Memory	PSEUDO RAMS
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IX	Military/Hi-Rel Products	MILITARY HI REL PRODUCTS

PRELIMINARY

MOSTEK®

2K x 8-BIT PSEUDOSTATIC™ RAM

MK4816(N/J)-3/4/5

FEATURES

- Organized as 2048 x 8 bits

Part Number	Access Time	Cycle Time
MK4816-3	200nsec	430nsec
MK4816-4	250nsec	550nsec
MK4816-5	300nsec	675nsec

- Single +5V \pm 10% power supply

- On-chip substrate bias generator
- Low power - 150mW active
25mW standby
- 128 refresh cycles/2msec
- All pins TTL compatible
- 28 pin ROM/PROM compatible package
- Built in refresh multiplexer and refresh address counter
- Power down (standby) refresh mode
- Automatic precharge
- Latched address and CS and independent \overline{OE} for easy interface in any microprocessor system

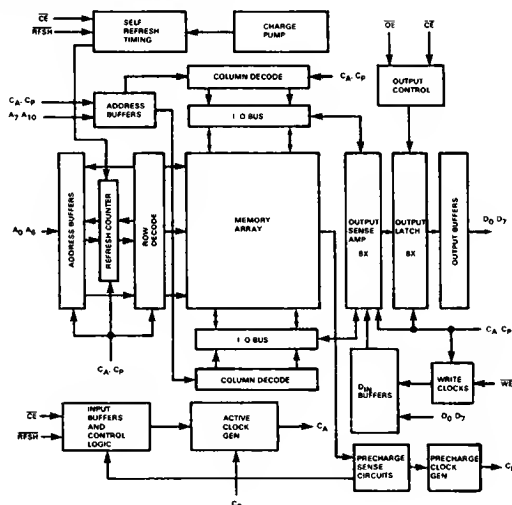
DESCRIPTION

The MK4816 uses Mostek's N Channel silicon gate process and advanced circuit design techniques to package 16,384 bits of Dynamic RAM on a single chip. The MK4816 is the first available 5V only Dynamic MOS RAM and the first wide-word Dynamic RAM designed specifically for use in present and future generation microprocessor systems. Organized as 2048 words x 8 bits, the MK4816 utilizes Mostek's Edge Activated™ design techniques to provide a low-power, high-performance, cost-effective RAM that includes many

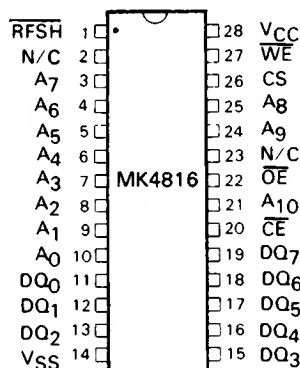
features designed to minimize external interface circuitry while maintaining the internal efficiency of a Dynamic RAM.

The MK4816 requires only a single +5 volt (\pm 10%) power supply and is fully TTL compatible on all inputs and outputs. A single Refresh pin allows flexible control of single cycle refresh, burst mode refresh, or automatic refresh in battery back-up mode. Common data I/O with independent chip select and Output Enable controls permit easy interface to either separate or multiplexed address and data bus systems.

BLOCK DIAGRAM



PIN OUT



PIN NAMES

DQ0-DQ7	Data	\overline{OE}	Output Enable
A0-A10	Address Inputs	WE	Write Enable
CE	Chip Enable	RFSH	Internal Refresh
CS	Chip Select		

PSEUDO
RAMS

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS}	-1.0V to +7.0V
Operating Temperature T_A (Ambient).....	0°C to +70°C
Storage Temperature (Ambient)(CERDIP).....	-65°C to +150°C
Power Dissipation	1 Watt
Short Circuit Output Current	20mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2		7.0	V	1
V_{IL}	Logic "0" Voltage All Inputs	-1.0		0.8	V	1

DC ELECTRICAL CHARACTERISTICS¹

(0°C ≤ T_A ≤ +70°C) (V_{CC} = 5.0 volts ± 10%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current ($T_C = t_C$ min)		30	mA	
I_{CC2}	Average V_{CC} Power Supply Current (Standby)		5	mA	3
I_{IL}	Input Leakage Current (Any Input)	-10	10	μA	2
I_{OL}	Output Leakage Current	-10	10	μA	2,3
V_{OH}	Output Logic "1" Voltage $I_{OUT} = -220\mu A$	2.4		V	
V_{OL}	Output Logic "0" Voltage $I_{OUT} = 4mA$		0.4	V	

AC ELECTRICAL CHARACTERISTICS¹

(0°C ≤ T_A ≤ +70°C) (V_{CC} = +5.0 volts ± 10%)

SYM	PARAMETER	TYP	MAX	NOTES
C_I	Input Capacitance	7pF	10pF	9
C_O	Output Capacitance	10pF	15pF	9,10

NOTES:

1. All voltages referenced to V_{SS}
2. Measured with $0V \leq V_{IN} \leq 5V$, $V_{CC} = 5V$, all other pins not under test = 0V
3. Output open circuit (\overline{CE} high)
4. An initial pause of 2ms is required after power-up followed by any 8 \overline{CE} cycles before proper device operation is achieved. If refresh counter is to be effective a minimum of 64 active \overline{RFSH} initialization cycles after one \overline{CE} cycle is required. The internal refresh counter must be accessed a minimum of every 2ms if auto mode refresh function is used.
5. AC measurements assume $t_T = 5ns$
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
7. Internal refresh counter initialization is required. 64 \overline{RFSH} stimulated cycles are sufficient for this purpose. \overline{RFSH} reinitialization is required when intervals greater than 2ms have occurred between refresh cycles controlled by \overline{RFSH} .
8. Measured with a load equivalent to 2 TTL loads and 50 pF. (Scope and Jig)
9. Effective capacitance calculated from the equation $C = \frac{\Delta I}{\Delta V}$ with $\Delta V = 3$ volts and power supplies at nominal levels.
10. D_{OUT} in high impedance state, by doing a read cycle with \overline{OE} held at V_{IH}
11. The specifications for t_C (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS^(4,5,6)
 $(0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}) (V_{CC} = 5.0\text{V} \pm 10\%)$

SYM	PARAMETER	MK4816-3		MK4816-4		MK4816-5		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_C	Read, Write, or Refresh Cycle Time	430		550		675		ns	11
t_{CEA}	Chip Enable Access Time		200		250		300	ns	8
t_{CEZ}	Chip Enable Data Off Time		45		55		65	ns	
t_{OEA}	Output Enable Access Time		70		90		110	ns	
t_{OEZ}	Output Enable Data Off Time		45		55		65	ns	
t_{ASC}	Address to \overline{CE} Set Up Time	0		0		0		ns	
t_{AHC}	Address from \overline{CE} Hold Time	55		70		85		ns	
t_{CSC}	Chip Select to \overline{CE} Set Up Time	0		0		0		ns	
t_{CHC}	Chip Select from \overline{CE} Hold Time	55		70		85		ns	
t_{RCS}	\overline{WE} to \overline{CE} Set Up Time for Read Cycle	0		0		0		ns	
t_{RCH}	\overline{WE} from \overline{CE} Hold Time for Read Cycle	0		0		0		ns	
t_{CE}	Chip Enable Duration	200	10,000	250	10,000	300	10,000	ns	
t_p	Chip Enable Precharge Time	65		80		95		ns	
t_{WSC}	Write Enable to \overline{CE} Set Up Time - Early Write	-35		-40		-45		ns	
t_{WHC}	Write Enable from \overline{CE} Hold Time - Early Write	125		160		195		ns	
t_{CSW}	Write Enable Delay from \overline{CE} - late write	35	5000	40	5000	45	5000	ns	
t_{CHW}	\overline{CE} Hold Time After \overline{WE} - Late Write	235		290		345		ns	
t_{DSC}	Data to \overline{CE} Set Up Time - Early Write	-10		-10		-10		ns	
t_{DHC}	Data from \overline{CE} Hold Time - Early Write	110		140		175		ns	
t_{DSW}	Data to \overline{WE} Setup Time - Late Write	0		0		0		ns	
t_{DHW}	Data from \overline{WE} Hold Time - Late Write	75		100		125		ns	
t_{WD}	Write Pulse Duration	90		120		150		ns	
t_{RD1}	Refresh Pulse Duration - Single Cycle	135	10000	145	10000	155	10000	ns	7
t_{CSR}	\overline{CE} to \overline{RFSH} Set Up Time	65		80		95		ns	
t_{ARA}	Auto Refresh Mode Delay Time	20		20		20		μs	7
t_{ARH}	Auto Refresh Mode Hold Time	430		550		675		ns	
t_{RDA}	Refresh Pulse Duration - Auto Refresh	20	∞	20	∞	20	∞	μs	7
t_T	Transition Time (rise and fall)	3	80	3	100	3	120	ns	6
t_{REF}	Refresh Period		2		2		2	ms	7
t_{CER}	\overline{CE} to \overline{RFSH} Hold Time	35		45		55		ns	
t_{FR}	\overline{RFSH} Recovery Time - Single Cycle	65		80		95		ns	

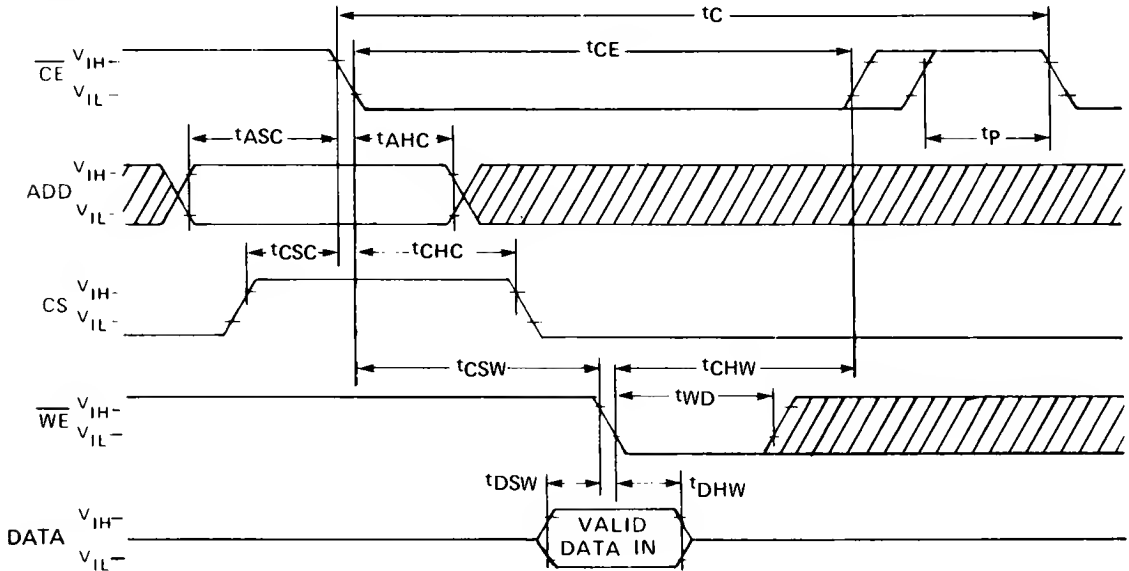
READ CYCLE



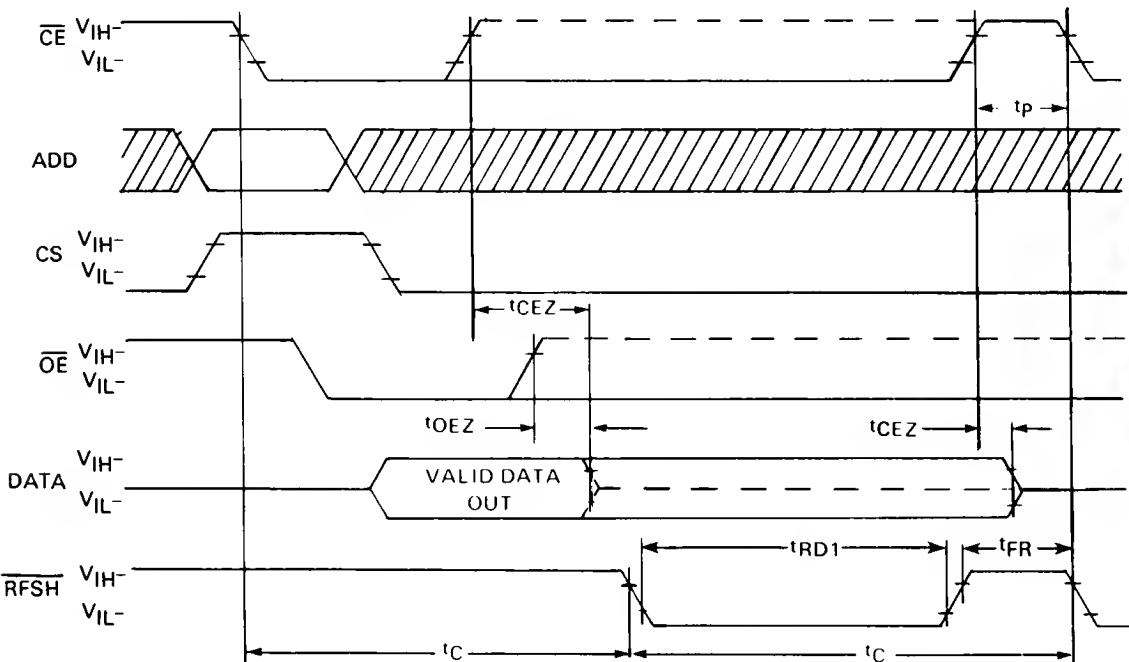
WRITE CYCLE — EARLY WRITE
($OE \geq V_{IH}$)



WRITE CYCLE - LATE WRITE
($\overline{OE} \geq V_{IH}$)



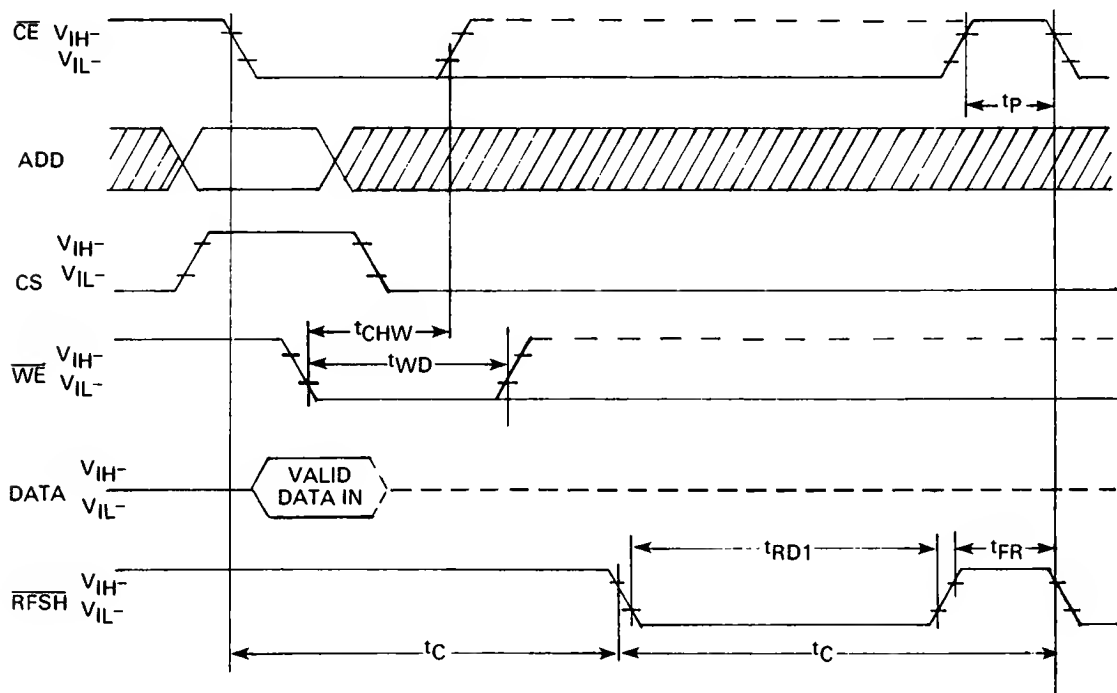
SINGLE REFRESH CYCLE AFTER READ CYCLE COMPLETE
($\overline{WE} \geq V_{IH}$)



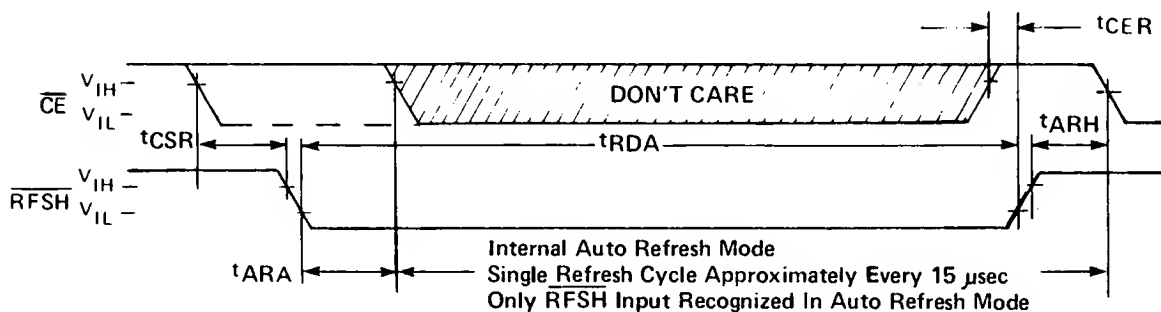
PSEUDO
RAMS

SINGLE REFRESH CYCLE AFTER WRITE CYCLE COMPLETE

($\overline{OE} \geq V_{IH}$)



AUTO REFRESH MODE



OPERATION

ADDRESSING

The 11 address bits required to decode 8 of the 16,384 memory cell locations within the MK4816 are latched into the on-chip address latches by the high-to-low transition of Chip Enable (\overline{CE}). Thus, the unique address specified by the 11 Address Inputs (A_n) define which 1 of 2048 bytes of data is to be accessed. Chip Enable also latches internally the state of Chip Select (CS). For a device to be selected, CS must be high during the high-to-low transition of \overline{CE} . After the specified hold time, the Addresses and CS may be changed in anticipation of the next cycle.

ACTIVE CYCLES

The MK4816 can perform three types of active cycles, determined by user control of \overline{CE} , \overline{OE} , CS , \overline{WE} , and $RFSH$. The cycles are READ, WRITE, and REFRESH. The MK4816 executes an automatic precharge at the end of any active cycle in preparation for the next active cycle. After the automatic precharge cycle is complete, the device will be in the standby mode until another active cycle is initiated.

READ CYCLE

A READ CYCLE is initiated by Chip Enable (\overline{CE}) going low with Chip Select (CS) High and Write Enable (\overline{WE}) high. The cycle is complete when data is output ($\overline{OE} = \text{LOW}$) or by \overline{CE} going high. Completion of the cycle initiates the automatic precharge cycle.

Data Out will become valid at access time provided that Output Enable (\overline{OE}) is low. If \overline{OE} is high at access time valid data will not appear at the output terminals although the data will be available to the output data buffers. Access time from \overline{OE} is approximately 36% of \overline{CE} access time, allowing adequate time for system decode of \overline{OE} .

At the end of the READ CYCLE, \overline{CE} going high unlatches the output. The trailing edge of \overline{CE} is non-critical in that it can be taken high any time after meeting the minimum \overline{CE} pulse width (t_{CE}).

After valid data is output ($\overline{CE} = \overline{OE} = \text{LOW}$ $t \geq t_{\text{ACCESS}}$), the MK4816 will initiate an automatic precharge cycle in preparation for the next active cycle. If \overline{OE} does not go low to permit valid data out, precharge will be initiated by \overline{CE} going high. The next active cycle may be initiated after the minimum cycle time (T_C) and the minimum precharge time (T_P) have been satisfied.

WRITE CYCLE

A WRITE CYCLE is initiated by Chip Enable (\overline{CE}) going low with Chip Select (CS) High and Output Enable (\overline{OE}) high. The cycle is complete when data is written into the memory array ($\overline{WE} = \text{LOW}$) or by \overline{CE} going high. Completion of the cycle initiates the automatic precharge cycle.

Data may be written into the memory locations specified by the address by either an EARLY WRITE CYCLE or a LATE WRITE CYCLE. The type of WRITE CYCLE is determined by the relative timing of the high-to-low transitions of \overline{CE} and \overline{WE} .

In an EARLY WRITE CYCLE, \overline{WE} and Valid Data In must be true with the specified setup and hold times relative to the high-to-low transitions of \overline{CE} . Upon completion of the WRITE operation, the MK4816 will initiate an automatic precharge cycle in preparation for the next active cycle. The next active cycle may be initiated after the minimum cycle time (T_C) and the minimum precharge time (T_P) have been satisfied.

In a LATE WRITE CYCLE, the high-to-low transition of \overline{CE} will latch the Addresses and CS internally; however, \overline{WE} may be delayed as much as 5 μ s to allow for more flexible system timing requirements. Valid Data In must be true with the specified setup and hold times relative to the high-to-low transition of \overline{WE} . In this case, the LATE WRITE CYCLE is initiated by the high-to-low transition of \overline{WE} . Upon completion of the WRITE Operation (or upon \overline{CE} going high, should \overline{WE} not make a transition) precharge will be initiated. The next active cycle may be initiated after the minimum cycle time (T_C) and the minimum precharge time (T_P) have been satisfied.

REFRESH CYCLE

The MK4816 can perform several types of REFRESH cycles, depending upon system requirements and/or user preference. As in other dynamic RAMs any active cycle performs refresh. Independent of the type of REFRESH cycle selected, 128 refresh cycles must be executed during each 2msec refresh interval. The user may specify the Refresh Address, or the Refresh Address generated by the internal Refresh Counter may be used.

EXTERNAL REFRESH ADDRESS ($\overline{RFSH} \geq V_{IH}$)

This refresh mode is identical to the refresh mode of the MK4116. The Row address specified by A_0 - A_6 defines the memory locations to be refreshed. A READ CYCLE or WRITE CYCLE at each of the 128 unique ROW addresses specified by A_0 - A_6 must be executed during each 2msec refresh interval. These REFRESH CYCLES may be either distributed or burst mode.

INTERNAL REFRESH ADDRESS ($\overline{\text{RFSH}}$ = PULSED LOW)

System refresh logic may be simplified or eliminated by utilizing the internal refresh control logic of the MK4816. This REFRESH CYCLE is initiated by an active low pulse applied to the Refresh pin ($\overline{\text{RFSH}}$). The $\overline{\text{RFSH}}$ pulse may occur one cycle time (t_C min) after $\overline{\text{CE}}$ initiates the cycle, or during Standby. In most microprocessor systems, it may be conveniently generated with each Instruction Fetch Cycle. (The MK3880 provides a $\overline{\text{RFSH}}$ output signal that connects directly to the $\overline{\text{RFSH}}$ input of the MK4816. Thus, the RAM appears totally static to the system.)

If the $\overline{\text{RFSH}}$ pulse occurs during standby, the $\overline{\text{RFSH}}$ CYCLE will be initiated immediately.

During the internally controlled REFRESH cycle, the Refresh Address specified by the internal Refresh Counter will be multiplexed onto the ROW address, the

REFRESH CYCLE will be executed, and the internal Refresh Counter will be incremented. Upon completion of the REFRESH CYCLE, the MK4816 will initiate an automatic precharge cycle in preparation for the next active cycle. Another active cycle may begin after the minimum cycle time (t_C) if $\overline{\text{RFSH}}$ is generated during standby. These REFRESH cycles may be either distributed or burst mode.

POWER DOWN AUTO REFRESH ($\overline{\text{RFSH}} \leq V_{IL}$)

For either power down (battery back-up) operation or microprocessor single-step operation, it is convenient to utilize the AUTO REFRESH mode of the MK4816. The AUTO REFRESH mode is initiated by maintaining $\overline{\text{RFSH}}$ in the low state. If $\overline{\text{RFSH}}$ remains low longer than $20\mu\text{s}$, the MK4816 will automatically initiate a single Internal Refresh Address REFRESH CYCLE approximately every $15\mu\text{s}$ until the AUTO REFRESH mode is terminated by $\overline{\text{RFSH}}$ going high. During the AUTO REFRESH mode, all inputs except $\overline{\text{RFSH}}$ are inhibited.

1980 MEMORY DATA BOOK

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MILITARY/HI-RELIABILITY PRODUCTS**

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MKB4027(J)-83/84	4096 x 1-Bit	IX-9
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MKB4116(E/F)-83/84	16,384 x 1-Bit	IX-13
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MKB4118(P/J)-82/83	1024 x 8-Bit	IX-21

Military and High Reliability Products

INTRODUCTION

Mostek's Military/Hi-Rel Products Department serves the special needs of the Defense, Aerospace and Commercial Hi-Rel markets. The organization's principal objective is to provide Mostek's state-of-the-art products screened to MIL-STD 883, Methods 5004 and 5005.

Traditional Military IC manufacturers have met stringent Military reliability requirements at a cost of being several years behind the state-of-the-art in commercial products. Mostek Military brings the leading edge in high reliability RAM, ROM, and EPROM devices to the Military systems designer today. As MIL-M-38510 slash sheets are announced, the Military Products Department will qualify Mostek's products in the JAN 38510 program. Mostek has already received QPL listing of its 4116 dynamic RAM. Designated JM-38510/240, this device is one of the most advanced MOS circuits to receive QPL listing to date.

The Military Products Department is also heavily engaged in the development of high density leadless chip carrier packaging technology. Several circuits are currently offered in carriers with more planned for the near future.

Product offerings are broken into two categories. Devices prefixed "MKB" are screened to the full requirements of MIL-STD-883 Class B. "MKM" prefixed devices are screened to a subset of 883B requirements and offer high reliability at significantly reduced cost (see the following sections for more detail concerning MKM products).

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MILITARY /
HI-REL

MOSTEK®

MILITARY/HI-REL PRODUCTS

Applications Guide

Customer's Product	Type of System	Mostek Type	Screening/Lot Conformance
Military	Ground Airbourne } Missile } —	MKM — { MKB — { JAN/JM-38510	883 Class B (Low Cost) 883 Class B 883 Class B (Domestic Assy)
Medical	Instrumentation	MKM	883 Class B (Low Cost)
Commercial	Large Boards Airbourne Other Hi-Rel	MKM MKB MKM	883 Class B (Low Cost) 883 Class B 883 Class B (Low Cost)

MILITARY/
HI-REL

Screening and Lot Conformance Comparison

Activity/Screen	MKM	MKB (883B)	JAN
Wafer Fabrication Assembly Test/Screening	Dallas Malaysia Mal. & Dal.	Dallas Malaysia Mal. & Dal.	Dallas Dallas Dallas
Die Inspect	Mostek Spec. 0066-01 (75X)	2010 Cond. B	2010 Cond. B
Pre-Seal Inspect	Mostek Spec. 0069-01(30-60X)	2010 Cond. B	2010 Cond. B
Stabilization Bake	1008 Cond. C	1008 Cond. C	1008 Cond. C
Temp. Cycle	1010 Cond. C	1010 Cond. C	1010 Cond. C
Centrifuge	QA Sample	2001 Cond. E	2001 Cond. E
Fine Leak	QA Sample	1014 Cond. B	1014 Cond. B
Gross Leak	QA Sample	1014 Cond. C2	1014 Cond. C2
Elect. Test 1	Max Rated Temp	Max Rated Temp	Per Slash Sheet
Voltage Stress (DRAMs only)	1015 Cond. D	1015 Cond. D	Per Slash Sheet
Elect. Test 2 (DRAMs only)	12 hrs. min Max Rated Temp	12 hrs. min Max Rated Temp	Max Rated Temp
Burn-in	1015 Cond. D	1015 Cond. D	1015 Cond. D
	48 hrs. min	160 hrs. min	160 hrs. min
Elect. Test 3	Max Rated Temp	Max Rated Temp	Per Slash Sheet
Elect. Test 4	—	Min Rated Temp	Per Slash Sheet
External Visual	Mostek Spec. 0088-00	2009	2009
QA Lot Acceptance	5005 Group A 25°C	5005 Group A/C of C	5005 Group A/C of C
Quality Conformance	—	5005 Groups B, C, D**	5005 Groups B, C, D**

**Upon Request

Military (MKB) Products Guide

Below is a listing of products Mostek currently offers screened to MIL-STD-883, Method 5004, Class B. They

are prefixed "MK8" rather than "MK" to designate Class B screening.

PART	PACKAGE TYPE	PART IDENTIFIER	ORGANIZATION	TEMPERATURE RANGE	ACCESS TIME
DYNAMIC RAMs					
MK84027	J	83	4K x 1	-55°C to 85°C	200ns
MK84027	J	84	4K x 1	-55°C to 85°C	250ns
JM-38510/ 24001BEC	JAN 4116	—	16K x 1	-55°C to 110°C*	200ns
JM-38510/ 240028EC					
	P	—	16K x 1	-55°C to 110°C*	250ns
MKB4116	E,F,J	82	16K x 1	-55°C to 85°C	150ns
MKB4116	E,F,J	83	16K x 1	-55°C to 85°C	200ns
MKB4116	E,F,J	84	16K x 1	-55°C to 85°C	250ns
MK84116	E,F,J	93	16K x 1	-55°C to 110°C*	200ns
MK84116	E,F,J	94	16K x 1	-55°C to 110°C*	250ns
STATIC RAMs					
MKB4104	E,J	84	4K x 1	-55°C to 125°C	250ns
MK84104	E,J	85	4K x 1	-55°C to 125°C	300ns
MKB4118	P,J	82	1K x 8	-55°C to 125°C*	150ns
MK84118	P,J	83	1K x 8	-55°C to 125°C*	200ns
READ ONLY MEMORIES					
MKB36000	P,J	83	8K x 8	-55°C to 125°C	250ns
MK836000	P,J	84	8K x 8	-55°C to 125°C	300ns
MK836000	P,J	80	8K x 8	-40°C to 85°C	250ns
ERASABLE PROGRAMMABLE READ-ONLY MEMORIES					
MKB2716	T,J	87	2K x 8	-55°C to 100°C	390ns
MKB2716	T,J	88	2K x 8	-55°C to 100°C	450ns

Package Type

*Case operating temperature

- F Ceramic Flat Package
- J Cerdip Hermetic
- E Leadless Hermetic Chip Carrier
- D Dual-in-Line Double Density Ceramic Package
- P Ceramic Dual-in-Line Hermetic Package
- T EPROM Hermetic Package

MOSTEK'S FUTURE MILITARY PRODUCTS

PART	ORGANIZATION	TEMPERATURE RANGE	ACCESS TIME	AVAILABILITY
DYNAMIC RAMs				
MKB4516	16K x 1	-55°C to 85°C	100ns	4Q80
MKB4164	64K x 1	-55°C to 85°C	120ns	1981
STATIC RAMs				
MKB2147	4K x 1	-55°C to 125°C	100ns	4Q80
MKB4802	2K x 8	-55°C to 125°C	100ns	1981
MKB4167	16K x 1	-55°C to 125°C	100ns	1981
READ ONLY MEMORY				
MKB37000	8K x 8	-55°C to 125°C	300ns	1981
ERASABLE PROGRAMMABLE READ ONLY MEMORY				
MKB2764	8K x 8	-55°C to 100°C	450ns	1981

Commercial Hi-Reliability (MKM) Products Guide

The military services normally procure systems whose component parts require special screening. Mostek addresses this market segment by screening parts to MIL-STD-883, Method 5004, Class B. This screening ensures that these parts will meet the high reliability military requirements. However, Mostek has determined that there is another market segment which requires the use of high reliability parts, but does not

have to adhere to all of the strict requirements of MIL-STD-883. Mostek has devised a flow which will provide a high reliability part but will offer significant cost savings.

The table below describes each of the high reliability products Mostek currently offers. They are prefixed "MKM" rather than "MK".

PART	PACKAGE	PART IDENTIFIER	ORGANIZATION	TEMPERATURE RANGE	ACCESS TIMES
DYNAMIC RAMs					
MKM4027	J	2	4K x 1	0°C to 70°C	150ns
MKM4027	J	3	4K x 1	0°C to 70°C	200ns
MKM4027	J	4	4K x 1	0°C to 70°C	250ns
MKM4116	J	2	16K x 1	0°C to 70°C	150ns
MKM4116	J	3	16K x 1	0°C to 70°C	200ns
MKM4116	J	4	16K x 1	0°C to 70°C	250ns
STATIC RAMs					
MKM4104	J	4	4K x 1	0°C to 70°C	250ns
MKM4104	J	5	4K x 1	0°C to 70°C	300ns
MKM4118	J	2	1K x 8	0°C to 70°C	150ns
MKM4118	J	3	1K x 8	0°C to 70°C	200ns
READ ONLY MEMORIES					
MKM36000	J	0	8K x 8	0°C to 70°C	250ns
ERASABLE PROGRAMMABLE READ ONLY MEMORIES					
MKM2716	J	6	2K x 8	0°C to 70°C	350ns
MKM2716	J	7	2K x 8	0°C to 70°C	390ns
MKM2716	J	8	2K x 8	0°C to 70°C	450ns
MKM2716	J	78	2K x 8	-40°C to 85°C	450ns
MICROCOMPUTERS					
MKM3880	P	4	CPU	0°C to 70°C	4MHz
MKM3881	P	4	PIO	0°C to 70°C	4MHz
MKM3882	P	4	CTC	0°C to 70°C	4MHz

MKM Screening Chart

Mostek's high reliability test flow is illustrated below.
Parts screened to this flow will carry the designation
"MKM".

PROCESS	MIL-STD-883 METHOD
Scribe/Break/SORT	Mostek Spec.
Die Inspect	2010 Cond. B
Die Mount	Mostek Spec.
Wire Bond	Mostek Spec.
Pre-Seal Inspect	2010 Cond. B
Lid Seal	Mostek Spec.
Stabilization Bake	1008 Cond C
Temp Cycle	1010 Cond C
Centrifuge	2001 Cond E
Fine Leak	1014 Cond B
Gross Leak	1014 Cond (C2)
Electrical Test 1	Max Rated Temp
Voltage Stress (DRAMs Only)	1015 Cond D, 12 hrs. min
Electrical Test 2 (DRAMs Only)	Max Rated Temp
Burn-in (LIFE)	1015 Cond D, 160 hrs. min
Final Test	Max Rated Temp
Symbolize	Per 38510
QA Lot Acceptance	Method 5005 Group A 2,5,8 max 10
External Visual	2009

Chip Carrier Packaging

The Military Products Department is committed to supporting the Military's need for high-density system

design with a full range of advanced memory components packaged in leadless chip carriers.

CURRENT PRODUCTS					
DEVICE	ORGANIZATION	ACCESS TIME	TEMPERATURE RANGE	ACTIVE POWER	STANDBY POWER
DRAMs					
MKB4116E-83	16K x 1	200ns	-55°C to 85°C	462mW	30mW
MKB4116E-84	16K x 1	250ns	-55°C to 85°C	462mW	30mW
MKB4116E-93	16K x 1	200ns	-55°C to 110°C**	462mW	30mW
MKB4116E-94	16K x 1	250ns	-55°C to 110°C**	462mW	30mW
SRAMs					
MKB4104E-84	4K x 1	250ns	-55°C to 125°C	150mW	53mW
MKB4104E-85	4K x 1	300ns	-55°C to 125°C	150mW	53mW

FUTURE OFFERINGS

New products released to the Military line will be offered in chip carrier packaging. This includes current and next generation dense RAM, ROM and EPROM.

CARRIER DESCRIPTIONS*

	Current Products (16/18 Pin)	Future Products (24/28 Pin) Preliminary Dimensions
# Pins	18	32 (per JEDEC algorithm)
Pin Spacing	50 mil	50 mil
Width	285 mil	450 mil
Length	350 mil	550 mil
	(425 mil, MKB4164)	
Height	75 mil	75 mil

*See Databook packaging section for additional dimensional details and pinout.

**Case Temperature

MKB Quality Specification

1.0 PURPOSE

This specification establishes the lot screening and quality conformance requirements used to achieve a level of quality and reliability commensurate with Class B of MIL-STD-883.

2.0 SCOPE

MKB prefixed MOS/LSI microcircuits

3.0 GENERAL

3.1 APPLICABLE DOCUMENTS

The following documents of issue in effect on the date of release of the Mostek sales order form a part of this specification except where amended herein.

- 3.1.1 MIL-M-38510 Microcircuits, General Spec for
- 3.1.2 MIL-STD-883 Test Methods and Procedures for Microcircuits
- 3.1.3 MIL-STD-1313 Microelectronics, Terms and Definitions
- 3.1.4 MIL-C-45662 Calibration Systems Requirements
- 3.1.5 MIL-STD-105 Sampling Tables
- 3.1.6 Applicable Device Data Sheet
- 3.1.7 Mostek Sales Order
- 3.1.8 Customer Purchase Order

3.2 DOCUMENT HIERARCHY

In the event of any conflict between this document and the referenced documents, the following order of precedence applies:

- 3.2.1 This document
- 3.2.2 Customer Purchase Order
- 3.2.3 Customer Device Specification
- 3.2.4 Mostek Device Data Sheet
- 3.2.5 Other Military Standards and Specification

3.3 DEFINITIONS

Terms, definitions and symbols are not defined herein shall have the same meaning as is commonly associated with the term, definition, or symbol used.

3.3.1 INSPECTION LOT

A group of microcircuits of the same device type, package type, and lead finish manufactured on the same production line using like production techniques which are sealed within seven calendar days beginning on Monday.

3.3.2 PERCENT DEFECTIVE ALLOWABLE (PDA)

The maximum percent defectives allowed which will allow a lot to continue normal processing. PDA shall be imposed across burn-in and measured by D.C. parametric failures only. PDA for MKB type devices shall not exceed 10%.

3.4 ITEM REQUIREMENTS

3.4.1 PACKAGE CONFIGURATION

The package lead configuration and physical dimensions shall be as specified in the detail device specification.

3.4.2 CASE MATERIAL

All devices manufactured under this document shall be hermetically sealed in a ceramic package. No organic materials shall be used inside the device package and the use of desiccant material shall not be permitted.

3.4.3 LEAD MATERIAL

All leads shall be plated in such a manner as to resist corrosion blistering, cracking and or peeling. Lead material may be either Type A (KOVAR) or Type B (ALLOY 42).

3.4.3.1 LEAD FINISH

Lead finish shall consist of one of the following:

PACKAGE TYPE LEAD FINISH

P,F,E	Gold (99.7% pure, 50 μ in min) over Ni underplate (50 μ in - 200 μ in)
J	Tin Plate (100 μ in min to 500 μ in max)

NOTE: "P" Type packages with hot solder dip lead finish may be supplied as an alternate to the "J" Type package but not without prior notification to the customer.

3.4.4 ELECTRICAL REQUIREMENTS

All devices manufactured under this document shall be guaranteed to meet the electrical characteristics specified in the customer device specifications as mutually agreed upon or the Mostek device data sheet.

3.4.5 ENVIRONMENTAL REQUIREMENTS

All end items manufactured under this document shall be capable of meeting the requirements of this specification after exposure to any or all of the environmental tests and conditions specified herein.

3.4.6 DEVICE MARKING REQUIREMENTS

Each end item manufactured under this specification shall be legibly and permanently (to the extent of MIL-STD-883 Method 2015) marked with the following information:

3.4.6.1 Manufacturers identification

3.4.6.2 Assembly location

3.4.6.3 Inspection lot date code

3.4.6.4 Manufacturers part type

3.4.6.5 Customer part no. (when applicable)

3.4.7 INDEX POINT

Each microcircuit package shall contain an index notch, tab or mark to denote pin one of the device.

3.4.8 WORKMANSHIP

All microcircuits supplied under this specification shall be manufactured using good engineering, production, and inspection practices as established by industry standards and inhouse controlled processing specifications.

3.4.9 LOT TRACEABILITY

Each inspection lot shall have traceability sufficient to detail all processing data related to the manufacture of that lot from wafer scribe through product shipment. All inspection lots shall be relatable to any or all production lots combined to form the inspection lot.

3.4.10 COUNTRY OF ORIGIN

Unless domestic manufacture is specifically required by the customer purchase order, MKB devices may be either of domestic or foreign origin.

Manufacture of MKB type devices at facilities not solely owned and operated by Mostek shall not be permitted.

4.0 PRODUCT ASSURANCE PROVISIONS

4.1 SAMPLING AND INSPECTION

Mostek shall be responsible for the performance of all inspections, as judged necessary by Mostek, required to produce product in compliance with this specification.

4.1.1 Inspections shall, as a minimum, be in accordance with MIL-STD-883 Method 5004 and Table 1 herein.

4.1.2 Quality conformance testing shall be in accordance with MIL-STD-883 Method 5005 and Table 2 herein.

4.1.3 Sampling plans shall be per MIL-STD-105 and MIL-M-38510 Appendix B.

4.2 TEST EQUIPMENT AND CALIBRATION

Mostek shall maintain test equipment sufficient to measure all electrical parameters and mechanical limits specified herein. Environmental tests subcontracted by Mostek shall be performed by subcontractors having active letters of laboratory suitability issued by D.E.S.C.

4.2.1 Calibration shall be per MIL-C-45662 on all inhouse equipment used to measure electrical parameters and/or mechanical dimensions which affect the quality or reliability of finished product produced under this document.

4.2.2 EQUIPMENT ACCURACY

Environmental and testing equipment shall have accuracies which meet or exceed the accuracy requirements of MIL-STD-883.

4.3 LOT SCREENING

All products shall be screened on a 100% basis to the tests and conditions specified in Table 1 herein. Electrical test subgroups shall be in accordance with Table 2 herein.

4.3.1 BURN IN

Burn-in shall be performed per MIL-STD-883 Method 1015 Condition D.

- a) $T_a = 125^{\circ}\text{C}$
- b) $t = 160 \text{ hrs min}$
- c) Burn-in P.D.A. shall be 10% as measured by D.C. parametric failures occurring at the first electrical test after completion of burn-in. Rejects occurring at electrical test performed prior to burn-in shall not be included in the P.D.A. calculation. P.D.A. shall be calculated as follows: The total D.C. parametric failures divided by the total quantity submitted for burn-in.
- d) Cool down with Bias: Bias during cool-down shall not be removed from devices while oven temperature conditions are above 35°C .

4.3.2 DYNAMIC RAMS ONLY

Voltage cell stress shall be performed per MIL-STD-883 Method 1015 Condition D except as follows:

- a) $T_a = 125^{\circ}\text{C}$
- b) $t = 12 \text{ hrs min}$
- c) $V_{dd}, V_{bb} = \text{Accelerated}$ - Refer to detail burn-in specification
- d) Voltage stress shall be inserted in Table 1 after hermiticity and prior to burn-in.

- 4.4** Processes in addition to those specified in Table 1 may be performed by Mostek where deemed necessary to enhance the quality or reliability of products manufactured under this document.

5.0 QUALITY CONFORMANCE

- 5.1** Quality conformance tests consisting of Groups A and B shall be performed on each inspection lot as defined herein. Groups B, C, and D shall be generic unless otherwise specified on the customer purchase order.

5.1.1 GROUP A

Inspection shall be in accordance with Mostek Spec 651-00020-10 and Table 2 herein. Group A may be sampled using either of the following methods:

- a) A random sample taken from the entire inspection lot, or
- b) A random sample taken from each production lot combined to form an inspection lot.

5.1.2 GROUP B

Inspection shall be in accordance with Mostek Spec 651-00021-10 and Table 2 herein. Group B may be sampled using one of the following methods:

- a) Catalog product-generic random sample taken from the first production lot (representing an inspection lot seal week) received by Q.A. Each inspection lot seal week shall have a minimum of Group B performed, or
- b) Customer inspection lot specific-random sample taken from the entire inspection lot.

5.1.3 GROUP C

Inspection shall be in accordance with Mostek Spec 651-00022-10 and Table 2 herein. Group C may be sampled using one of the following methods:

- a) Catalog product-generic random sample taken from the production lot produced for quality conformance testing. Production lots will be periodically manufactured (each 13 weeks) for the performance of Group C. Each microcircuit group, by device type, shall be produced, on a rotating basis, to insure each device type conforms to the requirements set forth herein. Microcircuit grouping shall be per Table 4, or
- b) Customer inspection lot specific-random sample taken from the entire inspection lot.

5.1.4 GROUP D

Inspection shall be in accordance with Mostek Spec 651-00023-10 and Table 2 herein. Group D may be sampled using one of the following methods.:

- a) Catalog product-generic random sample taken from the production lot produced for quality conformance testing. Production lots will be periodically manufactured (each 26 weeks) for the performance of Group D. Each microcircuit group, by package type, shall be produced, on a rotating basis, to insure each package type conforms to the requirements set forth herein. Microcircuit grouping shall be per Table 4 herein.
- b) Customer lot specific-random sample taken from entire insp. lot.

5.2 NON-CONFORMANCE

5.2.1 P.D.A.

Any lot exhibiting a percent defective greater than 10% but less than 20% may be resubmitted to burn-in one time. The resubmission P.D.A. shall be 7%. Lots having percents defective greater than 20% (initial) or 7% (resubmission) shall be submitted to M.R.B. for disposition.

5.2.2 QUALITY CONFORMANCE

Any subgroup(s) failed by an inspection lot may be resubmitted one time using a tightened LTPD. A second resubmission using tightened LTPD's is permitted only if Failure Analysis indicates the failure mechanism can be removed by rescreening the entire lot and the failure mechanism is not the result of poor basic design or processing. The inspection lot need only be resubmitted to the failed subgroup.

5.2.3 QUALITY CONFORMANCE FAILURE

Quality Conformance Failure shall occur anytime an inspection lot is withdrawn from quality conformance during a non-compliance condition or if the inspection lot fails to meet the requirements of Paragraphs 5.1.1, 5.1.2, 5.1.3, or 5.1.4. Shipment of inspection lots which fail quality conformance testing is prohibited unless specifically requested by the customer.

5.3 DATA

Data to be supplied with MKB products at time of shipment shall include one copy of the following attributes data:

5.3.1 Group A

5.3.2 Group B (Generic or lot specific, if specified on P.O.)

5.3.3 Group C (Generic or lot specific, if specified on P.O.)

5.3.4 Group D (Generic or lot specific, if specified on P.O.)

5.3.5 Lot processing summary, including P.D.A. data.

5.3.6 Certificate of compliance

6.0 PROCESSING OPTIONS

6.1 The following list of options may be ordered in addition to the MKB process defined by this document. Each option process must be specifically ordered on the customer P.O. with additional cost adders determined by Mostek.

6.1.1 Customer pre-cap visual inspection

6.1.2 Customer source inspection-finished goods shipping

6.1.3 Government source inspection-finished goods shipping

6.1.4 Radiographic insp. per 883/2012

6.1.5 P.I.N.D. test per 883/2020 A or B

6.1.6 Destructive physical analysis

6.1.7 240-hour burn-in per 883/1015 D

6.1.8 Failure analysis of life test failures

6.1.9 Non-standard temperature electrical testing

6.1.10 Quality conformance Groups B, C, and/or D generic

6.1.11 Quality conformance Groups B, C, and/or D lot specific

7.0 PACKAGING FOR SHIPMENT

7.1 Each microcircuit shall be fully enclosed in an antistatic material with sufficient conductivity to permit bleed-off of static charges and to prevent the introduction of electronic charges from the external environment.

7.2 Each intermediate shipping container shall be clearly marked with an "electrostatic sensitive" warning label.

7.3 All products procured by this document shall be packaged for shipment using well established packaging techniques to insure delivery to the purchaser in good working order.

8.0 ORDERING INFORMATION

8.1 The customer purchase order shall specify the following:

8.1.1 Device type

8.1.2 Package type

8.1.3 Source inspection detail requirements

8.1.4 Quality conformance requirements

8.1.5 Processing options (Para. 6.0)

8.1.6 Test data requirements (Para. 5.3)

8.1.7 Quantity required

LOT SCREENING

Table 1

Process	MIL-STD-883 Method	Mostek Specification
Scribe		0063-Xx
Break		0064-00
Sort		0065-00
Die Inspect	2010 Cond. B	0066-01
Die Mount		0067-00
Wire Bond		0068-00
Pre-Seal Inspect	2010 Cond. B	0069-01
Lid Seal		0070-XX
Stabilization Bake	1008 Cond. C	0074-10
Temp Cycle	1010 Cond. C	1012-10
Centrifuge	2001 Cond. E	1010-10
Fine Leak	1014 Cond. B	0071-10
Gross Leak	1014 Cond. C	1016-10
Elect Test 1	Max Rated Temp	Data Sheet
Voltage Stress	1015 Cond. D, 12 hrs. min.	690-XXXXX-XX
Elect Test 2	Max Rated Temp	Data Sheet
Burn-In	1015 Cond. D, 160 hrs min	690-XXXXX-XX
Final Test 1	Max Rated Temp	Data Sheet
Final Test 2	Min Rated Temp	Data Sheet
Symbolize		0077-05
External Visual	2009	0088-00
Quality Conformance	5005	3028-10

QUALITY CONFORMANCE (MIL-STD-883 Method 5005)

Table 2

Group	Subgroup	LTPD	Mostek Specification
Group A			3020-10
	1,4,7,9	5	Data Sheet
	2,5,8max,10	7	Data Sheet
	3,6,8min,11	7	Data Sheet
Group B			3021-10
	1	2 Devices	1022-10
	2	3 Devices	21150-10
	3	15	1027-10
	4	1 Device	0081-10
	5	15	1074-10
	6	3 Devices	70584-10
Group C			3022-10
	1	5	690-XXXXX-XX
	2	15	3022-10
Group D			3023-10
	1a	15	1022-10
	1b	3 Devices	70584-10
	2	15	3023-10
	3	15	3023-10
	4	15	3023-10
	5	15	3023-10

ELECTRICAL TEST

Table 3

Electrical Test	Electrical Subgroups	Test Temp	Device Types
Elect. Test 1	2,5,8max,10	Max Rated**	All
Elect. Test 2	2,5,8max,10	Max Rated	Dynamic RAMs Only
Final Test 1	2*,5,8max,10	Max Rated**	All
Final Test 2	3,6,8min,11	Min Rated**	All
Final Test 3	1,4,7,9	25°C**	Microprocessors Only
Group A	1,2,3,4,5,6,7,8,9 10,11	All	All
Groups C&D	2,5,8max,10	Max Rated	All

0*P.D.A. applies to subgroup 2 only; for microprocessors only, PDA applies to subgroup 1

**Microprocessor Test Temperature:

Elect Test 1 - 25°C

Final Test 1 - 25°C

Final Test 2 - Min Rated

Final Test 3 - Max Rated

MICROCIRCUIT GROUPING

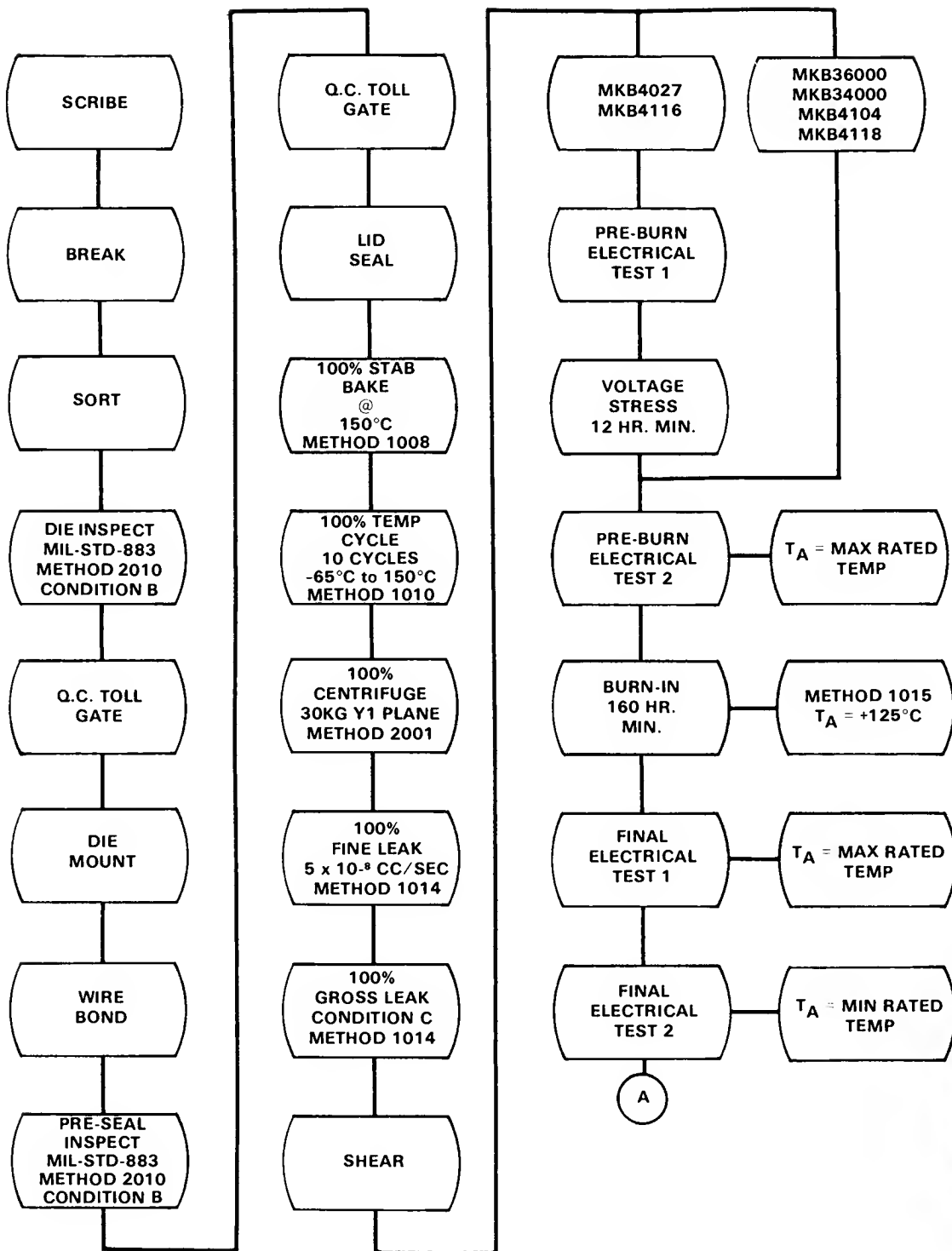
Figure 4

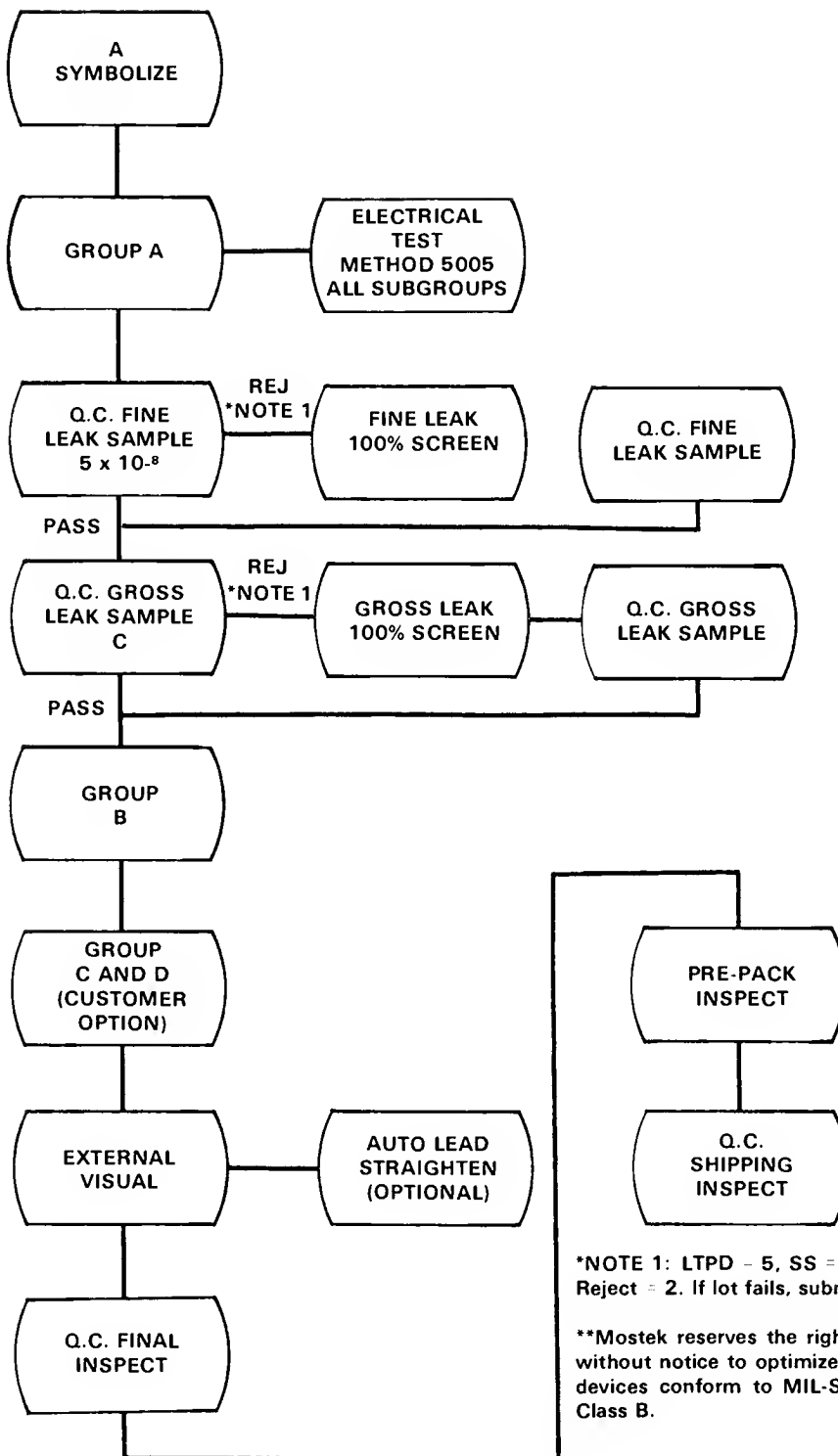
Package/Device Type	P	J	F	E	T
4116	2E	2A	2F	2Z	
4027		2A	2F	2Z	
4104	1V	1B	1G	1Z	
4118	1J	1C	1K		
2716					4Y
36000	3J	3C	3K		
34000	3J	3C			
3870	5Q				
3880	5Q				
3881	5Q				
3882	5X				
3883	5Q				
3884	5Q				
3885	5Q				
3886	5Q				
3887	5Q				

DEVICE CLASS

Package Designators

Static RAM—1	P(16)—E	J(16)—A	F(16)—F
Dynamic RAM—2	P(18)—V	J(18)—B	F(18)—G
ROM—3	P(24)—J	J(24)—C	F(24)—K
EPROM—4	P(28)—X	E(18)—Z	
Microprocessor—5	P(40)—Q	T(24)—Y	





*NOTE 1: LTPD = 5, SS = 77, Accept = 1.
Reject = 2. If lot fails, submit for 100% screen.

**Mostek reserves the right to implement changes without notice to optimize the MKB flow. All MKB devices conform to MIL-STD-883B, Method 5004, Class B.

MIL STD 105D

TABLE I
Sample size code letters

TABLE II-A
Single sampling plans for normal inspection (Master table)

Lot or batch size	General inspection levels			Sample size code letter	Sample size	Acceptable Quality Levels (normal inspection)																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																										
	I	NORMAL LEVEL II				III	.010	.015	.025	.040	.065	0.10	0.15	0.25	0.40	0.65	1.0	1.5	2.5	4.0	6.5	10	15	25																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																								
2 to 8	A	A	8	A	2	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	Ac	Re	

▼ = Use first sampling plan below arrow. If sample size equals, or exceeds, lot or batch size, do 100 percent inspection.
▲ = Use first sampling plan above arrow.

Re = Rejection number. Ac = Acceptance number.

MILITARY/
HI REL

TABLE C—1. LTPD sampling plans 1/2/
 Minimum size of sample to be tested to assure, with a 90 percent confidence, that a lot having percent-defective equal to the specified LTPD will not be accepted (single sample).

Max. Percent Defective (LTPD) or λ	20	15	10	7	5	3	2	1.5	1	0.7	0.5	0.3
Acceptance Number (C) ($r = c + 1$)	Minimum Sample Sizes (For device-hours required for life test, multiply by 1000)											
0	11 (0.46)	15 (0.34)	22 (0.23)	32 (0.16)	45 (0.11)	76 (0.07)	116 (0.04)	153 (0.03)	231 (0.02)	328 (0.02)	461 (0.01)	767 (0.007)
1	18 (2.0)	25 (1.4)	38 (0.94)	55 (0.65)	77 (0.46)	129 (0.28)	195 (0.18)	258 (0.14)	390 (0.09)	555 (0.06)	778 (0.045)	1296 (0.027)
2	25 (3.4)	34 (2.24)	52 (1.6)	75 (1.1)	105 (0.78)	176 (0.47)	266 (0.31)	354 (0.23)	533 (0.15)	759 (0.11)	1065 (0.080)	1773 (0.045)
3	32 (4.4)	43 (3.2)	65 (2.1)	94 (1.5)	132 (1.0)	221 (0.62)	333 (0.41)	444 (0.31)	668 (0.20)	953 (0.14)	1337 (0.10)	2226 (0.062)
4	38 (5.3)	52 (3.9)	78 (2.6)	113 (1.8)	158 (1.3)	265 (0.75)	398 (0.50)	531 (0.37)	798 (0.25)	1140 (0.17)	1599 (0.12)	2663 (0.074)
5	45 (6.0)	60 (4.4)	91 (2.9)	131 (2.0)	184 (1.4)	308 (0.85)	462 (0.57)	617 (0.42)	927 (0.28)	1323 (0.20)	1855 (0.14)	3090 (0.085)
6	51 (6.6)	68 (4.9)	104 (3.2)	149 (2.2)	209 (1.6)	349 (0.94)	528 (0.62)	700 (0.47)	1054 (0.31)	1503 (0.22)	2107 (0.155)	3509 (0.093)
7	57 (7.2)	77 (5.3)	116 (3.5)	166 (2.4)	234 (1.7)	390 (1.0)	589 (0.67)	783 (0.51)	1178 (0.34)	1680 (0.24)	2355 (0.17)	3922 (0.101)
8	63 (7.7)	85 (5.6)	128 (3.7)	184 (2.6)	258 (1.8)	431 (1.1)	648 (0.72)	864 (0.54)	1300 (0.36)	1854 (0.25)	2599 (0.18)	4329 (0.108)
9	69 (8.1)	93 (6.0)	140 (3.9)	201 (2.7)	282 (1.9)	471 (1.2)	709 (0.77)	945 (0.58)	1421 (0.38)	2027 (0.27)	2842 (0.19)	4733 (0.114)
10	75 (8.4)	100 (6.3)	152 (4.1)	218 (2.9)	306 (2.0)	511 (1.2)	770 (0.80)	1025 (0.60)	1541 (0.40)	2199 (0.28)	3082 (0.20)	5133 (0.120)

1/ Sample sizes are based upon the Poisson exponential binomial limit.

2/ The minimum quality (approximate AQL) required to accept (on the average) 19 of 20 lots is shown in parenthesis for information only.

1980 MEMORY DATA BOOK

I	Table of Contents	TABLE OF CONTENTS
II	Order Information Packaging	ORDER PKG INFORM
III	Sales Office Locations	SALES OFFICES
IV	Read Only Memory	ROMS
V	Dynamic Random Access Memory	DYNAMIC RAMS
VI	Static Random Access Memory	STATIC RAMS
VII	Pseudostatic Random Access Memory	PSEUDO RAMS
VIII	Military/Hi-Rel	MILITARY/ HI REL
IX	Military/Hi-Rel Products	MILITARY HI-REL PRODUCTS

FEATURES

- MKB36000 8K x 8 Organization - "Edge Activated" operation (CE)
- Maximum access time: 300ns (—84)
250ns (—83)
250ns (—80)
- Low Power Dissipation — 220mW max active
- Extended operating ambient temperature range
($-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$): —84
($-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$): —83
($-40^{\circ}\text{C} \leq T_A \leq +80^{\circ}\text{C}$): —80
- Standard 24 pin DIP (EPROM Pin Out Compatible)
- Low Standby Power Dissipation — 55mW typical (CE High)
- On chip latches for addresses
- Inputs and three-state outputs-TTL compatible
- Outputs drive 2 TTL loads and 100 pF
- Ruggedized for use in severe military environments
- Single +5V \pm 10% power supply

DESCRIPTION

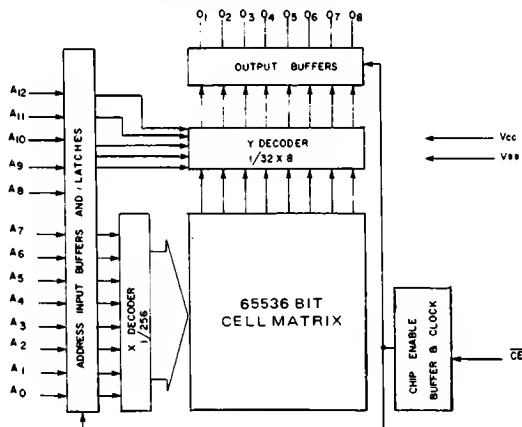
The MKB36000 is a new generation N-channel silicon gate MOS Read Only Memory, organized as 8192 words by 8 bits. As a state-of-the-art device, the MKB36000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining lower power dissipation and wide operating margins.

The MKB36000 utilizes what is fast becoming an industry standard method of device operation. Use of a static storage cell with clocked control periphery allows the circuit to be put into an automatic low power standby mode. This is accomplished by maintaining the

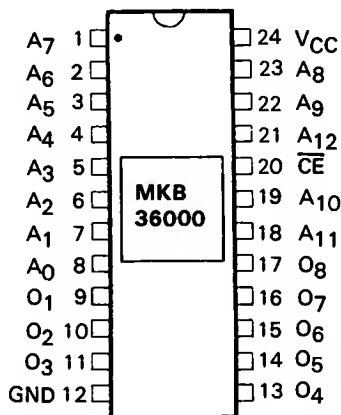
chip enable ($\overline{\text{CE}}$) input at a TTL high level. In this mode, power dissipation is reduced to typically 35mW, as compared to unlocked devices which draw full power continuously. In system operation, a device is selected by the $\overline{\text{CE}}$ input, while all other are in a low power mode, reducing the overall system power. Lower power means reduced power supply cost, less heat to dissipate and an increase in device and system reliability.

The edge activated chip enable also means greater system flexibility and an increase in system speed. The MKB36000 features onboard address latches controlled by the $\overline{\text{CE}}$ input. Once the address hold time specification has been met, new address data can be applied in anticipation of the next cycle. Outputs can be

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to V_{SS}	-0.5V to +7V
Operating Temperature T_A (Ambient) -83/84	-55°C to +125°C
Operating Temperature T_A (Ambient) -80	-40°C to +85°C
Storage Temperature — Ceramic (Ambient)	-65°C to +150°C
Power Dissipation	1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS⁶

(-55°C ≤ T_A ≤ +125°C) for -84; (-40°C ≤ T_A ≤ +85°C) for -80

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	Volts	6
V_{IL}	Input Logic 0 Voltage	-1.0		0.8	Volts	
V_{IH}	Input Logic 1 Voltage	2.4		V_{CC}	Volts	

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = 5V \pm 10\%$) (ELECTRICAL CHARACTERISTICS VALID OVER TEMPERATURE RANGE FOR EACH DEVICE)⁶

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{CC1}	V_{CC} Power Supply Current Active			40	mA	1
I_{CC2}	V_{CC} Power Supply Current Standby			10	mA	7
$I_{I(L)}$	Input Leakage Current	-10		10	μA	2
$I_{O(L)}$	Output Leakage Current	-10		10	μA	3
V_{OL}	Output Logic "0" Voltage @ $I_{OU1} = 3.3mA$			0.4	Volts	
V_{OH}	Output Logic "1" Voltage @ $I_{OU1} = 220 \mu A$	2.4			Volts	

AC ELECTRICAL CHARACTERISTICS

($V_{CC} = 5V \pm 10\%$)⁶ (ELECTRICAL CHARACTERISTICS VALID OVER TEMPERATURE RANGE FOR EACH DEVICE)⁶

SYM	PARAMETER	36000-80/83		36000-84		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_C	Cycle Time	375		450		ns	4
t_{CE}	CE Pulse Width	250	7500	300	7500	ns	4
t_{AC}	CE Access Time		250		300	ns	4
t_{OFF}	Output Turn Off Delay		60		75	ns	4
t_{AH}	Address Hold Time Referenced to CE	60		75		ns	4
t_{AS}	Address Setup Time Referenced to CE	0		0		ns	
t_p	CE Precharge Time	125		150		ns	

CAPACITANCE
($-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C ₁	Input Capacitance	5	8	pF	5
C ₀	Output Capacitance	7	15	pF	5

NOTES:

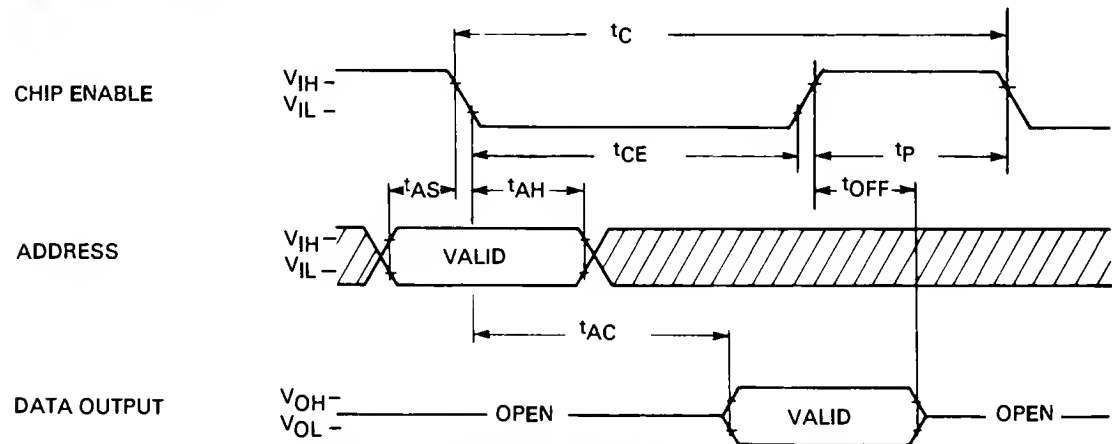
- Current is proportional to cycle rate. I_{CC1} is measured at the specified minimum cycle time.
- $V_{IN} = 0\text{V}$ to 5.5V
- Device unselected; $V_{OUT} = 0\text{V}$ to 5.5V
- Measured with 2 TTL loads and 100pF , transition times = 20ns .
- Capacitance measured with Boonton Meter or effective capacitance

calculated from the equation:

$$C = \frac{\Delta Q}{\Delta V} \text{ with } \Delta V = 3\text{volts}$$

- A minimum 2ms time delay is required after the application of $V_{CC} (+5)$ before proper device operation is achieved. \overline{CE} must be high during this period.
- \overline{CE} high.

TIMING DIAGRAM



MKB 36000 ROM PUNCHED CARD CODING FORMAT (1 & 6)

	COLS	INFORMATION FIELD	DATA FORMAT	
FIRST CARD	1-30 31-50 60-72	Customer Customer Part Number Mostek Part Number (2)	512 data cards (16 data words/card) with the following format:	
			COLS	INFORMATION FIELD
SECOND CARD	1-30 31-50	Engineer at Customer Site Direct Phone Number for Engineer	1-4	Four digit octal address of first output word on card
			5-7	Three digit octal output word specified by address in column 1-4
THIRD CARD	1-5	Mostek Part Number (2)		
FOURTH CARD	1-9 15-28 35-57	Data Format (3) Logic — ("Positive Logic" or "Negative Logic") Verification Code (4)	8-52	Next fifteen output words, each word consists of three octal digits.

NOTES:

- Positive or negative logic formats are accepted as noted in the fourth card.
- Assigned by Mostek; may be left blank.
- Mostek punched card coding format should be used Punch "Mostek" starting in column one.
- Punches as (a) VERIFICATION HOLD — i.e., customer verification of the data as reproduced by Mostek is required prior to production of the ROM. To accomplish this Mostek supplies a copy of its Customer Verification Data

Sheet (CVDS) to the customer.

- (b) VERIFICATION PROCESS — i.e., the customer will receive a CVDS but production will begin prior to receipt of customer verification; (c) VERIFICATION NOT NEEDED — i.e., the customer will not receive a CVDS and production will begin immediately.
- 512 cards for MKB36000.
- Please consult Mostek ROM Programming Guide for further details on other formats.

DESCRIPTION (Continued)

wire- 'OR'ed together, and a specific device can be selected by utilizing the \overline{CE} input with no bus conflict on the outputs. The \overline{CE} input allows the fastest access times yet available in 5 volt only ROM's and imposes no loss in system operating flexibility over an unlocked device.

Other system oriented features include fully TTL compatible inputs and outputs. The three state outputs, controlled by the \overline{CE} input, will drive a minimum of 2 standard TTL loads. The MKB36000 operates from a single +5 volt power supply with a wide $\pm 10\%$ tolerance, providing the widest operating margins available. The MKB36000 is packaged in the industry standard 24 pin DIP.

Any application requiring a high performance, high bit density ROM can be satisfied by the MKB36000 ROM. This device is ideally suited for 8 bit microprocessor systems such as those which utilize the Z80. It can offer significant cost advantages over PROM.

OPERATION

The MKB36000 is controlled by the chip enable (\overline{CE}) input. A negative going edge at the \overline{CE} input will activate the device as well as strobe and latch the inputs into the onchip address registers. At access time the outputs will become active and contain the data read from the selected location. The outputs will remain latched and active until \overline{CE} is returned to the inactive state.

PROGRAMMING DATA

Mostek is now able to utilize a wide spectrum of data input formats and media. Those presently available are listed in the following table:

Table 1

Acceptable Media	Acceptable Format
CARDS PAPER PROMS DATA LINK	MOSTEK INTEL CARD INTEL TAPE EA MOSTEK F-8 MOTOROLA 6800

**SUPPLEMENTAL DATA SHEET TO BE USED IN CONJUNCTION
WITH MK36000(P/N)-4/5 DATA SHEET**

MOSTEK®

2048 x 8-BIT UV ERASABLE PROM

Processed to MIL-STD-883, Method 5004, Class B

MKB2716(T/J)-87/88/90

FEATURES

- Extended operating temperature ($-55^{\circ}\text{C} \leq T_A \leq 100^{\circ}\text{C}$)
- Replacement for popular 1024 x 8 bit 2708 type EPROM
- Single +5 volt power supply during READ operation
- Fast Access Time in READ mode

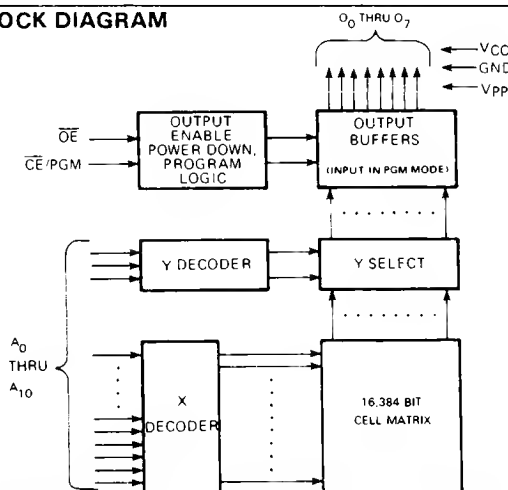
P/N	Access Time
MKB2716-87	390ns
MKB2716-88	450ns
MKB2716-90	550ns

DESCRIPTION

The MKB2716 is a 2048 x 8 bit electrically programmable/ultraviolet erasable Read Only Memory. The circuit is fabricated with Mostek's advanced N-channel silicon gate technology for the highest performance and reliability. The MKB2716 offers significant advances over hardwired logic cost, system flexibility, turnaround time and performance.

The MKB2716 has many useful system oriented features including a STANDBY mode of operation which lowers the device power from 633mW maximum active power to 165mW maximum for an overall savings of 75%.

BLOCK DIAGRAM



NOTE: Pin 18 and 20 have been renamed for compatibility with presently available 16K, 32K, and 64K ROMs and future generation 32K and 64K EPROMs. All other specifications for this device remain unaffected by this change.

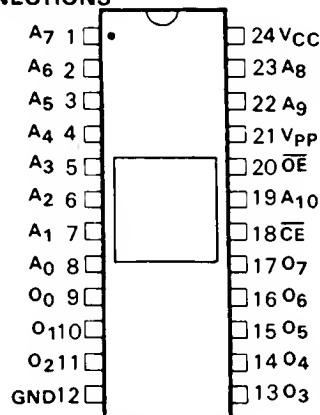
- Low Power Dissipation: 633 mW max active
- Power Down mode: 165 mW max standby
- Three State Output OR-tie capability
- Five modes of operation for greater system flexibility (see Table)
- Single programming requirement: single location programming with one 50 msec pulse
- TTL compatible in all operating modes
- Standard 24 pin DIP with transparent lid
- Ruggedized for use in severe military environments

MODE SELECTION

PIN MODE	$\overline{\text{CE}}/\text{PGM}$ (18)	$\overline{\text{OE}}$ (20)	VPP (21)	OUTPUT
READ	V_{IL}	V_{IL}	+5	Valid Out
STANDBY	V_{IH}	Don't Care	+5	Open
PROGRAM	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	Input
PROGRAM VERIFY	V_{IL}	V_{IL}	+25	Valid Out
PROGRAM INHIBIT	V_{IL}	V_{IH}	+25	Open

$V_{\text{CC}}(24) = 5\text{V}$ all modes

PIN CONNECTIONS



A0 - A10 Addresses
 $\overline{\text{CE}}/\text{PGM}$ Chip Enable/Program
 $\overline{\text{OE}}$ Output Enable
O0 - O7 Outputs

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS}	-0.3V to +6V (Except V_{PP})
Voltage on V_{PP} supply pin relative to V_{SS}	-0.3V to +28V
Operating Temperature T_A (Ambient)	$-55^{\circ}\text{C} \leq T_A \leq 100^{\circ}\text{C}$
Storage Temperature (Ambient)	$-65^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$
Power Dissipation	1 Watt
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

RECOMMENDED DC OPERATING CONDITIONS AND CHARACTERISTICS^{1,2,4,8}

($-55^{\circ}\text{C} \leq T_A \leq 100^{\circ}\text{C}$) ($V_{CC} = +5\text{V} \pm 10\%$, $V_{PP} = V_{CC}$)²

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	Volts	
V_{IL}	Input Low Voltage	-0.1		0.8	Volts	
I_{CC1}	V_{CC} Standby Power Supply Current ($\overline{OE} = \overline{V_{IL}}$; $CE = V_{IH}$)		10	30	mA	2
I_{CC2}	V_{CC} Active Power Supply Current ($\overline{OE} = CE = V_{IL}$)		57	115	mA	2
I_{PP1}	V_{PP} Current ($V_{PP} = 5.5\text{V}$)			10	mA	2
V_{OH}	Output High Voltage ($I_{OH} = -400 \mu\text{A}$)	2.4			Volts	
V_{OL}	Output Low Voltage ($I_{OL} = 2.1\text{mA}$)			.45	Volts	
I_{IL}	Input Leakage Current ($V_{IN} = 5.5\text{V}$)			10	μA	
I_{OL}	Output Leakage Current ($V_{OUT} = 5.5\text{V}$)			10	μA	

AC CHARACTERISTICS^{1,2,5}

($-55^{\circ}\text{C} \leq T_A \leq 100^{\circ}\text{C}$) ($V_{CC} = +5\text{V} \pm 10\%$, $V_{PP} = V_{CC}$)²

SYM	PARAMETER	-87		-88		-90		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{ACC}	Address to Output Delay ($CE = \overline{OE} = V_{IL}$)		390		450		550	ns	
t_{CE}	CE to Output Delay ($\overline{OE} = \overline{V_{IL}}$)		390		450		550	ns	5
t_{OE}	Output Enable to Output Delay ($\overline{CE} = V_{IL}$)		150		150		180	ns	9
t_{DF}	Chip Deselect to Output Float ($\overline{CE} = V_{IL}$)	0	130	0	130	0	130	ns	8
t_{OH}	Address to Output Hold ($\overline{CE} = \overline{OE} = V_{IL}$)	0		0		0		ns	

CAPACITANCE

(T_A = 25°C)⁸

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C _{IN}	Input Capacitance	4	6	pF	6
C _{OUT}	Output Capacitance	8	12	pF	6

READ OPERATION NOTES:

- 1 V_{CC} must be applied on or before V_{PP} and removed after or at the same time as V_{PP}.
- 2 V_{PP} and V_{CC} may be connected together except during programming, in which case the supply current is the sum of I_{CC} and I_{PP1}.
- 3 All voltages with respect to V_{SS}.
- 4 Load conditions: I_{TL} load and 100pF, t_{ri} = t_{rf} = 20ns, reference levels are 1V or 2V for inputs and 8V and 2V for outputs.
- 5 t_{OE} is referenced to \overline{CE} or the addresses, whichever occurs last.
- 6 Effective Capacitance calculated from the equation $C = \frac{Q}{V}$ where Q = 3V.
- 7 Typical numbers are for T_A = 25°C and V_{CC} = 5.0V.
- 8 t_{or} is applicable to both \overline{CE} and \overline{OE} , whichever occurs first.
- 9 OE may follow up to t_{ACC} + t_{OE} after the falling edge of \overline{CE} without effecting t_{ACC}.

PROGRAM OPERATION⁸

D.C. ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS⁸

(T_A = 25°C ± 5°C) (V_{CC} = 5V ± 10%, V_{PP} = 25V ± 1V)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I _{IL}	Input Leakage Current		10	μA	3
V _{IL}	Input Low Level	-0.1	0.8	Volts	
V _{IH}	Input High Level	2.0	V _{CC} + 1	Volts	
I _{CC}	V _{CC} Power Supply Current		100	mA	
I _{PP1}	V _{PP} Supply Current		5	mA	4
I _{PP2}	V _{PP} Supply Current during Programming Pulse		30	mA	5

A.C. CHARACTERISTICS AND OPERATING CONDITIONS^{1, 2, 6, 7}
(T_A = 25°C ± 5°C) (V_{CC} = 5V ± 10%, V_{PP} = 25V ± 1V)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t _{AS}	Address Setup Time	2			μs	
t _{OES}	$\overline{\text{OE}}$ Setup Time	2			μs	
t _{DS}	Data Setup Time	2			μs	
t _{AH}	Address Hold Time	2			μs	
t _{OE_H}	$\overline{\text{OE}}$ Hold Time	2			μs	
t _{DH}	Data Hold Time	2			μs	
t _{DF}	Output Enable to Output Float	0		130	ns	4
t _{OE}	Output Enable to Output Delay			120	ns	4
t _{PW}	Program Pulse Width	45	50	55	ms	
t _{PRT}	Program Pulse Rise Time	5			ns	
t _{PFT}	Program Pulse Fall Time	5			ns	

PROGRAM OPERATION NOTES:

1. V_{CC} must be applied at the same time or before V_{PP} and removed after or at the same time as V_{PP}. To prevent damage to the device it must not be inserted into a board with V_{PP} at 25V
2. Care must be taken to prevent overshoot of the V_{PP} supply when switching to -25V
3. 0.45V ≤ V_{IN} ≤ 5.25V
4. $\overline{\text{CE}}/\text{PGM}$ V_{IL}
5. $\overline{\text{CE}}/\text{PGM}$ V_{IH}
6. t_r = 20nsec
7. 1V or 2V for inputs and 8V or 2V for outputs are used as timing reference levels.
8. Although speed selections are made for READ operation all programming specifications are the same for all dash numbers

**SUPPLEMENTAL DATA SHEET TO BE USED IN CONJUNCTION
WITH MOSTEK MK2716(T)-6/7/8.**

FEATURES

- Extended operating temperature range ($-55^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$)
- Industry standard 16-pin DIP (MK4096) configuration
- 200ns access time, 375ns cycle (-83)
250ns access time, 375ns cycle (-84)
- $\pm 10\%$ tolerance on all supplies ($+12\text{V}$, $\pm 5\text{V}$)
- Low Power: 467mW active (max)
40mW standby (max)

DESCRIPTION

The MKB4027 is a 4096 word by 1 bit MOS random access memory circuit fabricated with Mostek's N-channel silicon gate process. This process allows the MKB4027 to be a high performance state-of-the-art memory circuit that is manufacturable in high volume. The MKB4027 employs a single transistor storage cell utilizing a dynamic storage technique and dynamic control circuitry to achieve optimum performance with low power dissipation.

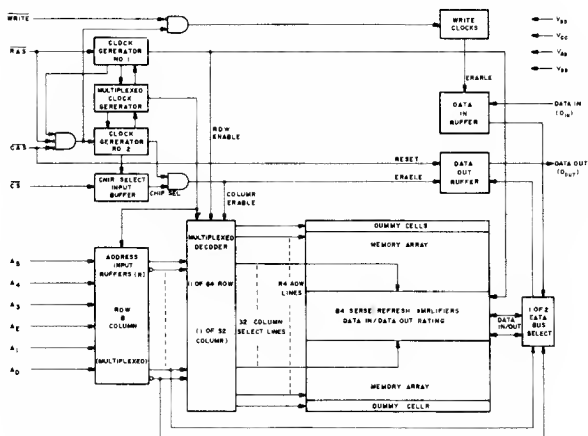
A unique multiplexing and latching technique for the address inputs permits the MKB4027 to be packaged in a standard 16-pin DIP on 0.3 in. centers. This package size provides high system-bit densities and is compatible

- Improved performance with "gated $\overline{\text{CAS}}$," " $\overline{\text{RAS}}$ only" refresh and page mode capability
- All inputs are low capacitance and TTL compatible
- Input latches for addresses, chip select and data in
- Three-state TTL compatible output
- Output data latched and valid into next cycle
- Ruggedized for use in severe military environments

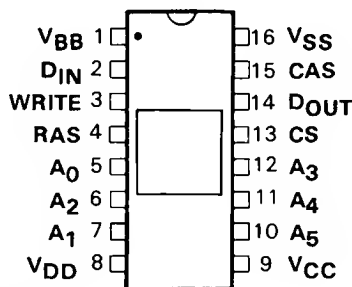
with widely available automated testing and insertion equipment.

System oriented features include direct interfacing capability with TTL, only 6 very low capacitance address lines to drive, on-chip address and data registers which eliminates the need for interface registers, input logic levels selected to optimize noise immunity, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MKB4027 also incorporates several flexible operating modes. In addition to the usual read and write cycles, read-modify write, page-mode, and $\overline{\text{RAS}}$ only refresh cycles are available with the MKB4027. Page-mode timing is very useful in systems requiring Direct Memory Access (DMA) operation.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A ₀ - A ₆	Address Inputs	WRITE	Read/Write Input
CS	Col Address Strobe	V _{BB}	Power (-5V)
D _{IN}	Data In	V _{CC}	Power (+5V)
D _{OUT}	Data Out	V _{DD}	Power (+12V)
RAS	Row Address Strobe	V _{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB}	-0.5V to +20V
Voltage on V_{DD} , V_{CC} relative to V_{SS}	-1.0V to +15V
$V_{BB} - V_{SS}$ ($V_{DD} - V_{SS} > 0$)	0V
Operating Temperature (Ambient)(Ceramic)	-55°C to +85°C
Storage Temperature (Ambient)(Ceramic)	-65°C to +150°C
Short Circuit Output Current	50mA
Power Dissipation	1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS⁴

(-55°C ≤ T_A ≤ 85°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	10.8	12.0	13.2	V	2
V_{CC}	Ground	4.5	5.0	5.5	V	2,3
V_{SS}	Supply Voltage	0	0	0	V	2
V_{BB}	Supply Voltage	-4.5	-5.0	-5.5	V	2
V_{IHC}	Logic 1 Voltage, \overline{RAS} , \overline{CAS} , \overline{WRITE}	2.7		7.0	V	2
V_{IH}	Logic 1 Voltage, all inputs except \overline{RAS} , \overline{CAS} , \overline{WRITE}	2.4		7.0	V	2
V_{IL}	Logic 0 Voltage, all inputs	-1.0		.8	V	2

DC ELECTRICAL CHARACTERISTICS⁴

(-55°C ≤ T_A ≤ 85°C) ($V_{DD} = 12.0V \pm 10\%$; $V_{CC} = 5.0V \pm 10\%$; $V_{SS} = 0V$; $V_{BB} = -5.0V \pm 10\%$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{DD1}	Avg. V_{DD} Power Supply Current			35	mA	5
I_{DD2}	Standby V_{DD} Power Supply Current			3.0	mA	8
I_{DD3}	Avg. V_{DD} Power Supply Current during " \overline{RAS} only" cycles			27	mA	
I_{CC}	V_{CC} Power Supply Current				mA	6
I_{BB}	Avg. V_{BB} Power Supply Current			200	μA	
$I_{(L)}$	Input Leakage Current (any input)			10	μA	7
$I_{O(L)}$	Output Leakage Current			10	μA	8,9
V_{OH}	Output Logic 1 Voltage @ $I_{OUT} = -5mA$	2.4			V	
V_{OL}	Output Logic 0 Voltage @ $I_{OUT} = 3.2mA$			0.4	V	

NOTES:

- T_A is specified for operation at frequencies to $t_{RC} \geq t_{RC}(\min)$. Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible provided that all AC parameters are met.
- All voltages referenced to V_{SS} .
- Output voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the $V_{OH}(\min)$ specification is not guaranteed in this mode.
- Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
- Current is proportional to cycle rate. $I_{DD1}(\max)$ is measured at the cycle rate specified by $t_{RC}(\min)$. See Figure 1 for I_{DD1} limits at other cycle rates.
- I_{CC} depends on output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to Data Out. At all other times I_{CC} consists of leakage currents only.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (4,11,7)
 $(-55^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C})^1$ ($V_{DD} = 12.0\text{V} \pm 10\%$, $V_{CC} = 0\text{V}$, $V_{BB} = -5.0\text{V} \pm 10\%$)

SYM	PARAMETER	MKB4027-83		MKB4027-84		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t _{RC}	Random read or write cycle time	375		380		ns	12
t _{RWC}	Read-write cycle time	375		395		ns	12
t _{RMW}	Read Modify Write Cycle	405		470		ns	12
t _{PC}	Page mode cycle time	225		285		ns	12
t _{RAC}	Access time from row address strobe		200		250	ns	13,15
t _{CAC}	Access time from column address strobe		135		165	ns	14,15
t _{OFF}	Output buffer turn-off delay		50		60	ns	
t _{RP}	Row address strobe precharge time	120		120		ns	
t _{RAS}	Row address and strobe pulse width	200	5000	250	5000	ns	
t _{RSH}	Row address strobe hold time	135		165		ns	
t _{CAS}	Column address strobe pulse width	135		165		ns	
t _{CSH}	$\overline{\text{CAS}}$ hold time	200		250		ns	
t _{RCD}	Row to column strobe delay	25	65	35	85	ns	16
t _{ASR}	Row address set-up time	0		0		ns	
t _{RAH}	Row address hold time	25		35		ns	
t _{ASC}	Column address set-up time	0		0		ns	
t _{CAH}	Column address hold-time	55		75		ns	
t _{AR}	Column address hold time referenced to $\overline{\text{RAS}}$	120		160		ns	
t _{CSC}	Chip select set-up time	0		0		ns	
t _{CH}	Chip select hold time	55		75		ns	
t _{CHR}	Chip select hold time referenced to $\overline{\text{RAS}}$	120		160		ns	
t _T	Transition time (rise and fall)	3	50	3	50	ns	17
t _{RCS}	Read command set-up time	0		0		ns	
t _{RCH}	Read command hold time	0		0		ns	
t _{WCH}	Write command hold time	55		75		ns	
t _{WCR}	Write command hold time referenced to $\overline{\text{RAS}}$	120		160		ns	
t _{WP}	Write command pulse width	55		75		ns	
t _{RWL}	Write command to row strobe lead time	70		85		ns	
t _{CWL}	Write command to column strobe lead time	70		85		ns	
t _{DS}	Data in set-up time	0		0		ns	18

ELECTRICAL CHARACTERISTICS (Continued)

SYM	PARAMETER	MKB4027-83		MKB4027-84		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t _{DH}	Data in hold time	55		75		ns	18
t _{DHR}	Data in hold time referenced to $\overline{\text{RAS}}$	120		160		ns	
t _{CRP}	Column to row strobe precharge time	0		0		ns	
t _{CP}	Column precharge time	80		110		ns	
t _{RFSH}	Refresh Period		2		2	ms	
t _{WCS}	Write command set-up time	0		0			19
t _{CWD}	$\overline{\text{CAS}}$ to WRITE delay	80		80		ns	19
t _{RWD}	$\overline{\text{RAS}}$ to WRITE delay	145		175		ns	19
t _{DOH}	Data out hold time	5		5		μs	

NOTES (Continued)

- 7 All device pins at 0 volts except V_{BB} which is at -5 volts and the pin under test which is at -10 volts
- 8 Output logic is disabled (high-impedance) and $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are both at a logic 1. Transient stabilization is required prior to measurement of this parameter
- 9 $0\text{V} \leq V_{\text{OUT}} \leq -10\text{V}$
- 10 Effective capacitance is calculated from the equation

$$C = \frac{\Delta Q}{\Delta V} \text{ with } \Delta V = 3 \text{ Volts}$$
- 11 AC measurements assume $t_1 = 5\text{ns}$
- 12 The specification for $t_{\text{RC}}(\text{min})$ and $t_{\text{RWC}}(\text{min})$ are used only to indicate cycle time at which proper operation over the full temperature range ($-55^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$) is assured. See Figure 2 for derating curve
- 13 Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$
- 14 Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$
- 15 Measured with a load circuit equivalent to 2 TTL loads and 100pF
- 16 Operation within the $t_{\text{RAC}}(\text{max})$ limit insures that $t_{\text{RCD}}(\text{max})$ is specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC}
- 17 $V_{\text{IH}}(\text{min})$ or $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{\text{IH}}(\text{C})$ or V_{IH} and V_{IL}
- 18 These parameters are referenced to CAS leading edge in random write cycles to WRITE leading edge in delayed write or read-modify-write cycles.
- 19 t_{WCS} , t_{CWD} , and t_{RWD} are restrictive operating parameters in a read/write or read/modify/write cycle only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the Data Out will contain the data written into the selected cell. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ and $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, the cycle is a read-write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indetermined.

AC ELECTRICAL CHARACTERISTICS

($-55^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$)¹ ($V_{\text{DD}} = 12.0\text{V} \pm 10\%$, $V_{\text{CC}} = 5\text{V} \pm 10\%$, $V_{\text{SS}} = 0\text{V}$, $V_{\text{BB}} = -5.0\text{V} \pm 10\%$)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C _{I1}	Input Capacitance ($A_0 - A_5$), D_{IN} , $\overline{\text{CS}}$	4	5	pF	10
C _{I2}	Input Capacitance $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, WRITE	8	10	pF	10
C _O	Output Capacitance (D_{OUT})	5	7	pF	8,10

**SUPPLEMENTAL DATA SHEET TO BE USED IN CONJUNCTION
WITH MOSTEK MK4027(J)-1/2/3 and MK4027(J)-4 DATA SHEETS**

16,384 x 1-BIT DYNAMIC RAM

Processed to MIL-STD-883, Method 5004, Class B

MKB4116(P/J)-82/83/84

MKB4116(E/F)-83/84

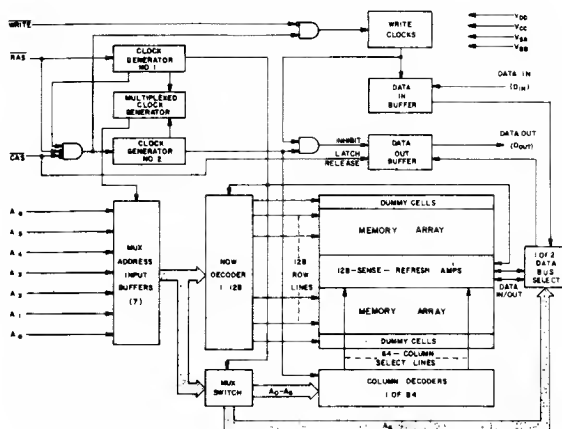
FEATURES

- Extended operating temperature range ($-55^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$)
- Recognized industry standard 16-pin configuration from Mostek
- 150ns access time, 320ns cycle (MKB4116-82)
200ns access time, 375ns cycle (MKB4116-83)
250ns access time, 410ns cycle (MKB4116-84)
- $\pm 10\%$ tolerance on all power supplies ($+12\text{V}$, $\pm 5\text{V}$)
- Low power: 462mW active, 30mW standby (max)
- Output data controlled by CAS and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- Common I/O capability using "early write" operation
- Read-Modify-Write, RAS-only refresh, and Page-mode capability
- All inputs TTL compatible, low capacitance, and protected against static charge
- 128 refresh cycles (2msec refresh interval: -83, -84)
- Leadless chip carrier (E) and flat pack (F) available for high density applications, -83/B4
- Ruggedized for use in severe military environments

DESCRIPTION

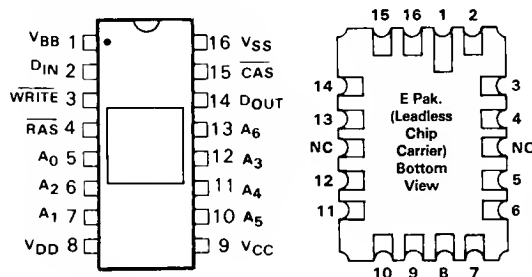
The MKB4116 is a new generation MOS dynamic random access memory circuit organized as 16,384 words by 1 bit. As a state-of-the-art MOS memory device, the MKB4116 (16K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving performance levels in speed and power previously seen only in Mostek's high performance MK4027 (4K RAM).

BLOCK DIAGRAM



The technology used to fabricate the MKB4116 is Mostek's double-poly, N-channel silicon gate, POLY I™ process. This process, coupled with the use of a single transistor dynamic storage cell, provides the maximal circuit density and reliability, while maintaining high performance capability. The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the MKB4116 a truly superior RAM product.

PIN CONNECTIONS



PIN NAMES

A0 - A6	Address Inputs	WRITE	Read/Write Input
CAS	Col. Address Strobe	VBB	Power (-5V)
DIN	Data In	VCC	Power (+5V)
DOUT	Data Out	VDD	Power (+12V)
RAS	Row Address Strobe	VSS	Ground

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB}	-0.5V to +20V
Voltage on V_{DD} , V_{CC} supplies relative to V_{SS}	-1.0V to +15.0V
$V_{BB} - V_{SS}$ ($V_{DD} - V_{SS} > 0V$)	0V
Operating Temperature, T_A (Ambient)	-55°C to +85°C
Storage Temperature (Ambient)	-65°C to +150°C
Short Circuit Output Current	50mA
Power Dissipation	1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

(-55°C ≤ T_A ≤ +85°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	10.8	12.0	13.2	Volts	2
V_{CC}	Supply Voltage	4.5	5.0	5.5	Volts	2,3
V_{SS}	Supply Voltage	0	0	0	Volts	2
V_{BB}	Supply Voltage	-4.5	-5.0	-5.5	Volts	2
V_{IHC}	Input High (Logic 1) Voltage, RAS, CAS, WRITE	2.7	—	7.0	Volts	2
V_{IH}	Input High (Logic 1) Voltage, all inputs except RAS, CAS, WRITE	2.4	—	7.0	Volts	2
V_{IL}	Input Low (Logic 0) Voltage, all inputs	-1.0	—	.8	Volts	2

DC ELECTRICAL CHARACTERISTICS

(-55°C ≤ T_A ≤ +85°C) ($V_{DD} = 5.0V \pm 10\%$; -5.5V ≤ V_{BB} ≤ -4.5V; $V_{SS} = 0V$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{DD1} I_{CC1} I_{BB1}	OPERATING CURRENT Average power supply operating current (RAS, CAS cycling; $t_{RC} = t_{RC}(\min)$)		35 400	mA μA	4 5
I_{DD2} I_{CC2} I_{BB2}	STANDBY CURRENT Power supply standby current ($\overline{RAS} = V_{IHC}$, $D_{OUT} = \text{High Impedance}$)	-10	2.25 10 200	mA μA μA	
I_{DD3} I_{CC3} I_{BB3}	REFRESH CURRENT Average power supply current, refresh mode (RAS cycling, $\overline{CAS} = V_{IHC}$; $t_{RC} = t_{RC}(\min)$)	-10	27 10 400	mA μA μA	4
I_{DD4} I_{CC4} I_{BB4}	PAGE MODE CURRENT Average power supply current, page-mode operation ($\overline{RAS} = V_{IL}$, CAS cycling; $t_{PC} = t_{PC}(\min)$)		27 400	mA μA	4 5
$I_{I(L)}$	INPUT LEAKAGE Input leakage, any input ($V_{BB} = -5V$, $0V \leq V_{IN} \leq +7.0V$, all other pins not under test = 0 volts)	-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, $0V \leq V_{OUT} \leq +5.5V$)	-10	10	μA	
V_{OH} V_{OL}	OUTPUT LEVELS Output high (Logic 1) voltage ($I_{OUT} = -5mA$) Output low (Logic 0) voltage ($I_{OUT} = 4.2mA$)	2.4	0.4	Volts Volts	3 ~

NOTES

1. T_A is specified here for operation at frequencies to $t_{RC} \geq t_{RC}(\min)$. Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met.
2. All voltages referenced to V_{SS} .
3. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the $V_{OH}(\min)$ specifications is not guaranteed in this mode.
4. I_{DD1} , I_{DD3} , and I_{DD4} depend on cycle rate. See Figures 2, 3 and 4 for I_{DD} limits at other cycle rates.
5. I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135 Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.
6. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
7. AC measurements assume t_1 5ns.
8. $V_{IH}(\min)$ or $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} or V_{IL} .
9. The specifications for $t_{PC}(\min)$ $t_{RMW}(\min)$ are used only to indicate cycle which proper operation over the full temperature range ($-55^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$) is assured.
10. Assumes that $t_{RCD} \leq t_{RCD}(\max)$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RCD} will increase by the amount that t_{RCD} exceeds the value shown.
11. Assumes that $t_{RCD} \geq t_{RCD}(\max)$
12. Measured with a load equivalent to 2 TTL loads and 100pF.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS ^(6,7,8) ($-55^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$) ($V_{DD} = 12.0\text{V} \pm 10\%$; $V_{CC} = 5.0\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, $-5.5\text{V} \leq V_{BB} \leq -4.5\text{V}$)

SYM	PARAMETER	MKB4116-82		MKB4116-83		MKB4116-84		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random read or write cycle time	320		375		410		ns	9
t_{RWC}	Read-write cycle time	320		375		425		ns	9
t_{RMW}	Read-modify-write cycle time	320		405		500		ns	9
t_{PC}	Page mode cycle time	170		225		275		ns	9
t_{RAC}	Access time from $\overline{\text{RAS}}$		150		200		250	ns	10,12
t_{CAC}	Access time from $\overline{\text{CAS}}$		100		135		165	ns	11,12
t_{OFF}	Output buffer turn-off delay	0	40	0	50	0	60	ns	13
t_T	Transition time (rise and fall)	3	35	3	50	3	50	ns	8
t_{RP}	RAS precharge time	100		120		150		ns	
t_{RAS}	$\overline{\text{RAS}}$ pulse width	150	5000	200	5000	250	5000	ns	
t_{RSH}	$\overline{\text{RAS}}$ hold time	100		135		165		ns	
t_{CSH}	$\overline{\text{CAS}}$ hold time	150		200		250		ns	
t_{CAS}	$\overline{\text{CAS}}$ pulse width	100	5000	135	5000	165	5000	ns	
t_{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	20	50	25	65	35	85	ns	15
t_{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	0		0		0		ns	
t_{ASR}	Row Address set-up time	0		0		0		ns	
t_{RAH}	Row Address hold time	20		25		35		ns	
t_{ASC}	Column Address set-up time	0		0		0		ns	
t_{CAH}	Column Address hold time	45		55		75		ns	
t_{AR}	Column Address hold time referenced to $\overline{\text{RAS}}$	95		120		160		ns	
t_{RCS}	Read command set-up time	0		0		0		ns	
t_{RCH}	Read command hold time	0		0		0		ns	
t_{WCH}	Write command hold time	45		55		75		ns	
t_{WCR}	Write command hold time referenced to $\overline{\text{RAS}}$	95		120		160		ns	
t_{WP}	Write command pulse width	45		55		75		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (*,7,8)

(-55°C ≤ T_A ≤ +85°C)¹ (V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ± 10%, V_{SS} = 0V, -5.5V ≤ V_{BB} ≤ -4.5V)

SYM	PARAMETER	MKB4116-82		MKB4116-83		MKB4116-84		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t _{RWL}	Write command to $\overline{\text{RAS}}$ lead time	50		70		85		ns	
t _{CWL}	Write command to $\overline{\text{CAS}}$ lead time	50		70		85		ns	
t _{DS}	Data-in set-up time	0		0		0		ns	15
t _{DH}	Data-in hold time	45		55		75		ns	15
t _{DHR}	Data-in hold time referenced to $\overline{\text{RAS}}$	95		120		160		ns	
t _{CP}	$\overline{\text{CAS}}$ precharge time (for page-mode cycle only)	60		80		100		ns	
t _{REF}	Refresh period		2		2		2	ms	19
t _{WCS}	$\overline{\text{WRITE}}$ command set-up time	0		0		0		ns	16
t _{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ delay	60		80		90		ns	16
t _{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ delay	110		145		175		ns	16

AC ELECTRICAL CHARACTERISTICS

(-55°C ≤ T_A ≤ +85°C) (V_{DD} = 12.0V ± 10%; V_{SS} = 0V; -5.5V ≤ V_{BB} ≤ -4.5V)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C _{I1}	Input Capacitance (A ₀ - A ₆), D _{IN}	4	5	pF	17
C _{I2}	Input Capacitance, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WRITE}}$	8	10	pF	17
C _O	Output Capacitance (D _{OUT})	5	7	pF	17,18

NOTES: Continued

13. t_{OP1} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
14. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only, if t_{RCP} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
15. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WRITE}}$ leading edge in delayed write or read-modify-write cycles.

16. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If t_{WCS} ≤ t_{WCS} (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If t_{CWD} ≤ t_{CWD} (min) and t_{RWD} ≤ t_{RWD} (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
17. Effective capacitance calculated from the equation $C = \frac{I_{\Delta V}}{\Delta V}$ with ΔV = 3 volts and power supplies at nominal levels.
18. CAS = V_{IHC} to disable D_{OUT}.

DESCRIPTION (Continued)

Multiplexed address inputs (a feature pioneered by Mostek for its 4K RAMs) permits the MKB4116 to be packaged in a standard 16-pin DIP. This recognized industry standard package configuration, while compatible with widely available automated testing and

insertion equipment, provides highest possible system bit densities and simplifies system upgrade from 4K to 16K RAMs for new generation applications. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

SUPPLEMENTAL DATA SHEET TO BE USED IN CONJUNCTION WITH MOSTEK MK4116-2/3 AND MK4116-4 DATA SHEETS

4096 x 1-BIT STATIC RAM

Processed to MIL-STD-883, Method 5004, Class B

MKB4104 (P/J/E)-84/85

FEATURES

- Extended operating temperature range ($-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$)
- Combination static storage cells and dynamic control circuitry for truly high performance

Part Number	Access Time	Cycle Time
4104(J)-84	250ns	385ns
4104(J)-85	300ns	510ns

- Average power dissipation less than 150mW

- Standby power dissipation less than 53mW
- Single +5V power supply (5% tolerance)
- Fully TTL compatible
 - Fanout: 2 - Standard TTL
 - 2 - Schottky TTL
 - 12 - Low Power Schottky TTL

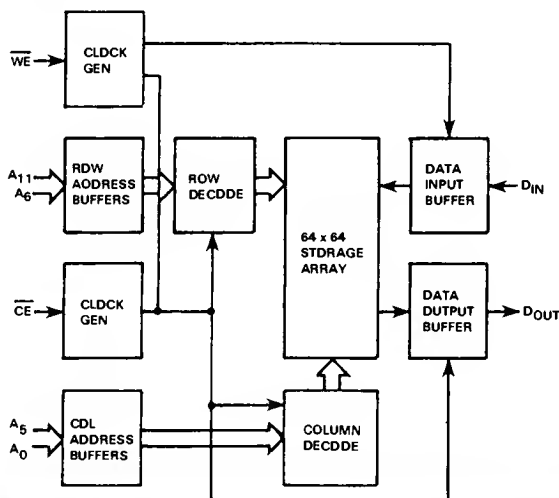
- Standard 18 pin DIP
- Leadless chip carrier (E package) available for high density applications
- Ruggedized for use in severe military environments

DESCRIPTION

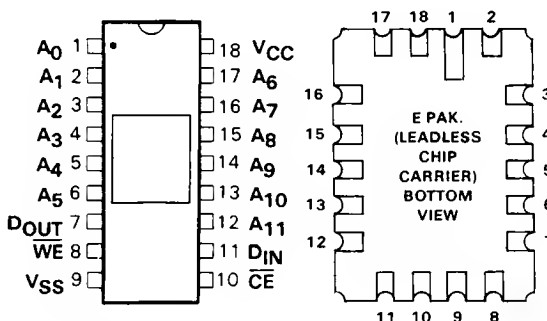
The Mostek MKB4104 is a high performance static random access memory organized as 4096 one bit words. The MKB4104 combines the best characteristics of static and dynamic memory techniques to achieve a TTL compatible, 5 volt only, high performance, low

power memory device. It utilizes advanced circuit design concepts and an innovative state-of-the-art N-channel silicon gate process specially tailored to provide static data storage with the performance (speed and power) of dynamic RAMs. Since the storage cell is static the device may be stopped indefinitely with the $\overline{\text{CE}}$ clock in the off (Logic 1) state.

FUNCTIONAL DESCRIPTION



PIN CONNECTIONS



PIN NAMES

A0-A11 Address Inputs
 $\overline{\text{CE}}$ Chip Enable
 DIN Data Input
 DOUT Data Output

VSS Ground
 VCC Power (+5V)
 WE Write Enable

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS}	–1.0V to +7.0V
Operating Temperature T_A (Ambient)	–55°C to +125°C
Storage Temperature (Ambient)(Ceramic)	–65°C to +150°C
Power Dissipation	1 Watt
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS⁶

(–55°C ≤ T_A ≤ +125°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.4		7.0	V	1
V_{IL}	Logic "0" Voltage All Inputs	–1.0		.65	V	1

DC ELECTRICAL CHARACTERISTICS

(–55°C ≤ T_A ≤ +125°C) (V_{CC} = 5.0 volts ± 5%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		27	mA	2
I_{CC2}	Standby V_{CC} Power Supply Current		10	mA	3
I_{IL}	Input Leakage Current (Any Input)	–10	10	μA	4
I_{OL}	Output Leakage Current	–10	10	μA	3,5
V_{OH}	Output Logic "1" Voltage I_{OUT} = –500μA	2.4		V	11
V_{OL}	Output Logic "0" Voltage I_{OUT} = 5mA		0.4	V	11

AC ELECTRICAL CHARACTERISTICS

(–55°C ≤ T_A ≤ +125°C) (V_{CC} = +5.0 volts ± 5%)

SYM	PARAMETER	MIN	TYP	MAX	NOTES
C_I	Input Capacitance		4pF	6pF	14
C_O	Output Capacitance		7pF	7pF	14

NOTES:

- All voltages referenced to V_{SS}
- I_{CC1} is related to precharge and cycle times. Guaranteed maximum values for I_{CC1} are at minimum cycle time.
- Output is disabled (open circuit), \overline{CE} is at logic 1
- All device pins at 0 volts except pin under test at 0. V_{IN} = 5.5V (V_{CC} = 5V)
- 0V = V_{OUT} = 5.5V (V_{CC} = 5V)
- During power up, \overline{CE} and \overline{WE} must be at V_{IH} for minimum of 2ms after V_{CC} reaches 4.75V, before a valid memory cycle can be accomplished
- Measured with load circuit equivalent to 2 TTL loads and C_L = 100pF
- If \overline{WE} follows after \overline{CE} by more than t_{WYS} , then data out may not remain open circuited
- Determined by user. Total cycle time cannot exceed t_{CF} max
- Data in set-up time is referenced to the later of the two falling clock edges \overline{CE} or \overline{WE}
- AC measurements assume t_I = 5ns. Timing points are taken at 8V and 2.0V on inputs and 8V and 2.0V on the output. Transition times are also taken between these levels
- t_C = t_{CL} + t_P + $2t_I$
- The true level of the output in the open circuit condition will be determined totally by output load conditions. The output is guaranteed to be open circuit within t_{OFF}
- Effective capacitance calculated from the equation $C = \frac{1 \Delta t}{\Delta V}$ with ΔV equal to 3V and V_{CC} nominal
- For RMW, t_{CE} = t_{AC} + t_{WPL} + 5MOD
- t_C = t_{AC} + t_{WPL} + t_P + $3t_I$ + 1MOD

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS^{6,11}
 $(-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}) (V_{CC} = +5.0 \text{ Volts} \pm 5\%)$

SYM	PARAMETER	MKB4104-84		MKB4104-85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_C	Read or Write Cycle Time		410	510		ns	12
t_{AC}	Random Access		250		300	ns	7
t_{CE}	Chip Enable Pulse Width	250	5000	300	5000	ns	15
t_P	Chip Enable Precharge Time	150		200		ns	
t_{AH}	Address Hold Time	135		165		ns	
t_{AS}	Address Set-Up Time	0		0		ns	
t_{OFF}	Output Buffer Turn-Off Delay	0	65	0	75	ns	13
t_{WS}	Write Enable Set-Up Time	0		0		ns	8
t_{DHC}	Data Input Hold Time Referenced to CE	210		250		ns	
t_{DHW}	Data Input Hold Time Referenced to WE	90		105			
t_{WW}	Write Enabled Pulse Width	60		90		ns	
t_{MOD}	Modify Time	0	5000	0	5000	ns	9
t_{WPL}	WE to CE Precharge Lead Time	85		105		ns	10
t_{DS}	Data Input Set-Up Time	0		0		ns	
t_{WH}	Write Enable Hold Time	185		225		ns	
t_T	Transition Time	5	50	5	50	ns	
t_{RMW}	Read-Modify-Write Cycle Time	500		620		ns	16
t_{RS}	Read Set-Up Time	0		0		ns	

DESCRIPTION (Continued)

All input levels, including write enable (\overline{WE}) and chip enable (\overline{CE}) are TTL with a one level of 2.4 volts and a zero level of .65 volts. The push-pull output (no pull-up resistor required) delivers a one level of 2.4V minimum and a zero level of .4 volts maximum. The output has a fanout of 2 standard TTL loads or 12 low power Schottky loads.

The RAM employs an innovative static cell which occupies a mere 2.75 square mils ($\frac{1}{2}$ the area of previous cells) and dissipates power levels comparable to CMOS. The static cell eliminates the need for refresh cycles and associated hardware thus allowing easy system implementation.

Power supply requirement of +5V combined with TTL compatibility on all I/O pins permits easy integration into large memory configurations. The single supply reduces capacitor count and permits denser packaging on printed circuit boards. The 5V only supply requirement and TTL compatible I/O makes this part an ideal choice for next generation +5V only micro-processors such as Mostek's Z80. The early write mode (\overline{WE} active prior to \overline{CE}) permits common I/O operation, needed for Z80 interfacing, without external circuitry.

Reliability is greatly enhanced by the low power dissipation which causes a maximum junction rise of only 6.6° at 1.6 Megahertz operation. The MKB4104 was designed for the system designer and user who require the highest performance available along with Mostek's proven reliability.

**SUPPLEMENTAL DATA SHEET TO BE USED IN CONJUNCTION
WITH MOSTEK MK4104(P/N) DATA SHEET**

1K x 8-BIT STATIC RAM

Processed to MIL-STD-883, Method 5004, Class B

MKB4118(P/J)-82/83

FEATURES

- ❑ Extended Operating Temperature Range
($-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$)
- ❑ Address Activated™ Interface combines benefits of Edge Activated™ and full static
- ❑ High performance

PART NUMBER	ACCESS TIME	CYCLE TIME
MKB4118-82	150 nsec	150 nsec
MKB4118-83	200 nsec	200 nsec

- Single +5 volt power supply

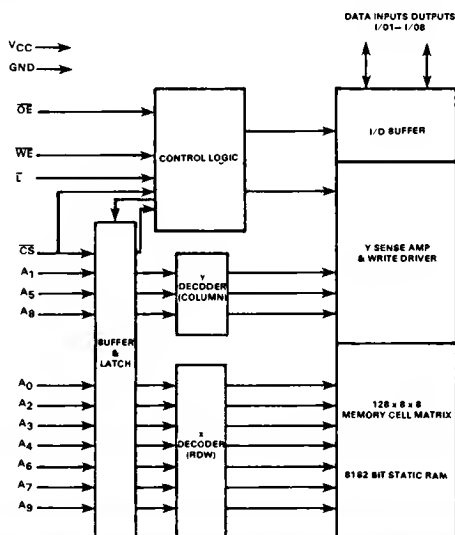
- ☐ TTL compatible I/O
 - Fanout: 2 - Standard
 - 2 - Standard TTL
 - 2 - Schottky TTL
 - 12 - Low power Schottky TTL
- ☐ Low Power - 400mW Active
- ☐ 24-pin ROM/PROM compatible pin configuration
- ☐ \overline{CS} , \overline{OE} , and \overline{LATCH} functions for flexible system operation
- ☐ Read-Modify-Write Capability
- ☐ Ruggedized for use in severe military environment

DESCRIPTION

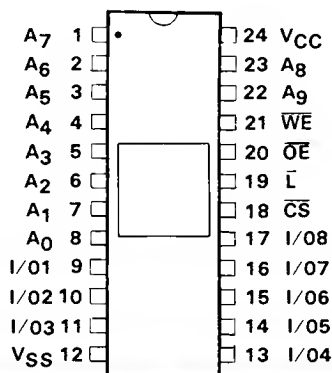
The MKB4118 uses Mostek's Poly R N-Channel Silicon Gate process and advanced circuit design techniques to package 8192 bits of static RAM on a single chip. Mostek's Address Activated™ circuit design technique

is utilized to achieve higher performance, low power, and easy user implementation. The device has a $V_{IH} = 2.2$, $V_{IL} = 0.8V$, $V_{OH} = 0.4V$ making it totally compatible with all TTL family devices.

BLOCK DIAGRAM



PIN CONNECTIONS



PIN NAMES			
A0 - A9	Address Inputs	\overline{WE}	Write Enable
CS	Chip Select	\overline{OE}	Output Enable
VSS	Ground	L	Latch
VCC	Power (+5V)	I/O ₁ I/O ₈	Data In/ Data Out

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS}	-0.5V to +7.0V
Operating Temperature	-55°C to +125°C
Storage Temperature (Ambient)(Ceramic)	-65°C to +150°C
Power Dissipation	1 Watt
Short Circuit Output Current	20mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS³

(-55°C ≤ T_C ≤ +125°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.4		7.0	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3		.8	V	1

DC ELECTRICAL CHARACTERISTICS^{1,3}

(-55°C ≤ T_C ≤ +125°C) (V_{CC} = 5.0 Volts ± 5%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current (Active)		100	mA	
I_{CC2}	Average V_{CC} Power Supply Current (Standby)		80	mA	5
I_{IL}	Input Leakage Current (Any Input)	-10	10	μA	2
I_{OL}	Output Leakage Current	-10	10	μA	2
V_{OH}	Output Logic "1" Voltage I_{OUT} = -1mA	2.4		V	
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4mA		0.4	V	

AC ELECTRICAL CHARACTERISTICS^{1,3}

(-55°C ≤ T_C ≤ +125°C) (V_{CC} = +5.0 Volts ± 5%)

SYM	PARAMETER	TYP	MAX	NOTES
C_I	Capacitance on all pins except I/O	4pF		4
$C_{I/O}$	Capacitance on I/O pins	10pF		4

NOTES:

1. All voltages referenced to V_{SS} .
2. Measured with $0 \leq V_I \leq 5V$ and outputs deselected (V_{CC} = 5V)
3. A minimum of 2ms time delay is required after application of V_{CC} (+5V) before proper device operation can be achieved.
4. Effective capacitance calculated from the equation $C = I \frac{\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} nominal
5. Standby mode is defined as condition with addresses, latch and WE remain unchanged.
6. AC timing measurements made with 2 TTL loads plus 100pF.

ELECTRICAL CHARACTERISTICS⁶

($-55^{\circ}\text{C} \leq T_C \leq 125^{\circ}\text{C}$ and $V_{CC} = 5.0 \text{ Volts} \pm 5\%$)

SYM	PARAMETER	MKB4118-82		MKB4118-83		UNIT	NOTES
		MIN	MAX	MIN	MAX		
t _{RC}	Read Cycle Time	150		200		ns	
t _{AA}	Address Access Time		150		200	ns	
t _{CSA}	Chip Select Access Time		75		100	ns	
t _{CSZ}	Chip Select Data Off Time	0	75	0	100	ns	
t _{OEa}	Output Enable Access Time		75		100	ns	
t _{OEZ}	Output Enable Data Off Time	0	75	0	100	ns	
t _{AZ}	Address Data Off Time	10		10		ns	
t _{ASL}	Address to Latch Setup Time	10		10		ns	
t _{AHL}	Address From Latch Hold Time	50		65		ns	
t _{CSL}	CS To Latch Setup Time	0		0		ns	
t _{CHL}	CS From Latch Hold Time	50		65		ns	
t _{LA}	Latch Off Access Time		200		260	ns	
t _{WC}	Write Cycle Time	150		200		ns	
t _{ASW}	Address To Write Setup Time	0		0		ns	
t _{AHW}	Address From Write Hold Time	50		65		ns	
t _{CSW}	CS to Write Setup Time	0		0		ns	
t _{CHW}	CS From Write Hold Time	50		65		ns	
t _{DSW}	Data to Write Setup Time	30		40		ns	
t _{DHW}	Data From Write Hold Time	30		40		ns	
t _{WD}	Write Pulse Duration	50		60		ns	
t _{LDH}	Latch Duration, High	50	DC	60	DC	ns	
t _{LDL}	Latch Duration, Low		DC		DC	ns	
t _{WEZ}	Write Enable Data Off Time	0	75	0	100	ns	
t _{LZ}	Latch Data Off Time	10		10		ns	
t _{WPL}	Write Pulse Lead Time	90		130		ns	

**SUPPLEMENTAL DATA SHEET TO BE USED IN
CONJUNCTION WITH MOSTEK MK4118(P/N) SERIES DATA SHEET**

The MKB4118 is designed for all wide word memory applications. The MKB4118 provides the user with a high-density, cost-effective 1K x 8 bit Random Access Memory. Fast Output Enable (\overline{OE}) and Chip Select (\overline{CS}) controls are provided for easy interface in micro-processor or other bus-oriented systems. The MKB4118 features a flexible Latch (\overline{L}) function to permit latching of

the address and \overline{CS} status at the user's option. Common data address bus operation may be performed at the system level by utilizing the \overline{L} and \overline{OE} functions for the MKB4118. The latch function may be bypassed by merely tying the latch pin to V_{CC} , providing fast ripple-through operation.

X	Dynamic Random Access Memory	DYNAMIC RAMS
XI	Static Random Access Memory	STATIC RAMS
XII	Read Only Memory	ROMS
XIII	Technology	TECHNOLOGY
XIV	Memory Systems	MEMORY SYSTEMS

MOSTEK®

DYNAMIC MOS RAMS

Technology

ABSTRACT

This paper discusses the evolution of dynamic MOS RAMs. Included is a discussion of address multiplexing and timing considerations of multiplexed address MOS RAMs. Static and dynamic sense amplifiers are compared in terms of power consumption and layout problems and the benefits resulting from the use of dynamic sense amplifiers are discussed. Data sheet specifications of three presently available 16K dynamic MOS RAMs are presented.

INTRODUCTION

Semiconductor random access memories have been developed at a very rapid pace throughout this decade. RAMs with very impressive performance have been produced using bipolar technology, while RAMs with moderate performance but very low cost have been produced using MOS technology. This paper will discuss dynamic MOS random access memories which are rapidly replacing core memories in most memory applications. This recent dominance by dynamic MOS RAMs in the random access memory market comes about as a result of the cost, performance, and reliability associated with the integration of up to 16,384 bits of RAM on a single integrated circuit. This level of integration in turn is made possible by the use of dynamic circuit techniques, and more specifically by the use of dynamic data storage. These techniques have undergone very rapid development, causing the performance characteristics of available memory circuits to vary greatly from design to design as different techniques are incorporated. Dynamic and static sense amplifiers will be discussed, and the performance specifications of a commercially available 16K RAM using dynamic sense amplifiers will be compared to the specifications of two 16K RAMs using static sense amplifiers. The state-of-the-art in commercially available MOS memory is a 16K x 1 dynamic circuit with a chip access time of 150 nanoseconds, and a read-modify-write cycle time of 320 nanoseconds. Cost of dynamic MOS memory is rapidly decreasing and is now about 0.1 cent per bit at the chip level and about 0.15 cent per bit at the system level.

DEVELOPMENT OF DYNAMIC MEMORY

The first MOS RAMs used cross-coupled flip-flops as storage cells, each cell containing six or eight MOS transistors. The combination of a complex cell structure and a new technology gave rise to a high per-bit memory cost that found very few applications. But applications were expanded by major breakthroughs that significantly reduced the cost of MOS RAM. The first breakthrough was the development of the concept of dynamic memory storage — storing a digital "0" or "1" by a low or high voltage stored on a capacitor in a 3-transistor cell. However, this can cause a problem since the charge will eventually leak off any capacitor. If data is to be retained for longer than the self discharge time of a cell storage capacitor, typically two milliseconds, the data must be sensed before it is lost and then restored to its original voltage level. The operation of restoring the cell voltages to good levels is called a refresh operation. This simultaneously occurs in all cells of the externally addressed row of the memory matrix. To refresh the entire memory array, it is necessary to perform a refresh cycle to each of the 16 to 128 rows of the memory array at least once every two milliseconds.

The second major breakthrough in the development of MOS RAMs was the development of the single transistor cell. This cell is poorly named because it really consists of a single transistor plus a single capacitor, and the capacitor occupies the majority of the cell area. But this cell still occupied less than half the area of the earlier 3-transistor cell and permitted integration of 4096 bits per chip compared to only 1024 bits per chip using the earlier 3-transistor cell. The three year delay between the introduction of the 1-transistor cell was due to the difficulty in sensing the small signal from the 1-transistor cell. For the first time, there was no amplifier built into every cell, and signal levels out of the memory matrix became millivolts instead of volts. Sense amplifiers have been developed to sense the small signals from the 1-transistor cell and will be discussed later.

The 1-transistor cell permitted integration of 4K bits per chip. In addition, improvements in the inter-

nal peripheral or support circuits made this new generation of circuits much easier to use than were the earlier 1K circuits. The 1K circuits required multiple, critically-timed, high-capacitance, high-voltage clock signals. In the 4K chips, these were replaced by a single high-voltage, high-capacitance clock (22 pin version) or two TTL-level, low-capacitance clocks (16 pin version). The 1K chips required high voltages for address and data inputs, which were replaced by TTL-level inputs in the 4K chips. The high impedance output of the 1K chips, requiring an external sense amplifier, was replaced by a low impedance output capable of driving one or more TTL loads in the 4K circuits. The relatively slow P-channel technology used for the 1K chips was replaced by faster N-channel technology for the 4K chips. Integration of 4096 bits per chip reduced the per-bit chip cost, while the simplification of external support circuitry reduced other system costs. These savings made MOS memory cost competitive with magnetic core for the first time in most general applications. Integration of 16,384 bits per chip promises to reduce the per-bit cost even further. Although 16K chips require the same external support circuitry as that required by 4K chips, a given printed circuit board size, power supply, cooling system, set of address buffers, etc., supports four times as many bits when using 16K chips as when using 4K chips. Memory systems using 16K chips should become less expensive than those using 4K chips some time in the first half of 1978.

ADDRESS MULTIPLEXING

While use of the single transistor cell increased the bit density on a chip, it degraded the access time by about 25 percent. This is due to the delay through the sense amplifiers in detecting and amplifying the very small signals from the memory cells. This delay, however, made the multiplexing of addresses a very attractive means for reducing package pin count for increased memory density on a printed circuit board.

An MOS memory chip is physically arranged as a two dimensional array of cells. Certain address inputs are used for row selection and the remaining address inputs are used for column selection. Row selection is required before the sense amplifiers can begin their slow detection process. Column selection is not required until the outputs of the sense amplifiers are valid, since its function is to gate data from the selected sense amplifier to the data output circuitry. Since the column selection information is not used internally until well after the row selection information is required, only the row addresses need to be available to the chip at the start of a cycle. The column address can come later with no penalty of access time. The multiplexed address memory takes advantage of this delayed need for column address. Instead of using 12 address pins to select one of 4096 memory cells, six address pins are used to

first select one of 64 rows, and subsequently the same pins are used to select one of 64 columns. The result is a 4096 bit RAM in a 16 pin package, rather than in the more straightforward 22 pin package.

When compared to the 22 pin 4K RAM, the 16 pin 4K RAM has both advantages and disadvantages. The primary advantage of the 16 pin approach is the substantial increase in board density that it allows. A second advantage is the reduction in the required number of address buffers from 12 to 6. A third advantage is that multiplexing permits a faster mode of operation, called page mode, which shall be discussed later. Finally, two more specific advantages were available to users of the 16 pin design. These were the use of TTL-level timing signals rather than a high voltage clock, and the use of dynamic sense amplifiers rather than static sense amplifiers to reduce power consumption. These last two differences were not a result of the multiplexing but were nevertheless, advantageous for users of the 16 pin design. .

The 16 pin implementation also had disadvantages. The multiplexed part required two timing signals and hence more complex timing. The first signal, RAS, initiates a cycle and strobes in the row address, and the second signal, CAS, strobes in the column address. Any skew in the timing of the second signal with respect to the first added directly to access time. Systems using the 22 pin design, which required only a single clock, had less complex timing and suffered no such degradation of access time. Finally, the 22 pin design, not having the TTL to MOS level clock driver on the chip, dissipated less than 1 mW in the standby mode compared to about 10 mW per chip for the 16 pin part.

In the first year after various designs were introduced, the 22 pin approach gained greater acceptance than the 16 pin approach, not because of the technical advantages or disadvantages of the two approaches, but because there were two major MOS memory suppliers manufacturing the 22 pin part and only one manufacturing the 16 pin part. Many users would not choose a single-sourced product. Other users had a strong enough preference for the multiplexed concept to commit to that design, correctly assuming that the market they created for the 16 pin design would cause additional manufacturers to offer their own 16 pin designs. Meanwhile, the 16 pin design was improved to eliminate the access time penalty due to multiplexing. This was accomplished by performing the critical timing of the second clock with circuitry on the chip rather than with external circuitry—a feature referred to as “gated CAS.” With many users committed to a multiplexed design, other manufacturers began supplying this part. And with multiple sourcing available, more and more users designed systems using the 16 pin part. This trend has escalated to the point where virtually all new memory system designs now incorporate the 16 pin device.

The acceptance of address multiplexing generated by 4K RAMs virtually assured its use in the next generation of dynamic MOS RAMs. And indeed all 16K RAMs on the market today use address multiplexing and are pin compatible with each other. Many new memory system designs take advantage of the pinout similarity between the 4K and 16K parts. Printed circuit boards are designed to accommodate either part, with only a single jumper wire required to switch from 4K to 16K chips, caused by the need for a seventh address pin on the 16K part, which replaces the chip select pin of the 4K part. Chip selection is accomplished on the 16K part by decoding \overline{RAS} or \overline{CAS} or both.

MULTIPLEX TIMING CONSIDERATIONS

Although address multiplexing provides some very substantial system benefits, it complicated system timing. It requires that both row and column addresses get into the chip in a short time using the same address pins. This establishes a rather tight timing window during which the individual events must occur. The sequence of events required to address the chip is as follows: (1) establish row addresses, (2) bring \overline{RAS} low, (3) maintain row addresses valid for some minimum hold time, (4) establish column addresses, (5) bring \overline{CAS} low, and (6) hold column addresses valid for some minimum time. To achieve specified access time from \overline{RAS} , it is necessary to bring \overline{CAS} low within some specified maximum delay after \overline{RAS} .

Every attempt is made during the design of multiplexed chips to simplify the system timing problem. This is done by first reducing the row address hold time to an absolute minimum, since the system must not begin to establish column addresses until the minimum row address hold time is met. Then, if possible, the design is made to tolerate a negative set-up time for the column addresses, which means that column addresses need not be valid until some time after \overline{CAS} starts low. This also increases the time available for multiplexing. Finally, the critical \overline{RAS} to \overline{CAS} timing is done on the chip, which means that if \overline{CAS} occurs earlier than needed by the chip, it is internally delayed until it is needed ("gated \overline{CAS} "). For high performance memory systems, the use of a delay line to minimize timing skews is essential. With a delay line, the timing sequence can be net such that \overline{CAS} occurs early enough after \overline{RAS} to guarantee the specified access time from \overline{RAS} .

OPERATION OF MULTIPLEXED DYNAMIC RAMS

In a multiplexed design, the 12 addresses of a 4K memory or the 14 addresses of a 16K memory are strobed into the memory chip in two groups of 6 or 7 respectively. When an address becomes available for a memory operation, the row address must

first be presented to the chip address pins. As soon as the row address inputs are valid, the first of two timing signals to the chip initiates a cycle. This signal strobes or latches the row address into the chip and is appropriately called Row Address Strobe or \overline{RAS} . With no further commands to the chip, the latched addresses are converted to MOS voltage levels, decoded, and the selected row is enabled. Data is thereby destructively read from each cell in the selected row by dumping its charge onto its respective column sense line. A sense amplifier for each column detects the change in voltage level on the column line resulting from this deposited charge, and amplifies this signal. The amplified signals from the sense amplifiers are then impressed back onto the column sense lines, returning the cells to their original voltages. A cell whose voltage had decayed is restored to its original voltage in the process. At this time the sense amplifiers contain the same data or information contained in the selected row, and the destructively-read cells in the row are restored (refreshed) to their proper voltage.

When an active cycle is initiated by \overline{RAS} going low, it must not be aborted. It is necessary to keep \overline{RAS} low for some minimum length of time to allow the sense amplifiers time to restore data back into the destructively-read cells. To summarize, the function of the Row Address Strobe is to initiate a cycle, strobe or latch the row address, enable the selected row of memory cells, sense and restore the data in that row of memory cells, and maintain the sensed data from the entire row of addressed memory cells in their respective sense amplifiers. The sense amplifiers maintain this data as long as \overline{RAS} remains active. At the end of a cycle, when \overline{RAS} is taken high, the selected row is immediately turned off, isolating the correct data in the cells. After the row is off, the half-digit lines are prepared for a new cycle.

The Column Address Strobe (\overline{CAS}), on the other hand, controls column selection circuitry and the transfer of data from the selected sense amplifier to the output circuitry. After \overline{RAS} strobes the row address information from the multiplexed address input pins, \overline{CAS} strobes the column address from the same pins. When \overline{CAS} goes active (low), the column address is strobed or latched into the circuit. This address is then decoded to select the proper column. Data from the selected sense amplifier is then transferred to the output buffer, completing read access.

During a write operation, the same sequence of events occurs as in a read cycle, with identically the same timing as in a read cycle except that the write enable signal, \overline{WRITE} , is brought active (low). This causes the data at the data input to be strobed into the chip, buffered, and written into the selected sense amplifier and, thereby, into the selected cell. A read-modify-write cycle starts out as a read cycle until read access

time. Then when input data becomes available to the memory, **WRITE** must be activated. As in a write-only cycle, this causes the data to be written into both the selected sense amplifier and into the selected cell. The active cycle must not be terminated until the internal write circuitry has had sufficient time to complete the write operation.

PAGE MODE OPERATION

The Row Address Strobe transfers the data from an entire row of memory cells into their respective sense amplifiers. The Column Address Strobe transfers the single bit of data from the selected sense amplifier into the output buffer. This organization permits data to be transferred into or out of multiple column locations of the same row by having multiple column cycles during a single active row cycle. This mode of operation is called page mode. A page of memory is defined as those memory locations sharing a common row address, but not necessarily confined to a single chip.

After a row has been selected by the Row Address Strobe, the contents of all cells in that row are available in their respective sense amplifiers. Repetitive column address cycles, while maintaining a single active row cycle, permit faster operation than is possible in the normal operating mode. This is because the delay through the sense amplifier only adds to the access time of the first column in the page. Data to be accessed from each subsequent column is already available in its respective sense amplifier. Therefore, page mode access is the access time from **CAS**, which is typically two-thirds the access time from **RAS**. Page mode reduces power consumption while typically doubling maximum operating frequency. Read, write, and read-modify-write cycles can be performed in either normal cycles or in page cycles. Page mode operation has a number of applications, with high-speed block transfer of data being the most important.

SENSE AMPLIFIER CONSIDERATIONS

The one-transistor memory cell has been simplified to a rather minimal structure: a capacitor stores digital data as a high or low voltage, and a transistor selectively connects the capacitor to a digit/sense line. (See Fig. 1.) Conduction through the transistor is controlled by its gate which is electrically connected to the other gates in a row. When a row is enabled by the row decoder, all transistors in that row become conductive, transferring charge from their respective capacitors to their respective digit/sense lines, destructively reading data. Each column has its own sense amplifier, whose function is to detect this charge and to amplify the signal caused

by this charge. The amplified signal is a full logic level, either at ground or close to V_{DD} .

The cell transistors remain conductive throughout this period so that the amplified signals from the sense amplifiers feed back into their respective cells, refreshing the voltage levels in the cells.

To maximize the signal into the sense amplifier, a large cell capacitance and a small digit/sense line capacitance are desired. This is because the cell and its digit line form a capacitive divider that attenuates the signal from the cell. But integration of large numbers of bits on one circuit requires a physically small cell size which implies an electrically small cell capacitance. Integration of large numbers of bits also requires that many cells share a common digit/sense line, causing this line to be physically long and to therefore have high stray capacitance. To keep the signal attenuation to an acceptable level, steps are taken to both maximize cell capacitance and to minimize digit line capacitance. Cell capacitance can be increased by using a double layer polysilicon fabrication process, which increases the percentage of cell area used for the capacitor. Digit line capacitance can be reduced by simply cutting the line in half. The sense amplifier is then placed in the center of a digit line, and senses a differential voltage between the two halves of the line. In 16K designs, the cell capacitance is typically 0.04 picofarad and the stray capacitance of one half-digit is typically 1 picofarad. Thus the signal from the memory cell is attenuated by a factor of 25 before being sensed by the sense amplifier.

Between cycles, the two halves of each digit line are equilibrated to precisely the same voltage. When an active cycle is initiated by **RAS** going low, these lines are momentarily allowed to float. Then a row is enabled, transferring charge from the enabled cell in each column to its half of its digit line. On each digit line, only a single memory cell is selected. This cell may be located on either the top or bottom half of the digit line. If the cell was originally at a high voltage, it causes its half-digit line voltage to be at some "high" value. If the cell was originally at a low voltage, its resulting half-digit line voltage is some "low" value. It should be noted that the attenuation of the digit line causes the "high" and "low" voltages to differ by less than one-half volt. The half-digit line not containing the addressed cell is simultaneously adjusted to a voltage somewhere between the "high" and "low" voltages of the addressed half by a special cell called a "dummy cell." Thus if a cell originally contained a high voltage, the voltage of its half-digit line will be approximately one-quarter volt above the adjusted intermediate voltage of the other half-digit line. If the cell originally contained a low voltage, the voltage of its half-digit line will be approximately one-quarter volt below the intermediate

voltage of the other half-digit line. It is now up to the sense amplifier to detect this differential signal of one-quarter volt or less.

A detailed analysis of the sense amplifier will not be attempted. It will simply be noted that the sense amplifier consists of a balanced flip-flop. Since the addressed cell, in conjunction with the dummy cell, guarantees an initial voltage imbalance to this flip-flop, the positive feedback of the flip-flop causes it to latch up. The half-digit line having the lower initial voltage goes to ground while the other half-digit line goes to or in the case of a dynamic sense amplifier, remains near V_{DD} .

Two types of sense amplifiers have been used in commercially available products. These are variations of the static amplifier in Fig. 1, and of the dynamic amplifier in Fig. 2. Both are about equal in their ability to detect and amplify small signals. The load resistors, R1 and R2, in the static amplifiers consume a substantial amount of power, typically half or more of the total chip power. Since these resistors are not present in dynamic amplifiers, the total power consumption of memory chips employing dynamic sense amplifiers is much less than that of circuits employing static sense amplifiers. There are, however, formidable design or layout problems associated with the use of dynamic sense amplifiers which will be discussed presently. These problems are severe enough that many chip designers chose to incorporate power-consuming static sense amplifiers into their designs.

To understand the differing circuit requirements for static and dynamic sense amplifiers, one must look at a write cycle or more accurately, a read-modify-write cycle. Suppose, in Fig. 1, cell 64 had originally stored a low voltage and was read. The sense amplifier, detecting a lower voltage on node B than on node A, will drive node B to ground and node A near V_{DD} . Transistor T3 then turns on, and the data from the cell becomes available to the output buffer at one end of the data bus. Now, assume that it is desired to write opposite data back into the cell. This requires forcing a high voltage onto node B and onto the storage capacitor, C64. To do this, the data input buffer will drive the input/output data bus to ground. Transistor T3 then forces node A to ground, overpowering R1. When node A goes to ground, transistor T2 turns off. This allows R2 to pull node B to V_{DD} as required to write the high level into the storage cell. Without R2, node B would simply remain at ground, and a high voltage could not have been written into the cell. With these resistors, data can be written into a cell in either half of the matrix with a single input/output data bus. A trade-off exists in the resistance value chosen for R1 and R2. Since either R1 or R2 will dissipate power in all of the sense amplifiers, a low value resistor results in a very high

power consumption. But the digit line capacitance of node B is quite large, and a high value resistor means an excessively long write time. There is no good compromise, and circuits using static sense amplifiers consume high power and have long write times.

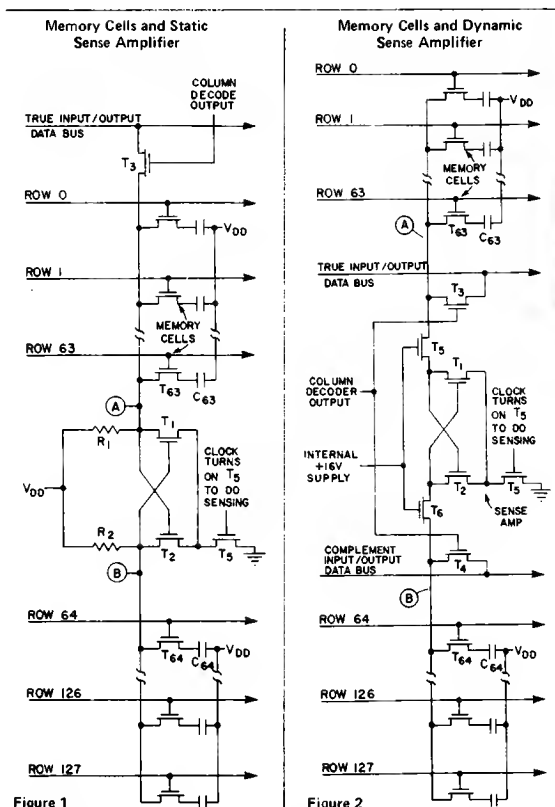


Figure 1 Memory Cells and Static Sense Amplifier. Memory chips using static sense amplifiers consume twice the power of chips using dynamic sense amplifiers, due to the conduction through either R1 or R2.

Figure 2 Memory Cells and Dynamic Sense Amplifier. The use of dynamic sense amplifiers requires both true and complement input/output data busses. This, in turn, requires either two full column decoders or placement of a single column decoder with the sense amplifiers in the center of the memory.

On paper, the dynamic sense amplifier solves the problem very well. Referring now to Fig. 2 and having again read a low voltage from cell 64, assume it is again desired to write a high voltage back into the cell. Now, as before, the input buffer drives the true data bus to ground, with transistor T3 causing node A to follow. But, in addition the input buffer also forces the complement data bus to V_{DD} , with transistor T4 causing node B to follow. In forcing node B to V_{DD} , the complement data bus performed the job previously done by the resistor. With row 64 still selected, the high voltage on node B is transferred into the cell, and the write operation is complete. It should be noted that transistors T3 and T4 function only as switches and can have very low resistances to

speed-up write time. No speed—power trade-off is involved. Therefore, memory designs using dynamic sense amplifiers consume far less power and write much faster than do designs using static sense amplifiers.

The layout problem associated with the dynamic sense amplifier is that it requires both a true and a complement data bus. These, in turn, require that the column decode outputs be available in both the top and bottom halves of the memory array. Placing single column decoder above (or below) the memory array is ruled out since it is not practical to run its outputs through the memory array to the other side. One solution to the layout problem is to use two entire column decoders, one above the top half of the array to service the true data bus, and the other below the bottom half of the array to service the complement data bus. This gains all the advantages of using dynamic sense amplifiers, but the duplication of the column decoder consumes a substantial amount of silicon area, thereby raising the cost of the chip.

A second solution is to use a single column decoder located in the center of the memory array along with the sense amplifiers. This approach requires great care in design. If the column decoder is located in the center of the chip, it is topologically necessary for the digit lines to cross the buffered column address signals. Just one address signal, moving from ground to V_{DD} , capacitively couples more signal onto a digit line than that provided by the memory cell. At first thought, this is frightening indeed. But on second thought, there are 127 unselected row lines that cross the digit lines and they do not cause a problem. They are quiet. Indeed if all lines crossing the digit line are kept quiet until the sense amplifier detects and amplifies its signal, there is no problem. With a multiplexed design, it is particularly easy to insure that the buffered column address lines remain quiet during this time, since multiplexing automatically causes the column address to be processed after the row addresses have been processed.

The advantages of dynamic sense amplifiers over static sense amplifiers are rather dramatically illustrated in Table 1. The power differences between the MK4116 and the other parts is due almost entirely to the choice of sense amplifiers. So is the write time. Other performance differences between the various designs are due to alternate circuit techniques used throughout the designs, not necessarily related to the choice of sense amplifier.

OTHER MOS RAMS

The very small area occupied by a single-transistor cell makes dynamic MOS RAM substantially less

Table 1

PART NUMBER	MK4116-2 MOSTEK	2116-2 (INTEL)	TMS 4070-2 (TI)
SENSE AMP	DYNAMIC	STATIC	STATIC
MAX I_{DD} (mA)	35	69	76
V_{DD} TOLERANCE	±10%	±10%	±5%
ACCESS TIME (FROM \overline{RAS}) (ns)	150	200	250
ACCESS TIME (FROM \overline{CAS}) (ns)	100	125	165
MAX \overline{RAS} to \overline{CAS} delay for specified \overline{RAS} access (ns)	50	75	80
Row Address Hold Time (ns)	20	45	50
Col Address Setup Time (ns)	—10	—10	0
WRITE TIME After READ	60	125	165
MIN READ or WRITE CYCLE (ns)	375	350	400
MIN READ- MODIFY-WRITE CYCLE	375	400	590
REFRESH Cycles REFRESH Interval	128 2ms	64 2ms	128 2ms
PAGE MODE	Yes	Yes	Yes
Package Pins	16	16	16

DATA SHEET SPECIFICATIONS FOR COMMERCIALLY AVAILABLE 16K MOS RAMs. All numbers pertain to fastest speed selection.

expensive than other forms of MOS RAM. For many applications, however, other forms of MOS RAM deserve consideration. All of the RAMs described below operate from a single +5 volt supply, compared to the +12, +5, and —5 volt supplies required by dynamic RAMs. All use static cells, eliminating the refresh cycles required by dynamic RAMs. These circuits are not multiplexed, simplifying system timing. These considerations make this group particularly attractive in small memory systems.

By using dynamic circuit techniques with a static (flip-flop) cell, low active power and even lower standby power can be achieved. Such 4K RAMs are now available with under 100 mW active power and under 10 mW standby power. Access times are similar to those of dynamic RAMs.

When access time is of paramount importance, static cells are used with static peripheral circuits. This permits access times of 50 nanoseconds or below at

active power levels of about 500 mW, and standby power of about 35 mW. Lower power versions are also available with longer access times.

For applications requiring extremely low power dissipation, complementary MOS RAMs are very attractive. These circuits are the most expensive of the group, but consume nanowatts to microwatts during standby and microwatts to milliwatts when active. They also tolerate extremely wide variations in power supply voltage, often from 3 to 15 volts.

CONCLUSION

Some of the dynamic MOS RAMs on the market today consume considerably less power than others. Some are considerably faster than others. But compared to other technologies, all of these parts represent very attractive building blocks for random access memory systems. The highest power 16K circuits only consume about 35 watts in a 256K work

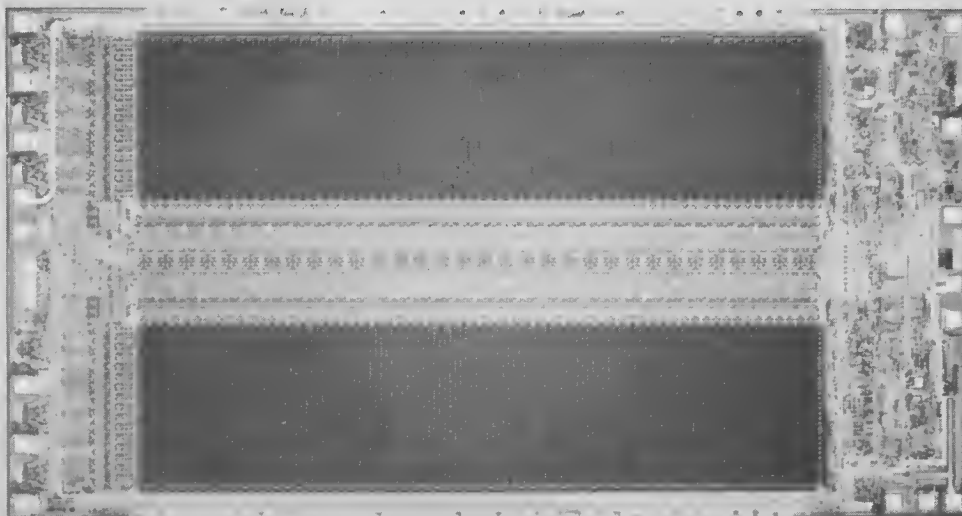
x 32 bit per word system. The slowest circuits permit system access times faster than 500 nanoseconds.

The high storage density resulting from the use of small 16 pin packages, each containing 16K bits, is very important in the design of large memory systems. The combination of TTL compatibility of all inputs and outputs, and relatively straightforward timing requirements make these circuits equally attractive for small memory systems.

In systems requiring extremely fast access times, bipolar technology provides the best answer. In systems tolerant of relatively slow serial access rather than requiring fast random access, other technologies, including disc, CCD, or bubble memories are potentially less expensive than dynamic MOS. But for those applications requiring random access memory of low to moderate performance, the combination speed, power, density, reliability and cost of dynamic MOS memory just can't be matched by any other technology today.

CHIP PHOTOGRAPH OF MK4116

Figure 3



The column decoders are located with the sense amplifiers between the top and bottom halves of the memory array. The chip size of this 16K RAM is 122 mils x 227 mils.

MOSTEK®

AN IN-DEPTH LOOK AT MOSTEK'S HIGH PERFORMANCE MK4027

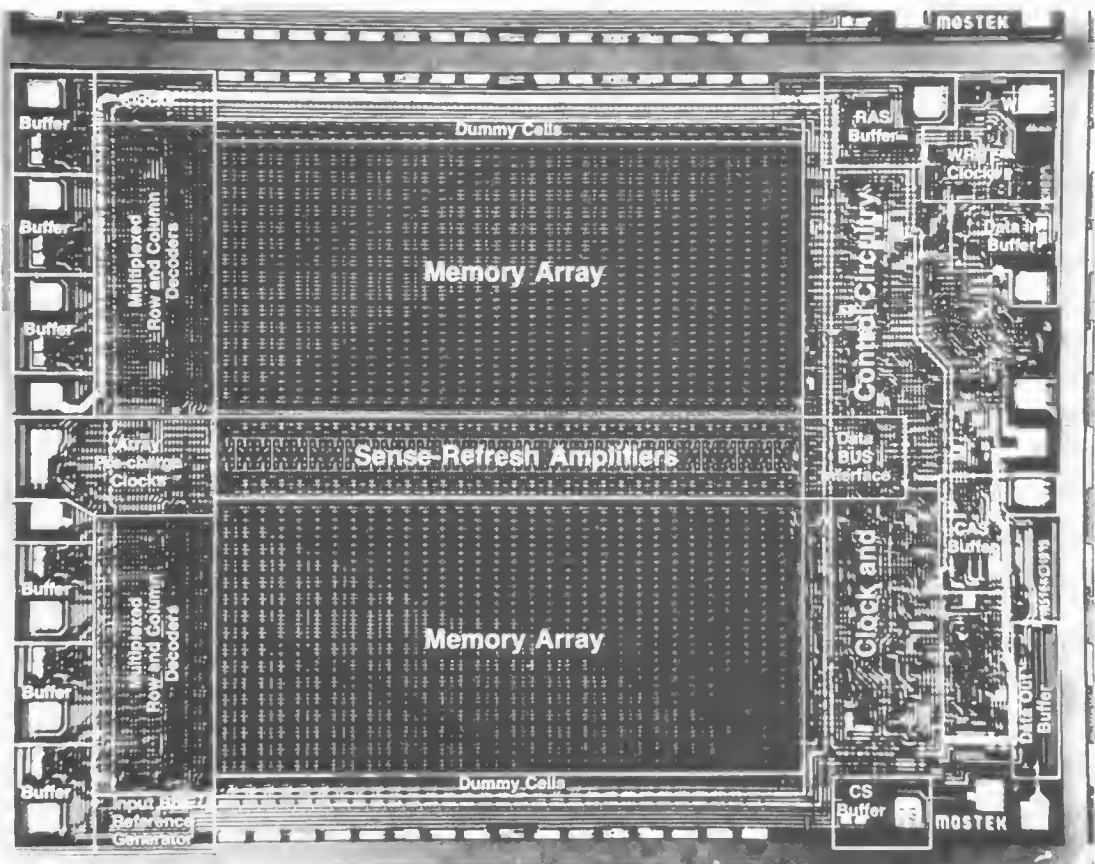
Application Note

The MK 4027, like its predecessor the MK 4096, is a 4096 word by 1 bit N-Channel MOS Random Access Memory circuit that is packaged in a standard 16-pin DIP. This small package size is the result of a unique multiplexing and latching technique for the address inputs which MOSTEK pioneered for its 4K RAM family. This innovative approach to dynamic RAM design has proven to be one of the most important semiconductor memory milestones in the past few years. With more than a dozen manufacturers having announced their intentions to produce equivalent circuits with identical pin configurations, the MOSTEK 16-pin 4K RAM family has become an industry standard.

The purpose of this application note is to acquaint the user with the MK 4027, and to provide a more complete and in-depth understanding of the circuit (and its use) than can be obtained from the data sheet alone. MOSTEK realizes that most experienced memory system designers go through a process of evaluating many potential memory devices and making a judgement as to which device is best for a particular application. MOSTEK also realizes that this evaluation process can be a very tedious and time consuming endeavor, especially if several potential candidates are to be evaluated. Therefore, the information presented in this application note is divided into major sections and presented in the order that MOSTEK has found to be most desirable in the typical evaluation process used by most designers.

DYNAMIC
RAMS

Figure 1

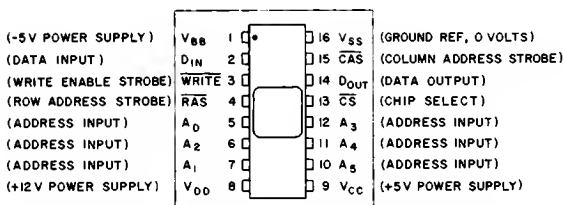


BACKGROUND

The pin configuration for the 16-pin 4K RAM was originated by MOSTEK Corporation when the MK 4096 was announced in 1973. Basically, the 16 pin device is made possible by eliminating six of the twelve address inputs required to select one out of 4096 bit locations in the RAM. Addressing is accomplished by the external generation of negative going Row and Column Address Strobe signals (RAS and CAS) which latch incoming multiplexed addresses into the chip. This same addressing technique is carried over from the MK 4096 to the higher performance MK 4027.

PIN CONNECTIONS

Figure 2



In addition to improved performance characteristics, the MK 4027 also incorporates several different and flexible operating modes and system-oriented features. These features include direct interfacing capability with TTL, low capacitance inputs and output, on-chip address and data registers, two methods of chip selection, simplified (RAS-only) refresh oper-

ation, and flexible column address timing to compensate for system timing skews. Also, the MK 4027 offers a unique cycling operation called page-mode. Page-mode timing is very useful in systems requiring Direct Memory Access (DMA) operation.

Before delving into the more detailed aspects of the MK 4027, it is helpful to obtain a basic understanding of the internal circuit operation. Once a designer understands the fundamental operation of the MK 4027, it is much easier to see how and why the device operates with such improved performance over existing 4K dynamic RAM designs.

Much of the internal structure of the MK 4027 is made possible by state-of-the-art processing. The MK 4027 is fabricated with MOSTEK's ion-implanted N-Channel silicon gate (Poly I) process, whose basic steps are illustrated in figure 3. This process allows independent adjustment of gate and field oxide thresholds by ion-implantation (a technique introduced by MOSTEK in 1971), which maximizes performance, density, and reliability.

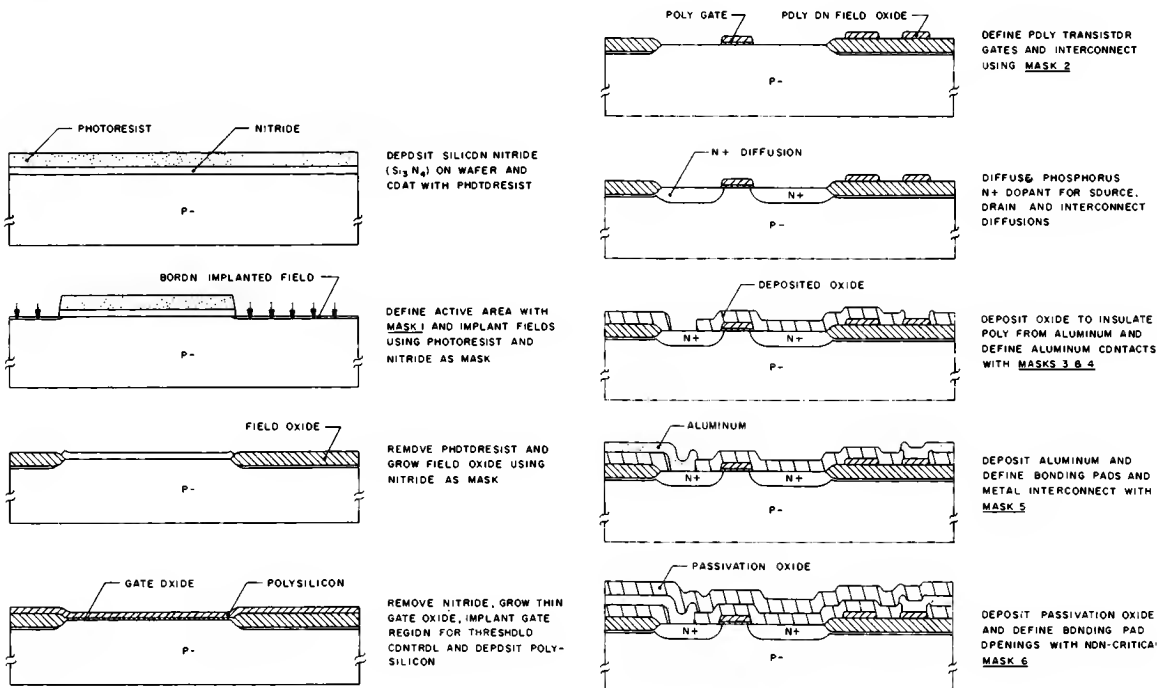
INTERNAL CIRCUIT OPERATION

The internal circuit operation of the MK 4027 is unlike any other 4K RAM in the industry. The MK 4027 utilizes a revolutionary new architecture for semiconductor memories. The circuit layout and design techniques incorporated within the MK 4027 are the main reasons for the increased performance capabilities and the additional system-oriented features. As an aid in understanding the operation of the MK 4027 refer to the block diagram in figure 4.

A major difference between the MK 4027 and most conventional RAMs is that the MK 4027 has

4027 PROCESS STEPS

Figure 3



only one internal decoder and only one set of input buffers for both the Row and Column addresses. This feature greatly reduces the active silicon area and input capacitance. Note also that the internal single transistor storage cell matrix is divided into two sections with the sense amplifiers and input/output circuitry located between the two. This type of sense amp configuration causes data stored in half of the memory to be inverted from the data stored in the opposite half. However, this inversion is completely invisible at the device terminals. The sense amplifiers incorporated within the MK 4027 are dynamic, balanced, differential sense amps which dissipate no D C or steady-state power. Furthermore, virtually all of the circuitry used in the MK 4027 is dynamic and consequently, most of the power dissipated by the MK 4027 is a function of operating frequency rather than active duty cycle.

MEMORY CYCLES

The MK 4027 will begin a memory cycle as soon as the Row Address Strobe (RAS) input is activated. This is done by changing the voltage potential at the RAS input from a high level to a low level. The first internal action that takes place is the conversion of the TTL-compatible RAS signal to the MOS (12 volt) level that is required within the chip. The internal amplifier that performs this conversion is, of necessity, powered up at all times. Therefore, the RAS input buffer always dissipates some D C power. The steady-state power dissipated by the RAS input buffer is the main component of the overall standby power.

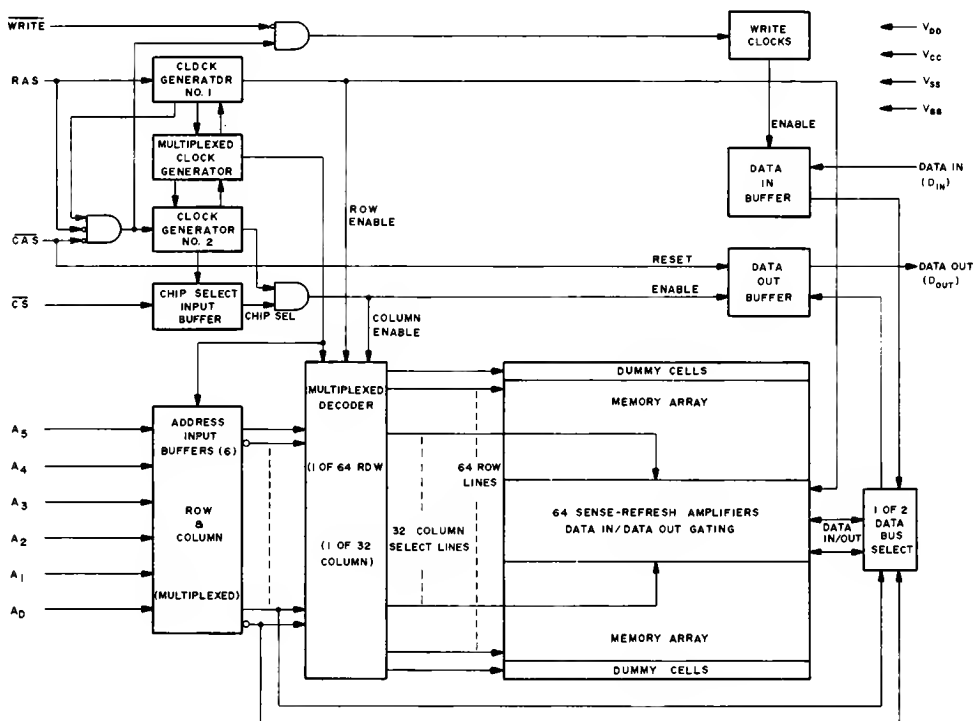
After the Row strobe reaches the proper level internally, a series of internal clock edges are generated to perform special control functions. The first of these clocks serves as a signal to "trap" the first set of six addresses into the address input buffers. These input buffers then generate the address into both true and complement form in high level, as required by the decoder. The addresses are then decoded for selection of the proper row in the memory cell matrix. Also, as the selected row is enabled, a set of dummy cells are enabled on the opposite side of the sense amplifier from the selected Row. These dummy cells serve to establish the proper trip point or reference voltage as required by the sense amps to differentiate between a one level and a zero level when the selected cell is read. As the selected Row and dummy cells are enabled, the address input buffers are already being reset and precharged so that the column addresses can be multiplexed into the chip.

The last action initiated by the row clocks causes the data in all 64 cell locations in the selected Row to be latched into the sense amplifiers which, in turn, restore proper data back into the cells. (This action is known as refreshing.) The selected Row output from the decoder remains enabled as long as the Row Address Strobe (RAS) is at a logic 0 level.

The second chain of events within the MK 4027 memory cycle, assuming that RAS is active, occurs when the Column Address Strobe (CAS) is activated. As soon as the CAS is brought to logic 0 level, the output buffer is turned off and the output assumes the high impedance (open-circuit) state. If, at this time, the input circuitry is ready to process the column data, the low level CAS signal is converted to

MK 4027 FUNCTIONAL BLOCK DIAGRAM

Figure 4



high level (12V) CAS. However, if the circuit is not yet ready to process column data, generation of the high level CAS signal is delayed. The internal mechanism for determining whether the MK 4027 is ready to process the column information is controlled by a signal from the row clock generator. This signal inhibits all column clocks until the sequence of row clocks has progressed to the appropriate time in the memory cycle. The internal "gating" of the RAS and CAS clocks has a very significant impact on external operation of the part. This is discussed in detail in a later section of this application note.

After CAS reaches the proper internal level, a series of clock edges are generated which operate in a similar manner to the RAS clocks. In the case of CAS, however, the second rather than the first clock serves to "trap" the second set of six addresses into the address input buffers. These buffers again generate true and complement high level addresses as required by the decoder. Also, at this time the WRITE circuitry is enabled and the input/output data buses, which are routed through the center of the cell matrix, and the output buffer are all precharged to proper levels.

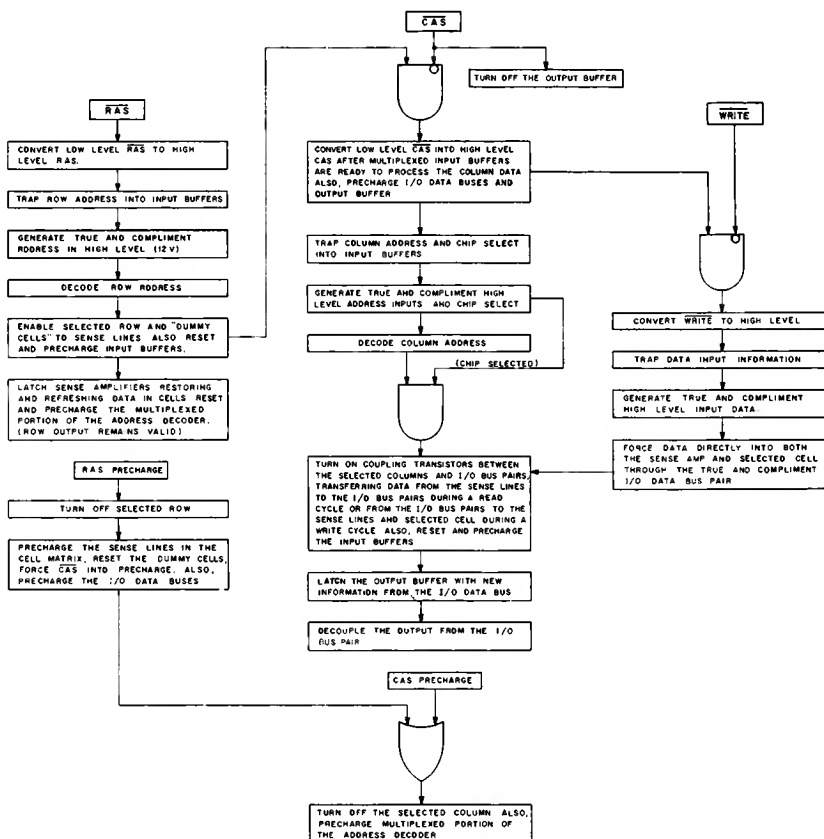
If the WRITE input is activated, a parallel series of clocks are enabled in addition to those enabled by the CAS circuitry alone. While the column addresses

are trapped into the address input buffers and converted into true and complement high-level addresses, the WRITE input is converted to a high-level clock and data is latched into the data input buffer where it is also converted to true and complement, high-level information. It should be pointed out that the CAS circuitry also enables the Chip Select (CS) input. The Chip Select input buffer is essentially the same type of circuit as an address input buffer, but, if the Chip Select input is not activated, the remaining series of CAS clocks are inhibited.

If, at this point in time, the chip has received a Row Address Strobe and a Column Address Strobe (with the Chip Select active), the chip will initiate either the Read or Write operation as indicated by the state of the WRITE input. The decoder selects the proper column by enabling the coupling transistors which connect the selected columns to the data input/output differential bus pairs. During a read cycle, data is transferred from the selected sense lines to the I/O bus pairs. A write cycle will cause data to be transferred from the selected data I/O bus to the sense lines so that proper data is forced into the selected storage cell. After the correct data is present on the I/O bus, the data output buffer is latched and the correct information is presented at the output of the chip. Once the output buffer is latched, the output is decoupled from the internal I/O bus.

FUNCTIONAL FLOW CHART

Figure 5



After the chip has performed all the functions required for a read, write or refresh operation, it remains in a quiescent state until the input control clocks (RAS and CAS) are taken to the inactive (high) state. If RAS remains active and CAS is taken to the precharge (high) condition, the previously selected column will be turned off and the multiplexed portion of the address decoder will be reset and precharged, ready for a new CAS cycle. However, the previously selected row will remain enabled and the sense amps will retain the information read from that row. (This feature of the MK 4027 makes possible "page-mode" operation.) When RAS is terminated, the selected Row is turned off, the sense lines and the data I/O buses are precharged and the dummy cells are reset. Also, the input buffers and decoders are reset and precharged, ready for a new RAS cycle. Deactivating RAS also forces CAS into the precharge condition internally, even though CAS may remain active at the input.

The internal workings of the MK 4027 can be best summarized by referring to the Functional Flow Chart in figure 5. From this brief outline of the internal operation of the device it is easy to see how the MK 4027 is capable of so many different and flexible timing modes. Besides the usual read, write, and read-modify-write cycles, the MK 4027 is also capable of "page-mode" cycles (very useful in Direct Memory Access operation) and "delayed-write" cycles (very useful in shift register applications.) While keeping in mind the internal structure of the MK 4027 it is now appropriate to delve into a more detailed discussion of the external characteristics and system implications of the MK 4027 memory device.

EXTERNAL DEVICE CHARACTERISTICS

ADDRESSING

As stated earlier, the 12 address bits required to decode one of the 4096 cell locations within the MK 4027 are multiplexed onto the 6 address inputs and latched into the on-chip address latches by externally applying two negative-going, TTL-level clocks. The first clock, the Row Address Strobe (RAS), latches the 6 row address bits into the chip. The second clock, the Column Address Strobe (CAS), subsequently latches the 6 column address bits plus Chip Select (CS) into the chip. Each of these clock signals, RAS and CAS, triggers off a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the CAS clock sequence are inhibited until the occurrence of a delayed signal derived from the RAS clock chain. This "gated CAS" feature allows the CAS clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the 6 address inputs have been changed from Row address to Column address information. This results in a system limit of $t_{RCD} = t_{RAH} + t_T + t_{ASC}$ (t_T = one transition time).

Note that CAS can be activated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing end points result from the internal gating of CAS which are called t_{RCD} (min) and t_{RCD} (max). No

data storage or reading errors will result if CAS is applied to MK 4027 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time for CAS (t_{CAC}) rather than from RAS (t_{RAC}), and access time from RAS will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

The significance of this "gated CAS" feature is that it allows a multiplexed circuit, such as the MK 4027, to be comparable in performance (access time) with non-multiplexed devices such as the 18- and 22-pin 4K RAMs. In essence, it allows the designer to compensate for system timing skews that may be encountered in the multiplexing operation when addressing the device. In the MK 4027, the "window" available for multiplexing from row address to column address information while still achieving minimum access time (t_{RAC}) is a full 25% of access time.

MEMORY CYCLES

Once the MK 4027 is properly addressed, the device is capable of performing various types of memory cycles. Selection of the various cycles, whether read, write or some combination thereof, is controlled by a combination of CAS and WRITE, while RAS is active. Also, since Chip Select (CS) does not have to be valid until CAS, which is well into the memory cycle, it is possible to start a cycle before it is known which is the selected device.

Data is retrieved from the memory in a read-only cycle by maintaining WRITE in the inactive or high state throughout the portion of the memory cycle in which CAS is active. Data read from the selected cell will be available at the output within the specified access time.

Data to be written into a selected cell is latched into an on-chip register by a combination of WRITE and CAS while RAS is active. The later of these signals (WRITE or CAS) to make its negative transition is the strobe for the Data-In register. This permits several options in the write cycle timing. In a write cycle, if the WRITE input is brought low prior to CAS, the Data In is strobed in by CAS, and the set-up and hold times are referenced to CAS. If the data input is not available at CAS time or if it is desired that the cycle be a read-write cycle, the WRITE signal will be delayed until after CAS goes low. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of WRITE rather than to CAS. Note that delaying WRITE until after the negative edge of CAS is termed a "read-write cycle" rather than read-modify-write. In a read-write cycle, it is not necessary to wait until data is valid at the output before the write operation is started. This feature is very useful when the MK 4027 is used in sequential memory applications or in systems that employ "interleaving techniques." However, if a true read-modify-write cycle is required (where the write operation occurs after read access), then WRITE can occur while RAS and CAS are still active and after t_{CAC} .

To take full advantage of this CAS/WRITE signal relationship it is necessary for one to understand how the Data Out Latch is controlled. The most important fact to remember is that any change in the condition of the Data Out Latch is initiated by the CAS negative edge. The output buffer is not affected by memory cycles in which only the RAS signal is applied to the MK 4027. Whenever CAS makes a negative transition, the output will go unconditionally open-

circuited, independent of the state of any other input to the chip. If the cycle in progress is a read, read-modify-write, or a delayed write cycle and the chip is selected, then the output latch and buffer will again go active, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle in progress is a write cycle (WRITE active low before CAS goes low) and the chip is selected, then at access time the output latch and buffer will contain the input data. Once having gone active, the output will remain valid until the MK 4027 receives the next CAS negative edge. Intervening refresh cycles in which RAS is received, but no CAS, will not cause valid data to be affected. Conversely, the output will assume the open-circuited state during any cycle in which the MK 4027 receives a CAS but no RAS signal (regardless of the state of any other inputs). The output will also assume the open-circuit state in normal cycles if the chip is unselected. Note that if the chip is unselected (CS high at CAS time) WRITE commands are not executed and, consequently, data stored in the memory is unaffected.

The three-state data output buffer presents the data output pin with a low impedance to VCC for a logic 1 and a low impedance to VSS (Ground) for a logic 0. The effective resistance to VCC (logic "1" state) is 420Ω maximum and < 100 Ω typically. The resistance to VSS (logic "0" state) is 125Ω maximum and < 50Ω typically. The separate VCC pin allows the output buffer to be powered from the positive supply voltage of the logic to which the chip is interfaced. During battery standby operation, the VCC pin may have power removed without affecting the MK 4027 refresh operation. This allows all system logic except the RAS timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

Specified on the MK 4027 data sheet are two electrical characteristics of the device which guarantee the appropriate state of the data output during a write cycle. These two specifications, RAS to WRITE delay (tRWD) and CAS to WRITE delay (tCWD) are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. The values listed in the "minimum" and "maximum"

THESE PARAMETERS APPLY TO ALL MK 4027 MEMORY CYCLES:

SYMBOL	DEFINITION
tRFSH	Maximum time that the device will retain stored data without being refreshed.
tRP	$\overline{\text{RAS}}$ precharge, or $\overline{\text{RAS}}$ inactive time of a cycle.
tRCD	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ lead time. Operation within the tRCD (max) limit insures that tRAC (max) can be met. tRCD (max) is specified as a reference point only; if tRCD is greater than the specified tRCD (max) limit, then access time is controlled exclusively by tCAC.
tASR	Row address set-up time.
tRAH	Row address hold time.
tASC	Column address set-up time.
tCAH	Column address hold time.
tCSH	Column address strobe hold time
tAR	Column address hold time referenced to $\overline{\text{RAS}}$.
tCSC	Chip select set-up time.
tCH	Chip select hold time.
tCHR	Chip select hold time referenced to $\overline{\text{RAS}}$.
tCRP	$\overline{\text{CAS}}$ inactive to $\overline{\text{RAS}}$ active precharge time.
tOFF	Output buffer turn-off delay.
tRAS	$\overline{\text{RAS}}$ pulse width or active time.
tCAS	$\overline{\text{CAS}}$ pulse width or active time.
tRAC	Access time from $\overline{\text{RAS}}$ falling edge.
tCAC	Access time from $\overline{\text{CAS}}$ falling edge.
tT	Transition time (rise and fall). Transition times are measured between VIHc or VIH and VIL : VIHc (min) or VIH (min) and VIL (max) are reference levels for measuring timing of input signals.

columns should be inserted as terms in the following equations:

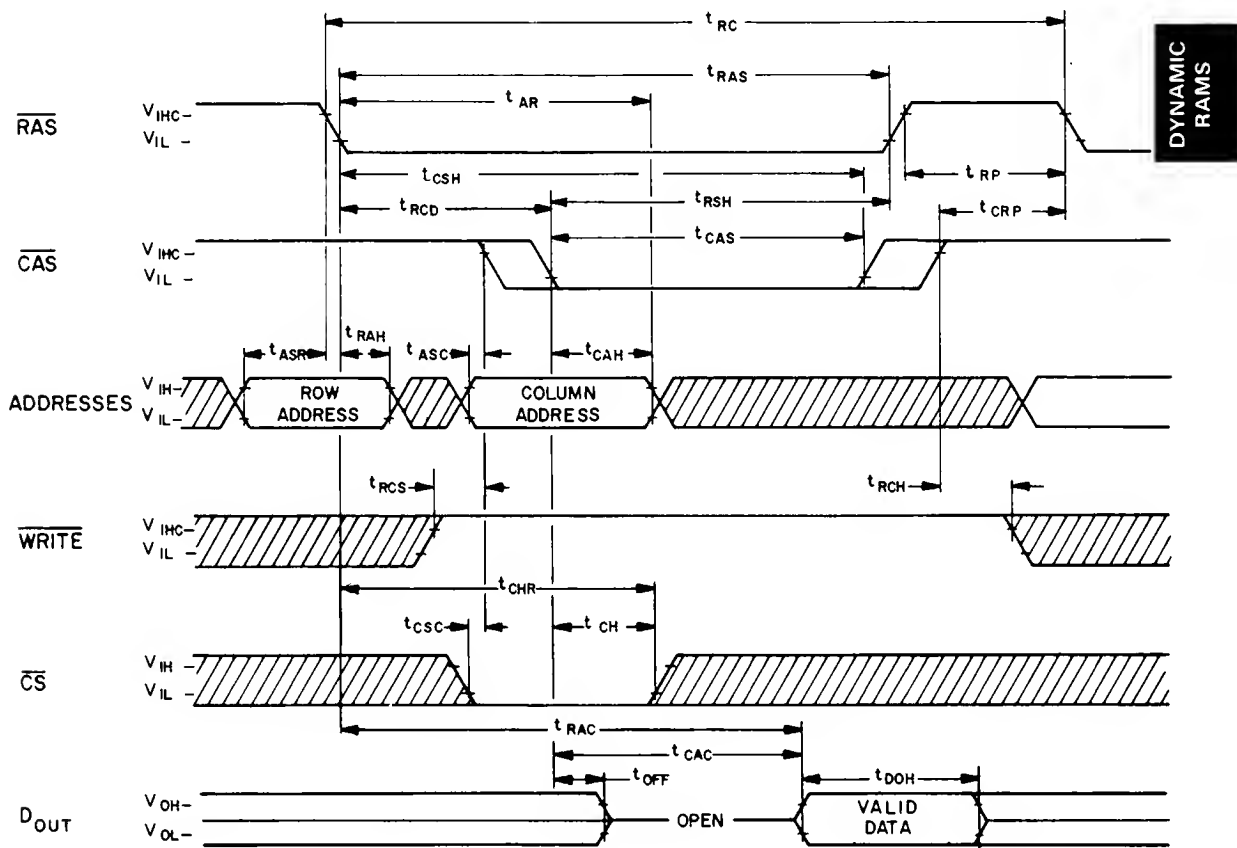
1. If $t_{CWD} + t_T \leq t_{CWD}(\min)$, the data out latch will contain the data written into the selected cell.
2. If $t_{CWD} \geq t_{CWD}(\max) + t_T$ and $t_{RWD} \geq t_{RWD}(\max) + t_T$, the data out latch will contain the data read from the selected cell.

3. If t_{CWD} does not meet the above constraints then the data out latch will contain indeterminate data at access time.

The following diagrams are representations of the MK 4027 timing waveforms for read, write and delayed-write or read-modify-write cycles. A list of the timing parameters associated with each cycle is also included.

READ CYCLE

Figure 6

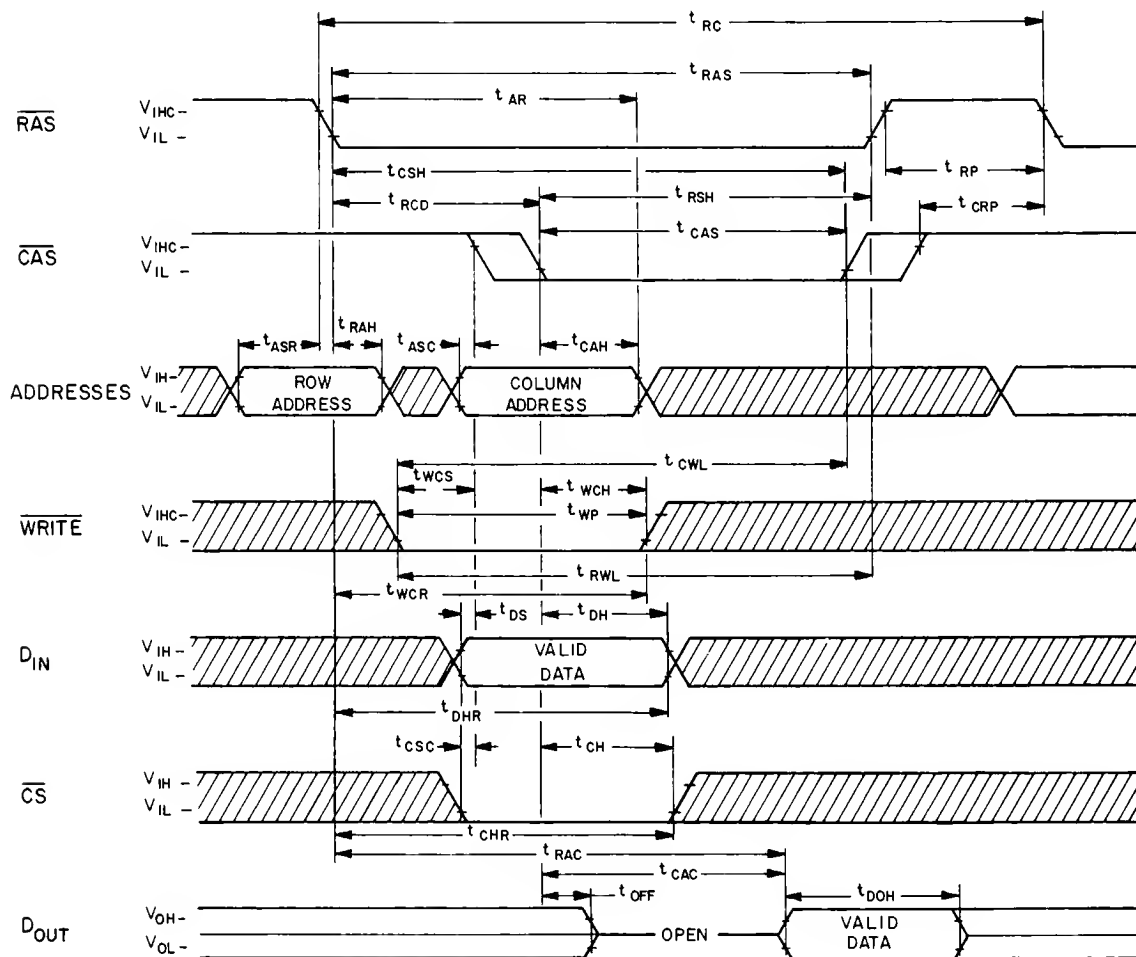


READ CYCLE ONLY

t_{RC}	Random read or write cycle time. $t_{RC}(\min) \geq t_T + t_{RAS} + t_T + t_{RP}$.
t_{RCS}	Read command set-up time.
t_{RCH}	Read command hold time.
t_{ACC}^*	Device access time, t_{ACC} , is the longer of two calculated intervals: 1. $t_{ACC} = t_{RAC}$, or 2. $t_{ACC} = t_{RCD} + t_T + t_{CAC}$ * This parameter is not shown in the timing waveforms.

WRITE CYCLE

Figure 7

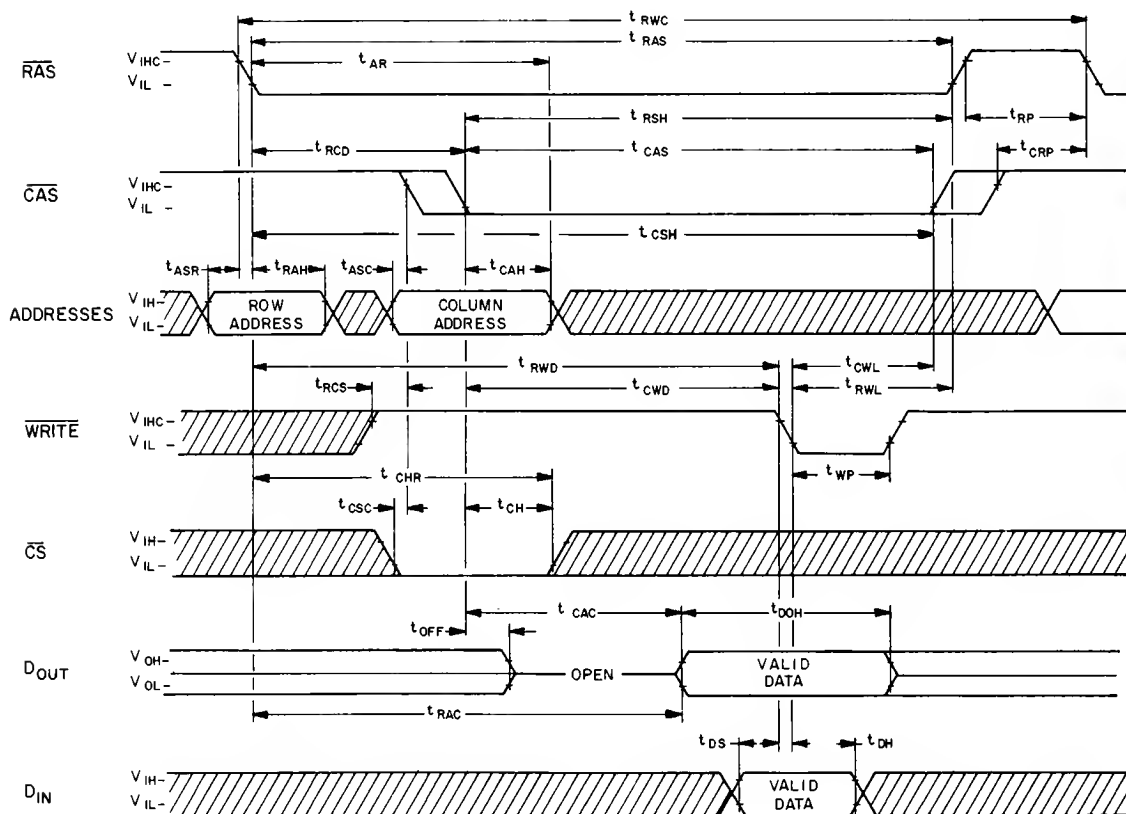


WRITE CYCLE ONLY

t_{RC}	Random read or write cycle time. $t_{\text{RC}} (\text{min}) \geq t_{\text{T}} + t_{\text{RAS}} + t_{\text{T}} + t_{\text{RP}}$.
t_{WCH}	Write command hold time referenced to $\overline{\text{CAS}}$.
t_{WCR}	Write command hold time referenced to $\overline{\text{RAS}}$.
t_{WP}	Write command pulse width.
t_{RWL}	Write command to $\overline{\text{RAS}}$ lead time.
t_{CWL}	Write command to $\overline{\text{CAS}}$ lead time.
t_{DS}	Data In set-up time (referenced to $\overline{\text{CAS}}$).
t_{DH}	Data In hold time (referenced to $\overline{\text{CAS}}$).
t_{DHR}	Data In hold time (referenced to $\overline{\text{RAS}}$).

READ - WRITE / READ - MODIFY - WRITE CYCLE

Figure 8



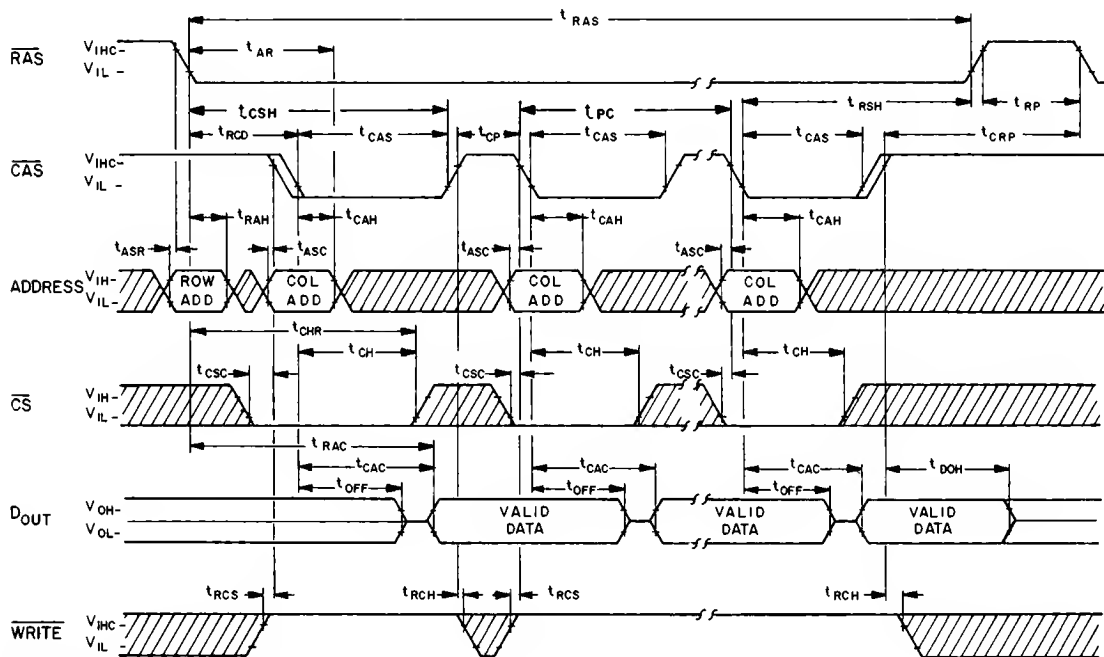
DYNAMIC
RAMS

READ/WRITE CYCLE

t_{RWC}	Read-write or "delayed write" cycle time. $t_{RWC} (\text{min}) \geq t_T + t_{RCD} + t_T + t_{CWD} + t_{RWL} + t_T + t_{RP}$. This is the minimum time to insure that both a read and write operation will occur at the same address in a single memory cycle.
t_{RCS}	Read command set-up time.
t_{WP}	Write command pulse width.
t_{RWD}	\overline{RAS} to \overline{WRITE} delay.
t_{CWD}	\overline{CAS} to \overline{WRITE} delay.
t_{RWL}	Write command to \overline{RAS} lead time.
t_{CWL}	Write command to \overline{CAS} lead time.
t_{DS}	Data In set-up time (referenced to \overline{WRITE}).
t_{DH}	Data In hold time (referenced to \overline{WRITE}).

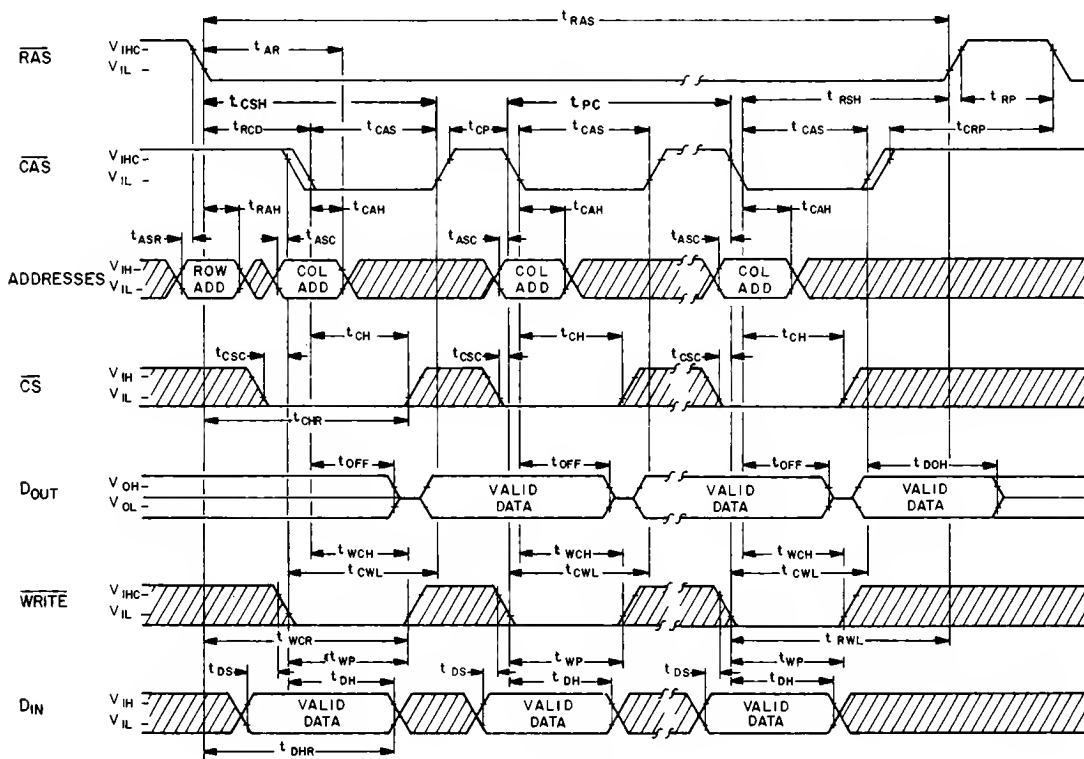
PAGE MODE READ CYCLE

Figure 9



PAGE MODE WRITE CYCLE

Figure 10



PAGE MODE

Keeping in mind the above mentioned cycle operations, it is now appropriate to introduce another category of memory cycles. The "page-mode" operation allows for successive memory operations at multiple column locations at the same row address with increased speed and with decreased power. This is done by strobing the row address into the chip and keeping the RAS signal active (at a logic 0) throughout all successive memory cycles in which the row address is common. This "page-mode" operation will not dissipate the power associated with the negative going edge of RAS. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times. Every type of cycle-read, write, read-modify-write and delayed-write cycles—can all be performed in the page mode. Also, the chip select (CS) is operative in page mode just as in normal cycles. It is not necessary that the chip be selected during the first cycle for subsequent cycles to be selected properly in a page operation. Likewise, the CS input can be used to select or disable any cycle (s) in a series of "page" cycles. This feature allows the page boundary to be extended beyond the 64 column locations in a single chip. The page boundary can be extended by applying RAS to multiple 4K memory blocks and decoding CS to select the proper block.

The addition of page mode to the MK 4027's repertoire of features adds only two additional constraints to the timing parameters mentioned earlier. The first constraint is that the length of time that a single chip can remain in the page mode is limited to the maximum RAS pulse width (t_{RAS}) as specified on the data sheet. Second, the CAS precharge time (t_{CP}), or the time from the positive edge of CAS in one page cycle to the negative edge of CAS in subsequent page cycles must be obeyed.

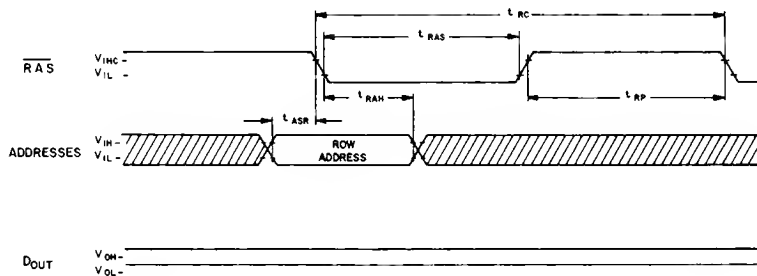
The following timing waveforms illustrate the page mode operation. Note that the page-mode write cycle depicts the Data In set-up and hold times referenced to WRITE rather than CAS. Once again, this is to illustrate the flexibility of the write cycle operation. Page-mode operation is particularly useful in transferring large blocks of data into or out of memory.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses within each 2 millisecond time interval.

"RAS ONLY" REFRESH CYCLE

Figure 11



Any cycle in which a \overline{RAS} signal occurs, accomplishes a refresh operation. A read cycle will refresh the selected row, regardless of the state of the Chip Select (CS) input. A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the selected cell. If during a refresh cycle, the MK 4027 receives a \overline{RAS} signal but no \overline{CAS} signal, the state of the output will not be affected. Therefore, data from the previous cycle will remain valid throughout the refresh cycle. However, if "RAS-only" refresh cycles (where RAS is the only signal applied to the chip) are continued for extended periods, the output buffer may eventually lose proper data and go open-circuit. The output buffer will regain activity with the first cycle in which CAS is applied to the chip.

The following diagram illustrates the "RAS-only" refresh cycle:

POWER DISSIPATION

The worst case power dissipation of the MK 4027, continuously operating at the fastest cycle rate, is the sum of $[V_{DD}(\text{max}) \times I_{DD}(\text{max}) \text{ plus } V_{BB}(\text{max}) \times I_{BB}(\text{max})]$, where maximum currents are the maximum currents averaged over one memory cycle. The worst case power for the MK 4027 with a cycle rate of 375 nanoseconds is less than 470mW, while the typical power is 170 mW at a $1 \mu\text{s}$ cycle time.

Typical power supply current waveforms for various types of memory cycles are shown in figure 12. From this picture it is easy to see that most of the power drawn by the MK 4027 is the result of an address strobe charging the capacitances of various internal circuit nodes.

Note also that there is very small DC component in the current waveforms, independent of how long the address strobes remain active. This is because most of the circuitry in the MK 4027 is dynamic, with the exception of the RAS input buffer.

The first portion of the current waveforms illustrates a normal RAS/CAS memory cycle. As expected, the I_{DD} waveform has three major current peaks above ground level. These occur when RAS goes active, then when CAS internally goes active, and finally when both RAS and CAS go back into precharge. On the other hand, both positive and negative current transients are associated with I_{BB} . This results in peak currents that can be two to four orders of magnitude higher than the average DC value.

The second cycle is representative of a page-mode cycle in which CAS is completely enveloped by RAS.

Note that delaying $\overline{\text{CAS}}$ until well after $\overline{\text{RAS}}$ goes negative demonstrates the relative contributions of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ to total power. This type of cycle operation has the effect of reducing the peak current associated with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ going into precharge simultaneously. Instead, two smaller current spikes are generated, each coinciding with the separate termination of $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$. From the current waveform it is clear that approximately 60% of all active power is due to $\overline{\text{RAS}}$ and only about 40% of all active power is due to $\overline{\text{CAS}}$. Thus, even with increased frequency, the maximum power dissipated in a page-mode operation is less than that in a normal cycle.

The third cycle is a " $\overline{\text{RAS}}$ -only" cycle which can be used for the refresh operation. Note that the MK 4027 will dissipate considerably less power when the refresh operation is accomplished with a " $\overline{\text{RAS}}$ -only" cycle as opposed to a normal $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycle.

TESTING THE MK 4027 MEMORY DEVICE

Production testing of each MK 4027 memory device begins early in the process of every MK 4027 wafer. Once a wafer is processed, each individual die on that wafer is subjected to probe testing. This is where each die is probed and tested for functionality, leakage and continuity. All die that pass this test are then packaged and subjected to further Quality Assurance Processing.

The next barrage of tests include the following:

100% Pre-burn testing at high temperature (for function, leakage, and continuity)

100% Temperature Cycling-screened to 10 cycles, -65°C to $+150^{\circ}\text{C}$

100% Centrifuge - screened to insure positive die and bond attachment

100% Dynamic Burn-In - each device is operated at conditions well beyond data sheet limits for many hours to insure that only quality devices reach the end user.

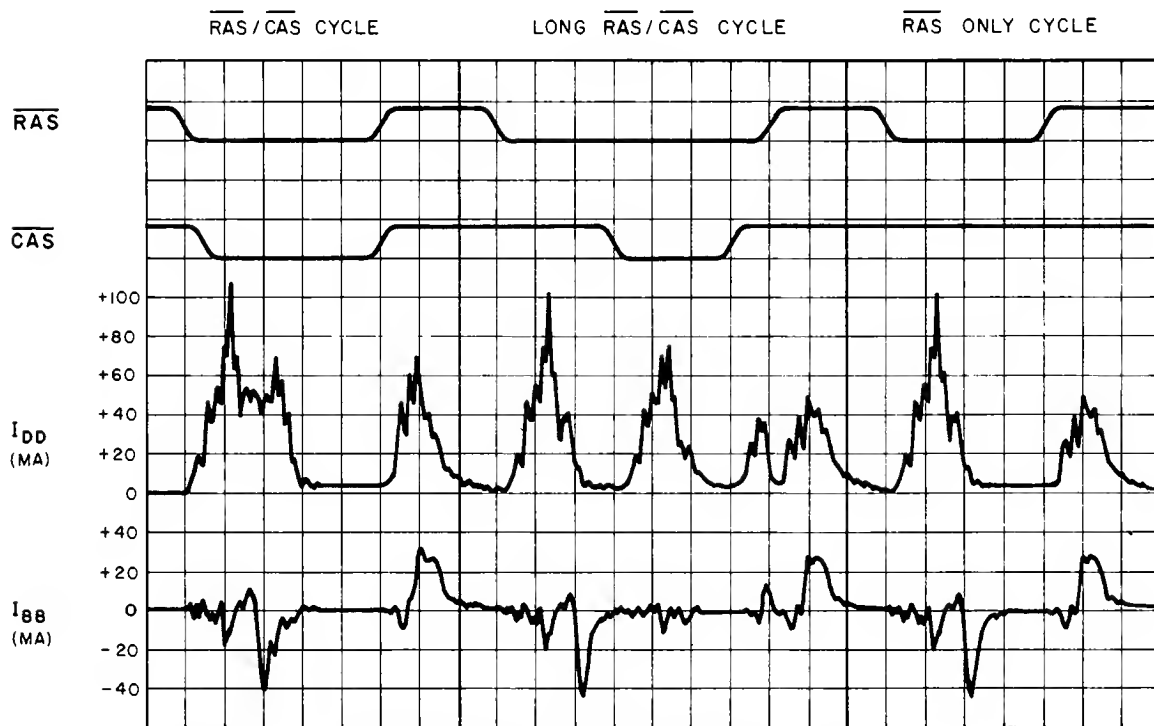
All MK 4027 devices that pass the previous tests are then final tested for customer use. At final test, all devices are tested at high temperature, to all data sheet AC and DC specifications with wide guardbands. This type of Quality Assurance Processing and Testing insures that not only does every MK 4027 perform well within the established data sheet limits, but also exhibits the quality and reliability standards necessary for today's (and tomorrow's) data processing applications.

Thorough testing of every MK 4027 is performed on what MOSTEK calls "MASTER TESTERS." These machines incorporate a very versatile pattern generator made by Computest and a very sophisticated parametric measurement unit (PMU) and clock section that was conceived and constructed by MOSTEK Test Equipment design engineers. This combination of purchased and custom designed hardware is controlled by a PDP-11 minicomputer. These MASTER

TESTERS are used not only in production testing but also in the engineering characterization of the MK 4027. This permits excellent correlation between characterization and production testing on the device. The test equipment is also used as an analysis tool in

RAS / CAS CYCLE - LONG RAS / CAS CYCLE - RAS ONLY CYCLE

Figure 12





MOSTEK's 4K testing area.

the "continuing engineering" phase of MK 4027 production.

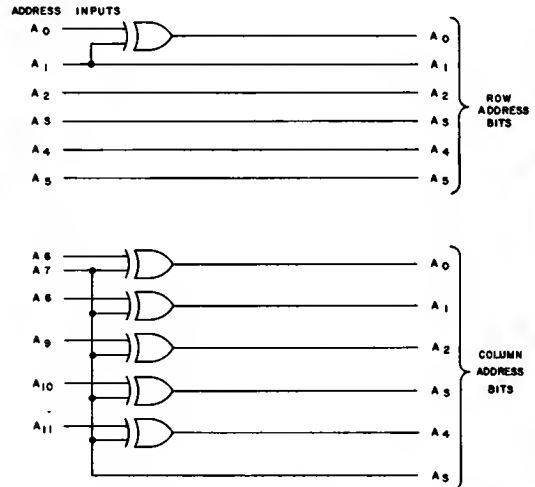
Establishing one's own incoming inspection and testing procedures for a device as complicated as a 4K dynamic RAM is one of the most important and critical procedures in any production program. Usually the effectiveness of the screening procedure may not be known until several assembled systems have been field tested for several months. Therefore, it is important that proper screening procedures are employed early in any production program.

Many times, in establishing electrical end-point tests, it is necessary to know the proper external addressing sequence to insure sequential addressing within a memory device. The internal address bit map of the MK 4027 is arranged in a somewhat unusual fashion to keep the chip size to a minimum. Therefore, sequentially addressing the MK 4027 cannot be done with a straight binary count without the

circuitry shown below. Note that this is for testing purposes only and is certainly not required or recommended for system use.

MK 4027 ADDRESS INTERPOLATION

Figure 13



Also, since the sense amplifiers within the MK4027 are located in the center of the memory matrix, data stored in half of the memory will be inverted from the data presented at the input pin. Once again, this inversion is completely transparent to the user (i.e., data stored in the memory as a "1" or "0" at the input will, when subsequently accessed, appear as a "1" or "0" respectively at the output). However, if one wishes to determine the polarity of data stored in the memory, refer to the following chart.

ROW ADDRESS A ₅	DATA STORED
0	inverted data
1	true data

INTRODUCTION

Memory Systems design is very much like any other interface design. It requires knowledge of the system being interfaced to and also an in-depth knowledge of the resource being interfaced. This in-depth knowledge must include the functional and electrical characteristics of the device as well as power requirement, noise sensitivities and driver requirements. This application note will attempt to cover all of the areas that are relevant to designing a memory system using the MK4027 or the MK4116. The discussion centers around a memory board that was designed for the LSI-11* microcomputer. Many of the techniques and methods used in this design can be applied to almost any other memory system design.

THE LSI-11* BUS

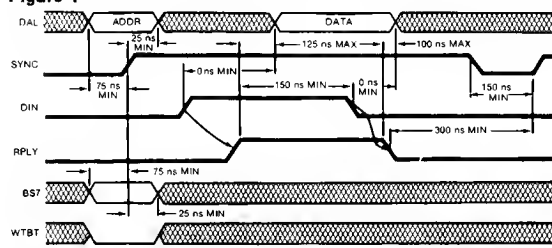
The LSI-11* microcomputer bus is used for all data transfers within the system. It has four types of cycles that are of significance to the memory system: read, write, read-modify-write and refresh. The timing for each of these cycles as seen from the interface side of the bus receivers is given in Figs. 1, 2, and 3. Since the memory can never institute a bus cycle it is always a slave device. As can be seen from the timing diagrams, all cycles are interlocked asynchronous. The bus cycles have three phases; device selection, transfer initiation and transfer termination. Device selection (either memory or peripheral) is accomplished by the bus master placing the device address on the multiplexed address-data lines. After allowing time for bus delays, driver-receiver skews and address decode the bus master sends SYNC to signal that a transfer will take place between the bus master and the addressed device. The type of cycle is identified by the state of the WTBT and the REF lines. Transfer initiation occurs when the bus master asserts DIN or DOUT. DIN and DOUT are used to control the direction of data flow. DIN causes the flow to be from slave to master (read cycle) and DOUT from master to slave (write cycle). Transfer termination is caused by the addressed device (slave) asserting RPLY. This indicates to the master that the read data is available on the address/data lines or that the write data has been received by the slave. In response to RPLY the bus master drops DIN or DOUT and the slave in turn drops RPLY. For a read-modify-write cycle the DIN-RPLY sequence is followed by

a DOUT-RPLY sequence. This allows read-modify-write to be done with only one address assertion. The LSI-11* also has a protocol to allow for refresh of dynamic RAMs. Refresh is normally done under control of the LSI-11* microcode. A refresh cycle consists of a DIN-RPLY sequence with RFSH active. During a refresh cycle no data is transferred and only A1-A6 have any significance. These addresses are used to indicate which row of a dynamic RAM is to be refreshed. Sixty-four refresh cycles are generated in a burst every 1.6ms.

DYNAMIC
RAMS

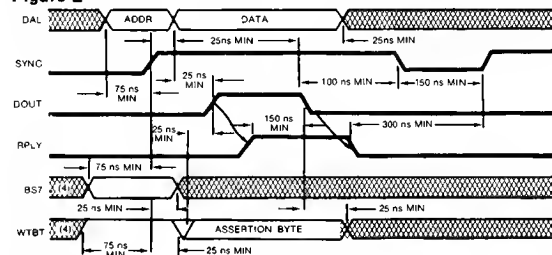
READ (REFRESH) CYCLE TIMING

Figure 1



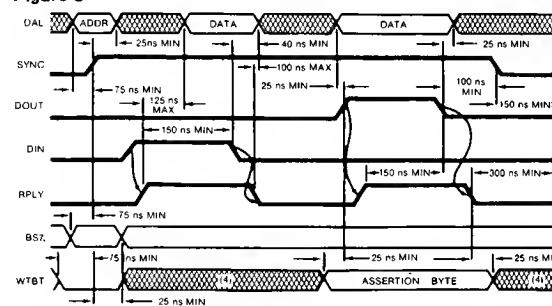
WRITE CYCLE TIMING

Figure 2



READ MODIFY WRITE CYCLE TIMING

Figure 3



*LSI 11 is a trademark of Digital Equipment Corporation

There are several points about the bus timing that should be mentioned in passing as they will influence some of the decisions made later. Since the transfers on the bus are asynchronous the memory does not have to respond in a fixed period of time. This is unlike many other microprocessors that favor synchronous transfers. Another point that should be made is that the cycle time requirements for the memory are not very stringent. In fact, the absolute minimum cycle time with a 0ns access memory is over 800 ns. This leaves quite a bit of 'dead' time in the cycle as far as the memory is concerned.

The final point is that logically there is no difference between transfers between the CPU and memory, or CPU and peripheral. Usually, the upper 4K words of the 32K word address space is reserved for peripheral addresses. When an address within the range is placed on the bus, BS7 is asserted to flag the address as being within the 4K I/O page. There is, however, no reason why the memory cannot be made to respond to some of the addresses in the I/O page as long as it does not conflict with peripheral addresses.

MK4027 FUNCTIONAL DESCRIPTION

Addressing

The 12 address bits required to decode 1 of the 4096 cell locations within the MK 4027 are multiplexed onto the 6 address inputs and latched into the on-chip address latches by externally applying two negative going TTL level clocks. The first clock, the Row Address Strobe (\overline{RAS}), latches the 6 row address bits into the chip. The second clock, the Column Address Strobe (\overline{CAS}), subsequently latches the 6 column address bits plus Chip Select (\overline{CS}) into the chip. The internal circuitry of the MK 4027 is designed to allow the column information to be externally applied to the chip before it is actually required. Because of this, the hold time requirements for the input signals associated with the Column Address Strobe are also referenced to \overline{RAS} . However, this gated \overline{CAS} feature allows the system designer to compensate for timing skews that may be encountered in the multiplexing operation. Since the Chip Select signal is not required until \overline{CAS} time, which is well into the memory cycle, its decoding time does not add to system access or cycle time.

Data Input/Output

Data to be written into a selected cell is latched into an on-chip register by a combination of \overline{WRITE} and \overline{CAS} while \overline{RAS} is active. The later of the signals (\overline{WRITE} or \overline{CAS}) to make its negative transition is the strobe for the Data In register. This permits several options in the write cycle timing. In a write cycle, if the \overline{WRITE} input is brought low prior to \overline{CAS} , the Data In is strobed by \overline{CAS} , and the set-up

and hold times are referenced to \overline{CAS} . If the data input is not available at \overline{CAS} time or if it is desired that the cycle be a read-write cycle, the \overline{WRITE} signal must be delayed until after \overline{CAS} . In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of \overline{WRITE} rather than to \overline{CAS} . Note that if the chip is unselected (\overline{CS} high at \overline{CAS} time) \overline{WRITE} commands are not executed and, consequently, data stored in the memory is unaffected.

Data is retrieved from the memory in a read cycle by maintaining \overline{WRITE} in the inactive or high state throughout the portion of the memory cycle in which \overline{CAS} is active. Data read from the selected cell will be available at the output within the specified access time.

Data Output Latch

Any change in the condition of the Data Out Latch is initiated by the \overline{CAS} signal. The output buffer is not affected by memory (refresh) cycles in which only the \overline{RAS} signal is applied to the MK 4027. Whenever \overline{CAS} makes a negative transition, the output will go unconditionally open-circuited, independent of the state of any other input to the chip. If the cycle in progress is a read, read-modify-write, or a delayed write cycle and the chip is selected, then the output latch and buffer will again go active and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle in progress is a write cycle (\overline{WRITE} active low before \overline{CAS} goes low) and the chip is selected, then at access time the output latch and buffer will contain the input data. Once having gone active, the output will remain valid until the MK 4027 receives the next \overline{CAS} negative edge. Intervening refresh cycles in which a \overline{RAS} is received (but no \overline{CAS}) will not cause valid data to be affected. Conversely, the output will assume the open-circuit state during any cycle in which the MK 4027 receives a \overline{CAS} but no \overline{RAS} signal (regardless of the state of any other inputs). The output will also assume the open circuit state in normal cycles (in which both \overline{RAS} and \overline{CAS} signals occur) if the chip is unselected.

The three-state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The output resistance to V_{CC} (logic 1 state) is 420 Ω maximum and 135 Ω typically. The output resistance to V_{SS} (logic 0 state) is 125 Ω maximum and 35 Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4027 refresh operation. This allows all system logic except the \overline{RAS} timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

Refresh

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses within each 2 millisecond time interval. Any cycle in which a $\overline{\text{RAS}}$ signal occurs, accomplishes a refresh operation. A read cycle will refresh the selected row, regardless of the state of the Chip Select ($\overline{\text{CS}}$) input. A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the selected cell. If, during a refresh cycle, the MK 4027 receives a $\overline{\text{RAS}}$ signal but no $\overline{\text{CAS}}$ signal, the state of the output will not be affected. However, if "RAS-only" refresh cycles (where $\overline{\text{RAS}}$ is the only signal applied to the chip) are continued for extended periods, the output buffer may eventually lose proper data and go open circuit. The output buffer will regain activity with the first cycle in which a $\overline{\text{CAS}}$ signal is applied to the chip.

Power Dissipation/Standby Mode

Most of the circuitry in the MK 4027 is dynamic and most of the power drawn is the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency rather than active duty cycle. Typically, the power is 170mW at 1 μ sec cycle rate for the MK 4027 with a worse case power of less than 470mW at 320 nsec cycle time. To minimize the overall system power, the Row Address Strobe ($\overline{\text{RAS}}$) should be decoded and supplied to only the selected chips. The $\overline{\text{CAS}}$ must be supplied to all chips (to turn off the unselected output). Those chips that did not receive a $\overline{\text{RAS}}$, however, will not dissipate any power on the $\overline{\text{CAS}}$ edges, except for that required to turn off the outputs. If the $\overline{\text{RAS}}$ signal is decoded and supplied only to the selected chips, then the Chip Select ($\overline{\text{CS}}$) input of all chips can be at a logic 0.

The chips that receive a $\overline{\text{CAS}}$ but no $\overline{\text{RAS}}$ will be unselected (output open-circuited) regardless of the Chip Select input. For refresh cycles, however, either the $\overline{\text{CS}}$ input of all chips must be high or the $\overline{\text{CAS}}$ input must be held high to prevent several "wire-OR'd" outputs from turning on with opposing force. Note that the MK 4027 will dissipate considerably less power when the refresh operation is accomplished with a "RAS-only" cycle as opposed to a normal $\overline{\text{RAS}}/\overline{\text{CAS}}$ memory cycle.

Page Mode Operation

The "Page Mode" feature of the MK 4027 allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by

strobing the row address into the chip and keeping the $\overline{\text{RAS}}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common.

This "page mode" of operation will not dissipate the power associated with the negative going edge of $\overline{\text{RAS}}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times. The chip select input ($\overline{\text{CS}}$) is operative in page mode cycles just as in normal cycles. It is not necessary that the chip be selected during the first operation in a sequence of page cycles.

Likewise, the $\overline{\text{CS}}$ input can be used to select or disable any cycle(s) in a series of page cycles. This feature allows the page boundary to be extended beyond the 64 column locations in a single chip. The page boundary can be extended by applying $\overline{\text{RAS}}$ to multiple 4K memory blocks and decoding $\overline{\text{CS}}$ to select the proper block.

MK4116 FUNCTIONAL DESCRIPTION

Addressing

The 14 address bits required to decode 1 of the 16,384 cell locations within the MK 4116 are multiplexed onto the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, the Row Address Strobe ($\overline{\text{RAS}}$), latches the 7 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{\text{CAS}}$), subsequently latches the 7 column address bits into the chip. Each of these signals, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{\text{CAS}}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{\text{RAS}}$ clock chain. This "gated $\overline{\text{CAS}}$ " feature allows the $\overline{\text{CAS}}$ clock to be externally activated as soon as the Row Address Hold Time specification (tRAH) has been satisfied and the address inputs have been changed from Row address to Column address information.

Note that $\overline{\text{CAS}}$ can be activated at any time after tRAH and it will have no effect on the worst case data access time (tRAC) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of $\overline{\text{CAS}}$ which are called $\text{tRCD}(\text{min})$ and $\text{tRCD}(\text{max})$. No data storage or reading errors will result if $\overline{\text{CAS}}$ is applied to the MK 4116 at a point in time beyond the $\text{tRCD}(\text{max})$ limit. However, access time will then be determined exclusively by the access time from $\overline{\text{CAS}}$ (tCAC) rather than from $\overline{\text{RAS}}$ (tRAC), and access time from $\overline{\text{RAS}}$ will be lengthened by the amount that tRCD exceeds the $\text{tRCD}(\text{max})$ limit.

Data Input/Output

Data to be written into a selected cell is latched into an on-chip register by a combination of WRITE and CAS while RAS is active. The later of the signals (WRITE or CAS) to make its negative transition is the strobe for the Data In (Din) register. This permits several options in the write cycle timing. In a write cycle, if the WRITE input is brought low (active) prior to CAS, the Din is strobed by CAS, and the set-up and hold times are referenced to CAS. If the input data is not available at CAS time or if it is desired that the cycle be a read-write cycle, the WRITE signal will be delayed until after CAS has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of WRITE rather than CAS. (To illustrate this feature, Din is referenced to WRITE in the timing diagrams depicting the read-write and page-mode write cycles while the "early write" cycle diagram shows Din referenced to CAS).

Data is retrieved from the memory in a read cycle by maintaining WRITE in the inactive or high state throughout the portion of the memory cycle in which CAS is active (low). Data read from the selected cell will be available at the output within the specified access time.

Data Output Control

The normal condition of the Data Output (Dout) of the MK 4116 is the high impedance (open-circuit) state. That is to say, anytime CAS is at a high level, the Dout pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. Dout will remain valid from access time until CAS is taken back to the inactive (high level) condition.

If the memory cycle in progress is a read, read-modify write, or a delayed write cycle, then the data output will go from the high impedance state to the active condition, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. Once having gone active, the output will remain valid until CAS is taken to the precharge (logic 1) state, whether or not RAS goes into precharge.

If the cycle in progress is an "early-write" cycle (WRITE active before CAS goes active), then the output pin will maintain the high impedance state throughout the entire cycle. Note that with this type of output configuration, the user is given full control of the Dout pin simply by controlling the placement of WRITE command during a write cycle, and the pulse width of the Column Address Strobe during read operations. Note also that even though data is not latched at the output, data can

remain valid from access time until the beginning of a subsequent cycle without paying any penalty in overall memory cycle time (stretching the cycle).

This type of output operation results in some very significant system implications.

Common I/O Operation — If all write operations are handled in the "early write" mode, then Din can be connected directly to Dout for a common I/O data bus.

Data Output Control— Dout will remain valid during a read cycle from tCAC until CAS goes back to a high level (precharge), allowing data to be valid from one cycle up until a new memory cycle begins with no penalty in cycle time. This also makes the RAS/CAS clock timing relationship very flexible.

Two Methods of Chip Selection— Since Dout is not latched, CAS is not required to turn off the outputs of unselected memory devices in a matrix. This means that both CAS and/or RAS can be decoded for chip selection. If both RAS and CAS are decoded, then a two dimensional (X, Y) chip select array can be realized.

Extended Page Boundary— Page-mode operation allows for successive memory cycles at multiple column locations of the same row address. By decoding CAS as a page cycle select signal, the page boundary can be extended beyond the 128 column locations in a single chip. (See page-mode operation).

Output Interface Characteristics

The three state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The effective resistance to V_{CC} (logic 1 state) is 420 Ω maximum and 135 Ω typically. The resistance to V_{SS} (logic 0 state) is 95 Ω maximum and 35 Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4116 refresh operation. This allows all system logic except the RAS timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

Page Mode Operation

The "Page Mode" feature of the MK 4116 allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the RAS signal at a logic 0 throughout all successive memory cycles in which the row address

is common. This "page-mode" of operation will not dissipate the power associated with the negative going edge of RAS. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

The page boundary of a single MK 4116 is limited to the 128 column locations determined by all combinations of the 7 column address bits. However, in system applications which utilize more than 16,384 data words, (more than one 16K memory block), the page boundary can be extended by using CAS rather than RAS as the chip select signal. RAS is applied to all devices to latch the row address into each device and then CAS is decoded and serves as a page cycle select signal. Only those devices which receive both RAS and CAS signals will execute a read or write cycle.

Refresh

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "RAS-only" cycles. RAS-only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{DD3} specification called out in the MK4116 data sheet.

Power Considerations

Most of the circuitry used in the MK 4116 is dynamic and most of the power drawn is the result of an address strobe edge. Consequently, the dynamic power is primarily a function of operating frequency rather than active duty cycle. This current characteristic of the MK 4116 precludes inadvertent burn out of the device in the event that the clock inputs become shorted to ground due to system malfunction.

Although no particular power supply noise restriction exists other than the supply voltages remain within the specified tolerance limits, adequate decoupling should be provided to suppress high frequency noise resulting from the transient current of the device. This insures optimum system performance and reliability. Bulk capacitance requirements are minimal since the MK 4116 draws very little steady state (DC) current.

In system applications requiring lower power dissipation, the operating frequency (cycle rate) of the MK 4116 can be reduced and, the (guaranteed maximum) average power dissipation of the device will be lowered in accordance with the I_{DD1} (max) spec limit curve illustrated in Figure 4. NOTE: The MK 4116 family is guaranteed to have a maximum I_{DD1} requirement of 35mA @ 375ns

cycle with an ambient temperature range from 0° to 70°C. A lower operating frequency, for example 1 microsecond cycle, results in a reduced maximum I_{DD1} requirement of under 20mA with an ambient temperature range from 0° to 70°C.

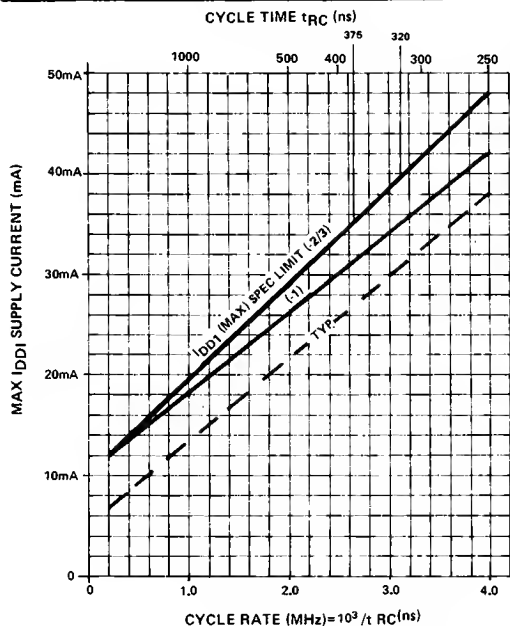


Fig. 4 Maximum I_{DD1} versus cycle rate for device operation at extended frequencies. I_{DD1} (max) curve is defined by the equation:

$$I_{DD1} \text{ (max) mA} = 10 + 9.4 \times \text{cycle rate [MHz]} \text{ for } -2/3 \text{ only}$$

$$I_{DD1} \text{ (max) mA} = 10 + 8.0 \times \text{cycle rate [MHz]} \text{ for } -1 \text{ only}$$

It is possible to operate certain versions of the MK 4116 family (the -2 and -3 speed selections for example) at frequencies higher than 2.66 MHz (375ns cycle), provided all AC operating parameters are met. Operation at shorter cycle times (< 375ns) results in higher power dissipation and, therefore, a reduction in ambient temperature is required.

Although RAS and/or CAS can be decoded and used as a chip select signal for the MK 4116, overall system power is minimized if the Row Address Strobe (RAS) is used for this purpose. All unselected devices (those which do not receive a RAS) will remain in a low power (standby) mode regardless of the state of CAS.

TERMINAL CHARACTERISTICS OF THE MK4027 AND MK4116

Inputs

Addresses, Chip Select and Din — The address, Din and CS input circuitry for the MK4027 and MK4116 is shown in Fig. 5. This particular input circuit has some characteristics that make it particularly useful for the address and data inputs. First of all, it has a low input capacitance which is very important in

large arrays of memory chips where it is desirable to tie many address inputs together and to drive them with a single buffer. This circuit also allows the address hold time for row addresses to be very short. This makes the available 'window' for address multiplexing as wide as possible.

Clocks — The $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WRITE}}$ inputs are basically MOS inverter stages. (Fig 6) The $\overline{\text{RAS}}$ input buffer is always active (the depletion load on the inverter is always supplying current to the inverter) because the device must always be able to respond to RAS transitions. The $\overline{\text{RAS}}$ input buffer accounts for the vast majority of the 1.5 ma of standby current on V_{DD} . The $\overline{\text{CAS}}$ and $\overline{\text{WRITE}}$ buffers differ from the $\overline{\text{RAS}}$ buffer in that the load device is clocked. When the memory is in standby ($\overline{\text{RAS}}$ high), the $\overline{\text{CAS}}$ and $\overline{\text{WRITE}}$ buffers load device is turned off. The input capacitance of the $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WRITE}}$ buffers is fairly high (10pf) in comparison to the address inputs. This is because the input transistors are comparatively large since they have to have good current handling capability and also because of "Miller" effects during input transitions. In most cases this higher input capacitance is not a problem because the number of devices on each $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ buffer is small when compared to the number of devices on each address buffer.

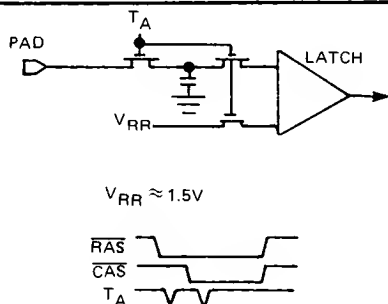


Figure 5 : ADDRESS AND DATA INPUTS

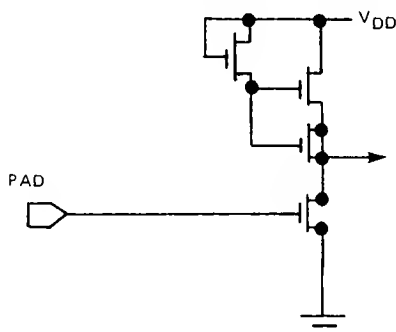


Figure 6: CLOCK INPUT CIRCUIT

MK4116 AND MK4027 COMPATIBLE DESIGNS

Because of their similarities it is very easy to design a memory system that will accommodate either the MK4027 or the MK4116. This is often a very desirable goal because it allows the memory system to be tailored to meet a wide range of overall system requirements. There are some differences however, between the MK4027 and MK4116 that require special consideration.

Refresh And Dout Interaction

In many systems that use transparent refresh, such as this *LSI-11 memory system, it is required that refresh take place immediately after a memory read or write cycle. If refresh takes place after a read cycle it may be required that the read data be held while refresh takes place. The only way to accomplish this in a compatible design is by adding data latches. The MK4027 will, in fact, work without latches if " $\overline{\text{RAS}}$ only" refresh is used. The MK4116, however, requires that $\overline{\text{CAS}}$ be held low to maintain the output data which means that no cycle may start while the data is being held.

Address Multiplexing

The differing address requirements for the MK4027 and MK4116 can be accommodated without jumpers. Fig. 7 shows a multiplexing scheme that uses the 'extra' multiplexer in a 74S158 to supply an inverted address to half the memory. When row addresses are selected two of the multiplexor outputs contain the same address data. The MK4027 will ignore this address data because it is applied to the $\overline{\text{CS}}$ input which is a 'don't care' at $\overline{\text{RAS}}$ time. The MK4116, however sees this input as another address and will strobe it in at $\overline{\text{RAS}}$ time. When column addresses are selected the extra multiplexor contains a complement address. The MK4027 uses this input as a $\overline{\text{CS}}$ input and the MK4116 uses it as another column address. Two high order addresses are used such that they are part of the $\overline{\text{RAS}}$ decode for the MK4027 but are not terms in the $\overline{\text{RAS}}$ decode for the MK4116. The net effect is that for the MK4027 half the chips will receive $\overline{\text{CS}}$ and only one selected row will receive $\overline{\text{RAS}}$. For the MK4116 the column data on half the rows will be reversed around A6.

Generating The Memory Timing

The timing generator for the *LSI-11 memory system has many responsibilities. It must provide the row address hold time (t_{RAH}), it must generate the multiplexing control signal, it must provide column address setup time, it must generate a column address strobe delay, it must generate a valid data or end of write signal, and must provide the necessary precharge interval (T_{RP}).

Any number of methods may be used to generate this timing such as an oscillator driving a counter or a shift register; or a series of one-shots. However, each of these methods has a number of problems. The oscillator is necessarily asynchronous to cycle initiation and the cycle startup problems are acute. The one-shot approach simply cannot be made accurate when short delays are required. The simplest and most reliable solution to generating the necessary timing edges is to use a delay line.

The delay line shown has a 200 ns total delay with 5 taps at 40 ns intervals. This line was chosen because it was a standard 'off the shelf' item and was adequate for prototyping. The delay line timing and resulting system timing for read and write cycles is shown in figs. 9 and 10.

The timing and control logic is shown in Fig. 8. All cycle timing is derived from the delay line. The input to the delay line is a low going signal that propagates to the end of the line and resets the input such that the new memory cycle can be initiated whenever the output of the line returns high.

The synchronous refresh timing is similar to the read cycle timing but the asynchronous refresh (fig. 11) cycle has some interesting features. When the refresh interval timer indicates that a refresh should occur all further external cycles are inhibited from starting. After a 50ns delay if no cycle is in progress the address multiplexor can be switched to select the refresh addresses from the refresh address counter. After an additional 50ns delay to allow refresh addresses to stabilize, the cycle is started and proceeds much like any other cycle except no RPLY is generated and CAS is inhibited.

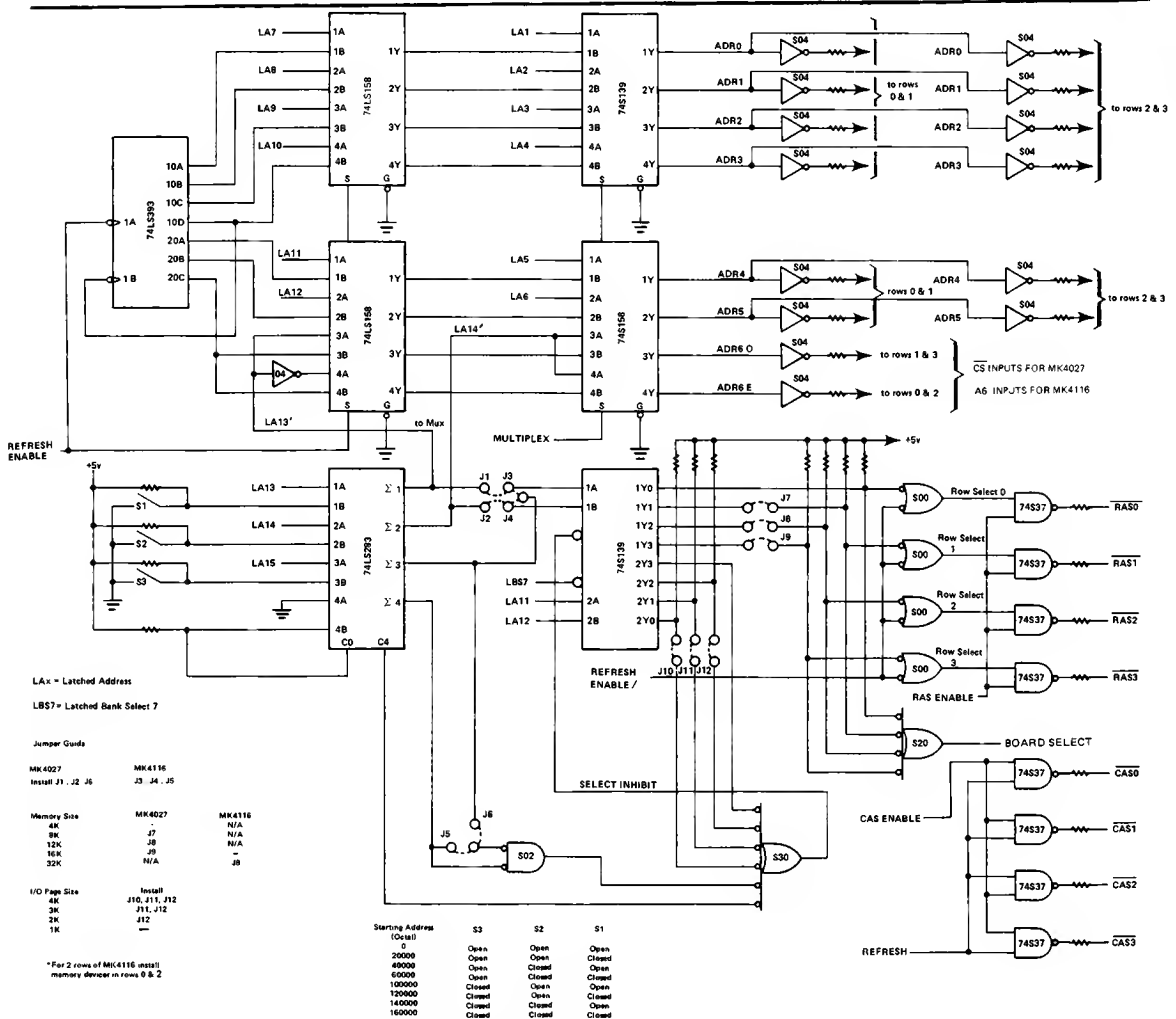


FIG. 7 MEMORY ADDRESS DECODING LOGIC

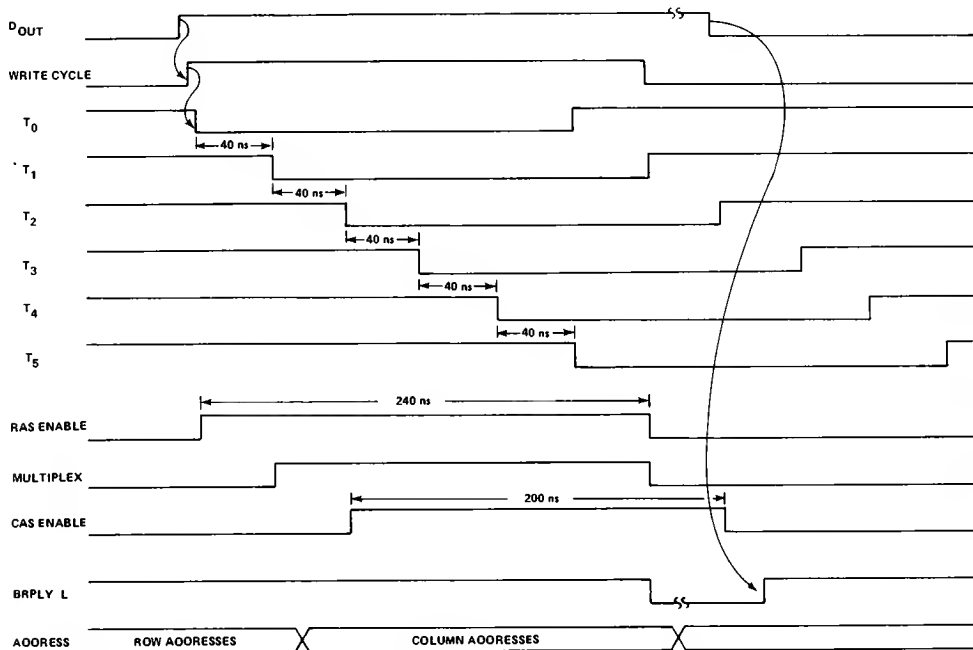


FIG. 10 WRITE CYCLE TIMING

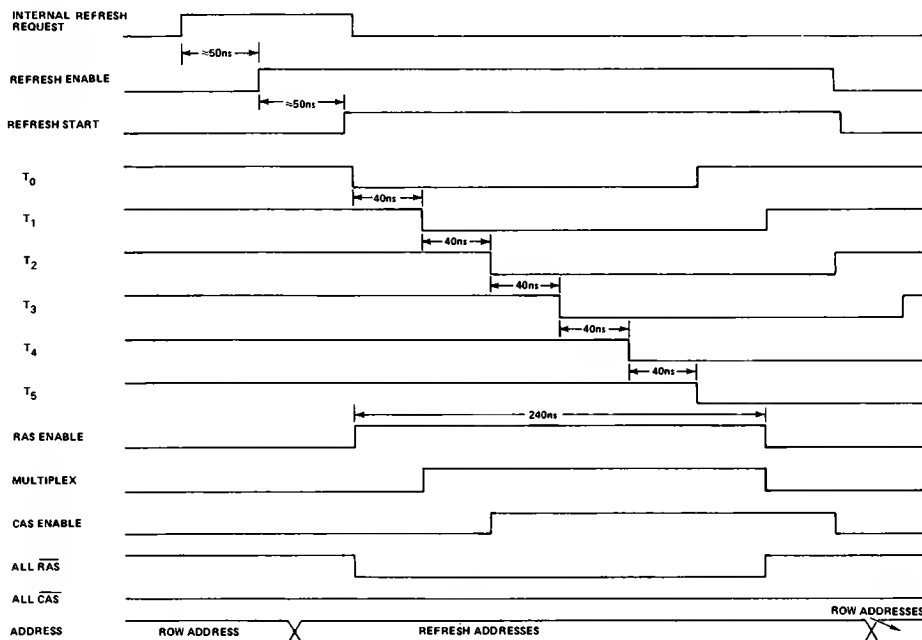


FIG. 11 INTERNAL REFRESH CYCLE TIMING

Refresh Techniques

In most memory systems it is difficult to guarantee that the normal order of events will cause all the rows within a memory to be accessed within the specified refresh interval. For this reason, most dynamic memory systems have special circuitry that will cause extra memory cycles in an ordered manner such that all rows of memory devices are accessed within the 2 ms interval.

There are three commonly used techniques for introducing these extra memory refresh cycles. The first is in a "burst" where all normal memory accesses are inhibited for a fixed period of time while all rows are accessed. The second is "cycle stealing" where single memory cycles are periodically stolen from the CPU in order to refresh a single row. The third and most common is "transparent" where refresh cycles are periodically generated for refresh but they are introduced at a time when the memory is not being accessed and thus they are transparent to the CPU (i.e. the CPU is not affected by refresh).

The *LSI-11 microcode has provisions for performing "burst" refresh and the memory system described here will respond to the "burst" refresh from the LSI-11.* In addition, this memory system also has provisions for "transparent" refresh so that the "burst" refresh on the LSI-11* can be disabled for enhanced real-time system response.

The LSI-11* generates 64 cycles for refresh of 4K dynamic RAMs. The MK4116 requires 128 cycles for refresh. Instead of trying to do two refresh cycles for each synchronous refresh request, the distributed refresh is allowed to run even in the burst mode when the board is populated with MK4116's. Thus, 64 refresh cycles are provided by the LSI-11* and 64 cycles are generated by the on-board refresh running at half speed. In order to eliminate addressing problems the on-board refresh counter is used for all refresh cycles.

Synchronous and Asynchronous Refresh

One of the most important factors in a dynamic memory design is deciding whether the memory refresh will be synchronous or asynchronous. For synchronous refresh, the designer can use some system event (clock) to trigger refresh. In the asynchronous system the designer must provide for a local event to trigger the refresh. With an asynchronous refresh there will usually be cases when a system memory request and local refresh request occur simultaneously. To provide for such circumstances, some arbitration scheme must be present on

the asynchronously refreshed memory. Extreme care must be taken in the design of the arbitration logic because if it does not contain adequate safeguards the memory system can (and will) malfunction causing some rather interesting and impossible to duplicate errors. Because of the inherent difficulties of asynchronous refresh it should be used only as a last resort. This is probably why DEC included the refresh microcode in the *LSI-11* to allow refresh to be system synchronous.

The arbitration logic for this memory system is shown in Fig. 8. For normal read or write cycles, without refresh interference, the and-or-invert (AOI) sets the cycle start latch which feeds the delay line generating the memory timing signals. When an asynchronous refresh must take place the INTERNAL REFRESH REQUEST signal inhibits any bus requested cycles (read, or write) from setting the cycle start latch. After a short delay the output of the cycle start latched is sampled and if no cycle is in progress the address multiplexer is switched to select the refresh addresses and the refresh cycle is allowed to start. In the event of the refresh request overriding the read/write requests, the output of the AOI might not allow the cycle start latch to set properly and a timing glitch could propagate through the delay line. To prevent such a catastrophic event, the output of the open collector AOI gate has an RC delay that serves to stretch any low going pulse making it wide enough to insure proper setting of the latch.

The refresh enable has an alternate path that bypasses the arbitration delay. This is used for synchronous refresh cycles that are generated by the LSI-11.* The arbitration can be bypassed because it is possible to merge the synchronous refresh requests and not cause a conflict with a normal cycle.

DRIVING MOS WITH TTL

Driver Characteristics

For the Schottky devices the important parameters are the output impedance in the high and low level output state and the rise and fall time of the signal. The worst case high level output impedance can be calculated by using the I_{O5} values for the device and observing that the voltage across the current limiting resistor in the Schottky output stage is given by:

$$V = V_{CC} - 2V_{BE} + V_D$$

The larger the voltage across the resistor the higher its resistance, so by assuming a small value for V_{BE} (0.65V) and a large value for the drop across the Schottky diode in the driver (0.6V), a safe worst case number can be calculated.

For the low level output impedance the low level output current (I_{OL}) and low level output voltage (V_{OL}) can be used. Assuming a small value for the low level open circuit output voltage (V_{OLO}) of about 0.2 volts the output impedance can be estimated by:

$$R_{OL} = \frac{V_{OL} - V_{OLO}}{I_{OL}}$$

Calculations for the 74S04 give a worst case output impedance of about 114Ω in the high level state and about 15Ω in the low level state. The 74S04 has a worst case high level output impedance of about 89Ω and a worst case low level impedance of about 5Ω . The values for the 74S04 can be used for most Schottky TTL functions because the output structures are similar.

Line Termination

It is not obvious that line termination is necessary, but it is. If no termination is used, a low going signal will be injected into the line having an amplitude that can be calculated by dividing the signal swing between the source impedance and the characteristic impedance of the line. For a 3 volt negative signal swing from a 75S37 into a 50Ω line the transmitted signal will have an amplitude of 2.7 volts. This signal will propagate to the end of the line, be 100% reflected at the end of the line and return to the driver. At the driver the signal will reflect about 80% and 180° out of phase. In the case where the fall time of the signal is shorter than the two way propagation delay of the line the resulting reflection from the driver will cause the signal to swing positive at the end of the line to about 2.0 volts. This amount of ringing obviously cannot be tolerated so some types of termination must be used.

Termination of the line at the 'receiving' end is one method that is often used in TTL transmission line systems. This type of termination has several drawbacks. If a simple pullup resistor to +5 volts is used, the low level DC current through a resistor with a resistance equal to the impedance of the line will in most cases consume almost all of the drive capability of the bus driver. Even if the line impedance is as high as 200Ω the logic '0' level current through a 200Ω resistor would be 25 mA.

When considering termination of lines in a memory array it becomes very impractical to use receiving end termination. If terminating pairs were used the driver would have to be capable of sinking about 30 mA for each terminated line because of the low impedance of signal lines in a memory array.

The best choice for line termination is to use a series resistor at the driver. This approach is not practical when driving TTL loads because the I_{LL} current causes a loss of logic '0' level. MOS loads however, have such small current requirements that this is not a problem. A series resistor of 100Ω with 100 MOS loads would produce only 0.1 volt of signal level loss. Series damping has an additional advantage over parallel termination in that it draws no DC supply current. For proper termination of the line it is necessary to match the low level source impedance of the driver to the impedance of the line being driven. This reduces ringing in the low level where the margins are most critical. In cases where multiple lines are being driven by the driver, the parallel combination of the lines should be used for the line impedance and the series resistor chosen accordingly. In practice, the resistor value is best chosen empirically. The board should be designed to accommodate the resistors and then different values tried on a prototype. The waveform with the ideal resistor will be slightly underdamped.

DELAY TIME CALCULATIONS

The switching delays for TTL devices driving capacitive loads such as memory signal lines can best be estimated by using the equation for the charge time of an RC circuit. R will be the maximum output impedance of the gate plus the series damping resistance, and C is the sum of the capacitances of the inputs being driven plus the capacitance of the board. When calculating the capacitance of the line the data sheet typical values for capacitance should be used rather than the maximums. This is because high input capacitance is not a function of the wafer lot, and the probability of having mostly worst case capacitance on the same signal line is very very small.

The equation for the maximum rise time is:

$$t_r = -RC \ln \frac{3.85V - V_{IH}}{3.85V - 0.2V} = -RC \ln \frac{3.85V - V_{IH}}{3.65V}$$

$V_{IH} = 2.2$ volts for addresses on 4027

$V_{IH} = 2.4$ volts for addresses on 4116 and clocks on 4027

$V_{IH} = 2.7$ volts for clocks on 4116

The fall time is:

$$t_f = -RC \ln \frac{0.8}{3.95} = 1.6RC$$

SIGNAL	V_{IH}	DRIVER	SERIES RESISTOR	LOADS/ LINE	LOAD CAPACITANCE	t_{PLH}	t_{PHL}
4027 CLOCKS	2.4	74S37	22Ω	16	148pF	15ns	6.5ns
4116 CLOCKS	2.7	74S37	22Ω	16	148pF	19ns	6.5ns
4027 ADDRESSES	2.2	74S37	22Ω	32	169pF	18ns	10ns
4116 ADDRESSES	2.4	74S04	22Ω	32	168pF	21ns	10ns

Table 1 Calculated Propagation Delays for Memory Signal Buffers

Power Distribution and Decoupling

The layout for dynamic memories is of special importance. Layout techniques that have been used successfully in the past for older generation MOS memories are simply inadequate for current state-of-the-art memories such as the MK4027 and MK4116. The newer devices have shallow diffusions that make possible fast memory devices but the shallow diffusions and fast switching speeds create larger current transients with higher frequency components than did the older designs. (Fig. 12) In order to tame these current transients and prevent them from generating voltage spikes that can cause loss of data and 'soft' errors every effort must be made to minimize the impedance in the decoupling path for the device.

The decoupling path is the trace distance from a power pin through a decoupling capacitor and to package ground. The impedance of this path is determined by the line inductance and the series impedance of the decoupling capacitor. Because the current transients on the MK4027 and MK4116 have significant harmonic content up to 100MHz the line inductance is one of the most critical factors. The line inductance can be minimized either by providing a power plane or by gridding the power. In order to increase the effectiveness of the grided power, decoupling capacitors should be placed judiciously. A capacitor placement that has shown to be very effective is shown in Fig. 13. V_{DD} and V_{BB} are decoupled at every other chip with $0.1\mu\text{F}$ capacitors such that the decoupling creates a 'checkerboard' pattern. This particular pattern was used on the LSI-11* memory board and measurements of the V_{DD} noise with a differential probe showed that the noise was below 400 mV peak-to-peak.

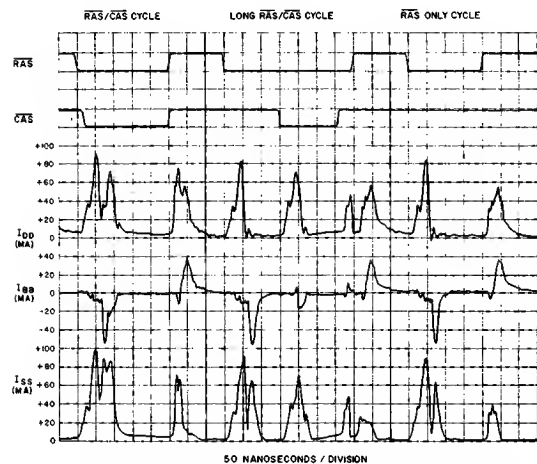


FIG. 12 CURRENT WAVEFORMS FOR MK4116

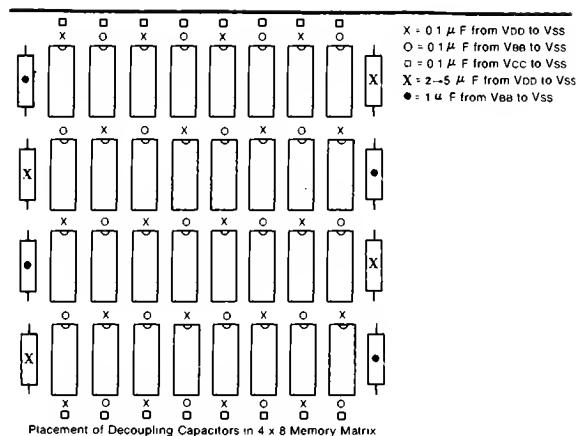


FIG. 13

While the $0.1\mu\text{F}$ decoupling capacitors are more than adequate for suppression of transients some larger bulk capacitors should be used to provide enough energy storage to prevent supply droop. The long term (cycle time) current requirements of the MK4027 and MK4116 are fairly low at 35 mA max. Assuming 64 memory devices all cycling at the maximum rate of 375 ns with 120 ns of precharge only $8.4\mu\text{F}$ of capacitance is required to keep the voltage drop below .1 volts. As with the high frequency decoupling it is good practice to distribute the bulk capacitance around the storage matrix to minimize the effects of the inductive and resistive voltage drops.

Decoupling of the V_{CC} (+5) supply is fairly non-critical. In most cases only one row of memory devices is accessed at a time. The V_{CC} supply, therefore only needs to provide enough current to charge one Dout line for each column of memories. The V_{CC} decoupling capacitors ($0.1\mu\text{F}$) were placed at the top and bottom of each column of memories. The V_{CC} voltage at each device was measured when a data '1' was being read. The drop in V_{CC} was less than 300 mV. Calculations of the resultant rise time indicate that a 300 mV decrease in V_{CC} would cause less than a 10% increase in output rise time at $V_{CC}=4.75$ volts.

Bulk decoupling of the V_{CC} supply is usually not required in the memory. The DC current loading of the V_{CC} supply is dependent on the TTL loading and is usually quite small (less than 1mA for each 8 bits in the output word). The bulk decoupling, therefore, can be provided by the bulk capacitance used for the TTL.

The other performance advantages of gridding the power are the crosstalk between signal lines is decreased because of the close proximity of ground; and ground voltage differentials between the TTL drivers and the memory devices is reduced enhancing the noise immunity to switching transients from the TTL devices.

Most of the layout techniques used in the memory array should be extended to the TTL circuitry on all boards. Ground should be grided wherever possible. The decoupling paths should be kept as short as possible. Board ground should connect to backplane ground at as many points as possible.

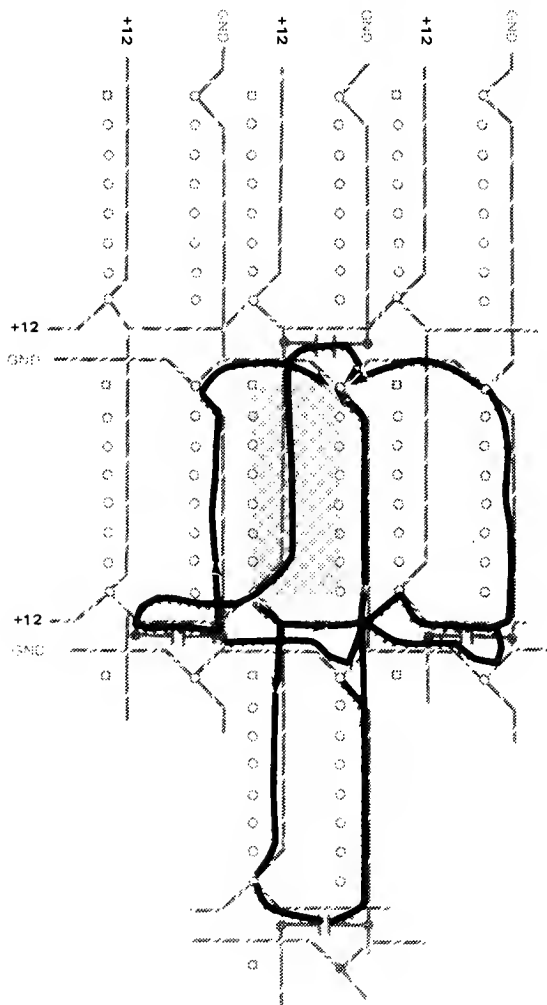


FIG. 14

Decoupling Currents With Grided Power And
Checkerboard Decoupling

Signal Lines

Routing of the signal lines within the memory matrix is fairly straight forward. Address and clock lines can be daisy chained along each row and cause no cross-

talk problems when a good ground mesh is employed. In cases where multiple rows of chips are driven by the same TTL buffer the lines should be vertically bused outside the memory and tapped for each horizontal row of chips. The lines should in no case be snaked through the memory. Snaked lines are more susceptible to externally induced noise and crosstalk because of the longer path to the signal source.

Naturally, all lines should be kept as short as possible. This implies that the signal drivers and receivers should be physically close to the memory array. In cases where there are a large number of memory chips in each row the address drivers should be placed in the center of the array. (Fig. 16) If the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ buffers drive one row of memory chips each can be placed either in the center of the array or on the side of the array. If the drivers will not fit in the middle of the matrix, they may be placed below the matrix. The signal lines would then be routed vertically and 'T'd' for each horizontal connection. In such cases, it is recommended that each stub be the same length in order to minimize the distortion of the signal edges caused by mismatched stubs.

DYNAMIC
RAMS

MISCELLANEOUS POWER CONSIDERATIONS

Power Sequencing

The data sheets for the MK4027 and MK4116 state that no special power sequencing is required for proper device operation. This does not mean that the power sequencing should be ignored. In many systems the power supply lines exhibit overshoot on power up. This can cause V_{DD} at the memory to exceed data sheet limits for a short period of time. If V_{BB} is not applied when V_{DD} overshoots, breakdown can occur and destroy the memory. If a system does have this overshoot, sequencing the supplies so that V_{BB} is applied first will provide extra margin and help prevent device destruction.

The data sheet specified that V_{BB} should not be allowed to go positive with respect to ANY other input. If it does, injection currents can occur and cause loss of functionality. Special precautions should be taken in the V_{BB} power distribution to prevent this occurrence. A high current Schottky diode from V_{BB} to ground can protect against many of the hazards such as an open V_{BB} supply or a momentary short to a signal or power line. Note that the layout in Fig. 15 has the V_{BB} run next to ground in the memory array. This will help reduce the chance of memory damage should a screwdriver or scope probe get loose in the system.

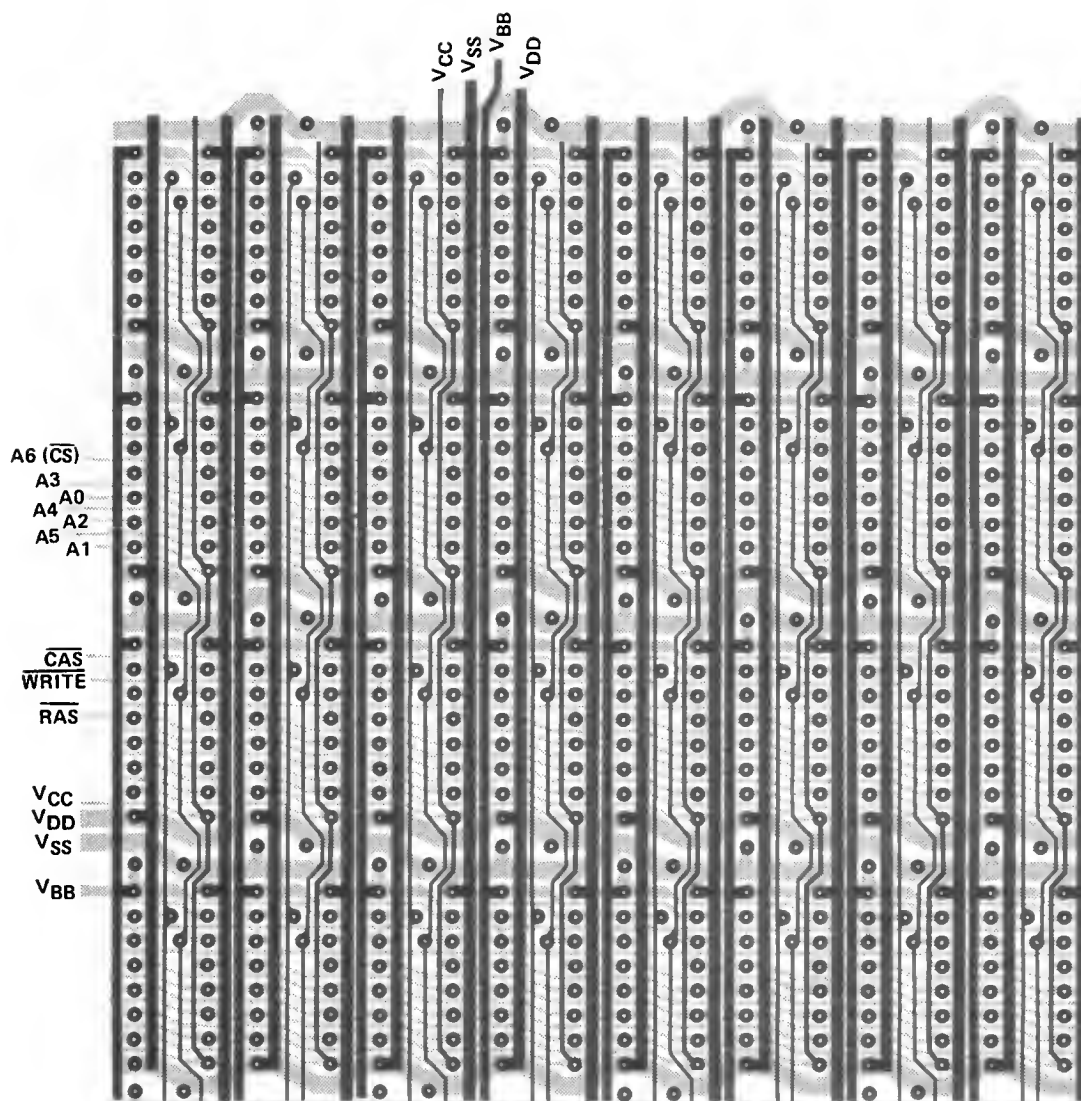


FIG. 15 SUGGESTED P.C. LAYOUT FOR MK4027 OR MK4116

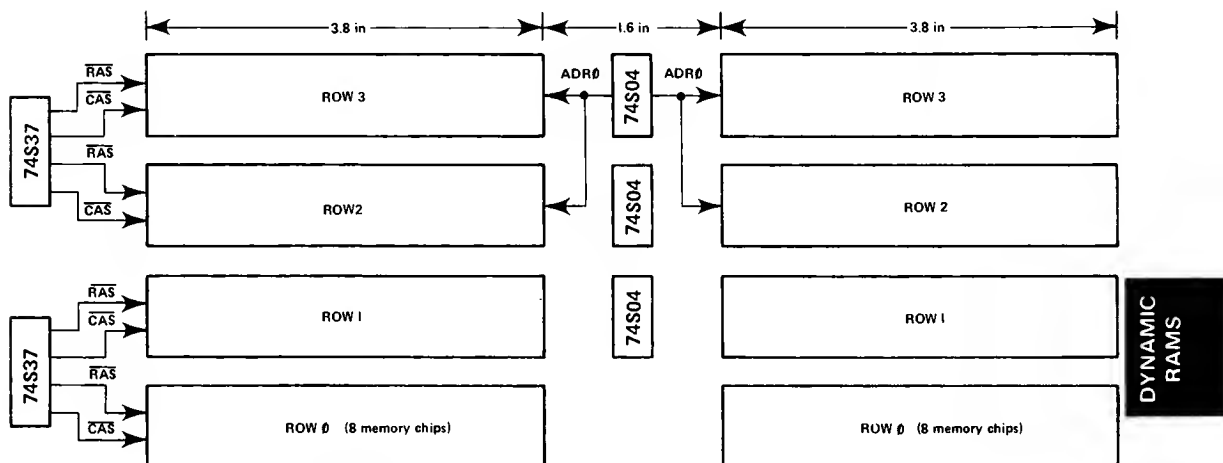


FIG. 16 TYPICAL PLACEMENT FOR DRIVERS WITHIN MEMORY MATRIX

Power Calculations

Calculation of the V_{DD} supply current involves a fairly simple averaging procedure. The active refresh and standby currents are averaged over any given time period and multiplied times the maximum supply voltage to give the maximum power dissipation. The equation for the maximum average I_{DD} is given by:

$$I_{DDAVE} = [n_{ACC} \times c_{ACC} [10mA (t_{RAS} + 120ns) + 9.4mA \times 10^{-6} s] + n_{REF} \times c_{REF} [10mA (t_{RRAS} + 120ns) + 6.5mA \times 10^{-6}s] + I_{DD2} [n_{TOTAL} \times 1s - n_{ACC} \times c_{ACC}(t_{RAS} + 120ns) - n_{REF} \times c_{REF} (t_{RRAS} + 120ns)] / 1s$$

n_{ACC} = Number of devices accessed per normal cycle

n_{REF} = Number of devices refreshed per \overline{RAS} only refresh cycle

n_{TOTAL} = Total number of devices in system

c_{ACC} = Frequency of normal accesses

c_{REF} = Frequency of refresh cycles

t_{RAS} = \overline{RAS} active time for normal cycles

t_{RRAS} = \overline{RAS} active time for refresh cycles

This equation takes into account the variations in current vs operating frequency and current vs duty cycle and provides for differences in number of devices in standby and number of devices active. As an example, assume a board with 8 rows of 8 chips per row. Refresh will occur every $7\mu s$ but only half the devices will be refreshed every refresh cycle. The other parameters are:

$$n_{ACC} = 8$$

$$n_{REF} = 32$$

$$n_{TOTAL} = 64$$

$$c_{ACC} = 2MHz$$

$$c_{REF} = 1/7\mu s \sim 143KHz$$

$$t_{RAS} = 240ns$$

$$t_{RRAS} = 200ns$$

$$I_{DD2} = 1.5ma (MK4116)$$

$$I_{DDAVE} = 8 \times 2 \times 10^6 [1 \times 10^{-2}A (240 \times 10^{-9}s)$$

$$+ 9.4 \times 10^{-3}A \times 1 \times 10^{-6}s] + 32 \times 143 \times 10^3$$

$$[1 \times 10^{-2}A (200 \times 10^{-9}s + 120 \times 10^{-9}s) + 6.5$$

$$\times 10^{-3} \times 1 \times 10^{-6} \text{ s}] + 1.5 \times 10^{-3} [64 \times 10^{-8} \\ \times 2 \times 10^6 (240 \times 10^{-9} \text{ s} + 120 \times 10^{-9} \text{ s}) - 32 \times 143 \\ \times 10^3 (200 \times 10^{-9} \text{ s} + 120 \times 10^{-9} \text{ s})]$$

$$I_{DD\text{AVE}} = 337.6 \text{ mA}$$

Power calculations for the LSI-11 board using distributed refresh and with MK4027 gives:

$$n_{\text{ACC}} = 16$$

$$n_{\text{REF}} = 16, 32, 48, 64$$

$$n_{\text{TOTAL}} = 16, 32, 48, 64$$

$$c_{\text{ACC}} = 1 \text{ MHz (bus limit)}$$

$$c_{\text{REF}} = 32.5 \text{ KHz}$$

$$t_{\text{RAS}} = 240 \text{ ns}$$

$$t_{\text{RRAS}} = 240 \text{ ns}$$

$$I_{\text{DD2}} = 2.0 \text{ mA}$$

Yielding a maximum I_{DD} current of 233 mA for 4K words, 270 mA for 8K, 307 mA for 12K and 344 mA for 16K.

Using the MK4116 we have:

$$n_{\text{ACC}} = 16$$

$$n_{\text{REF}} = 16, 32$$

$$n_{\text{TOTAL}} = 16, 32$$

$$c_{\text{ACC}} = 1 \text{ MHz}$$

$$c_{\text{REF}} = 65 \text{ KHz}$$

$$t_{\text{RAS}} = 240 \text{ ns}$$

$$t_{\text{RRAS}} = 240 \text{ ns}$$

$$I_{\text{DD2}} = 1.5 \text{ mA}$$

This gives a maximum average I_{DD} current of 233 mA for 16K and 267 mA for 32K.

It is interesting to note that on a per chip basis the MK4116 actually consumes less power than the MK4027 even though the MK4116 is refreshed at twice the rate.

Z80 INTERFACING TECHNIQUES FOR DYNAMIC RAM

Application Note

INTRODUCTION

Since the introduction of second generation microprocessors, there has been a steady increase in the need for larger RAM memory for microcomputer systems. This need for larger RAM memory is due in part to the availability of higher level languages such as PL/M, PL/Z, FORTRAN, BASIC and COBOL. Until now, when faced with the need to add memory to a microcomputer system, most designers have chosen static memories such as the 2102 1Kx1 or possibly one of the new 4Kx1 static memories. However, as most mini or mainframe memory designers have learned, 16-pin dynamic memories are often the best overall choice for reliability, low power, performance, and board density. This same philosophy is true for a microcomputer system. Why then have microcomputer designers been reluctant to use dynamic memory in their system? The most important reason is that second generation microprocessors such as the 8080 and 6800 do not provide the necessary signals to easily interface dynamic memories into a microcomputer system.

Today, with the introduction of the Z80, a true third generation microprocessor, not only can a microcomputer designer increase system throughput by the use of more powerful instructions, but he can also easily interface either static or dynamic memories into the microcomputer system. This application note provides specific examples of how to interface 16-pin dynamic memories to the Z80.

OPERATION OF 16-PIN DYNAMIC MEMORIES

The 16-pin dynamic memory concept, pioneered by MOSTEK, uses a unique address multiplexing technique which allows memories as large as 16,384 bits x 1 to be packaged in a 16-pin package. For example the MK4027 (4,096x1 dynamic MOS RAM) and the MK4116 (16,384x1 dynamic MOS RAM) both use address multiplexing to load the address bits into memory. The MK4027 needs 12 address bits to select 1 out of 4,096 locations, while the MK4116 requires 14 bits to select 1 out of 16,384. The internal memories of the MK4027 and MK4116 can be thought of as a matrix. The MK4027 matrix can be thought of as 64x64, and the MK4116 as 128x128. To select a particular location, a row and column address is supplied to the memory. For the MK4027, address bits A₀-A₅ are the row address, and bits A₆-A₁₁

are the column addresses. For the MK4116, address bits A₀-A₆ are the row address, and A₇-A₁₃ are the column address. The row and column addresses are strobed into the memory by two negative going clocks called Row Address Strobe (RAS) and Column Address Strobe (CAS). By the use of RAS and CAS, the address bits are latched into the memory for access to the desired memory location.

Dynamic memories store their data in the form of a charge on a small capacitor. In order for the dynamic memory to retain valid data, this charge must be periodically restored. The process by which data is restored in a dynamic memory is known as refreshing. A refresh cycle is performed on a row of data each time a read or write cycle is performed on any bit within the given row. A row consists of 64 locations for the MK4027 and 128 locations for the MK4116. The refresh period for the MK4027 and the MK4116 is 2ms which means that the memory will retain a row of data for 2ms without a refresh. Therefore, to refresh all rows within 2ms, a refresh cycle must be executed every $32\mu\text{s}$ ($2\text{ms} \div 64$) for the MK4027 and $16\mu\text{s}$ ($2\text{ms} \div 128$) for the MK4116.

To ensure that every row within a given memory is refreshed within the specified time, a refresh row address counter must be implemented either in external hardware or as an internal CPU function as in the Z80. (Discussed in more detail under Z80 Refresh Control and Timing.) The refresh row address counter should be incremented each time that a refresh cycle is executed. When a refresh is performed, all RAMs in the system should be loaded with the refresh row address. For the MK4027 and the MK4116, a refresh cycle consists of loading the refresh row address on the address lines and then generating a RAS for all RAMs in the system. This is known as a RAS only refresh. The row that was addressed will be refreshed in each memory. The RAS only refresh prevents a conflict between the outputs of all the RAMs by disabling the output on the MK4116, and maintaining the output state from the previous memory cycle on the MK4027.

Z80 TIMING AND MEMORY CONTROL SIGNALS

The Z80 was designed to make the job of interfacing

to dynamic memories easier. One of the reasons the Z80 makes dynamic memory interfacing easier is because of the number of memory control signals that are available to the designer. The Z80 control signals associated with memory operations are:

MEMORY REQUEST (\overline{MREQ}) - Memory request signal indicating that the address bus holds a valid memory address for a memory read, memory write, or memory refresh cycle.

READ (\overline{RD}) - Read signal indicating that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

WRITE (\overline{WR}) - Write signal indicating that the CPU data bus hold valid data to be stored in the addressed memory or I/O device.

REFRESH (\overline{RFSH}) - Refresh signal indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current \overline{MREQ} signal should be used to generate a refresh cycle for all dynamic memories in the system.

Figures 1a, 1b, and 1c show the timing relationships of the control signals, address bus, data bus and system clock Φ . By using these timing diagrams, a set of equations can be derived to show the worst case access times needed for dynamic memories with the Z80 operating at 2.5MHz.

The access time needed for the op code fetch cycle and the memory read cycle can be computed by equations 1 and 2.

$$(1) \ t_{ACCESS\ OP\ CODE} = 3(t_c/2) \cdot t_{DL\overline{\Phi}(MR)} \cdot t_{S\overline{\Phi}(D)}$$

where: t_c = Clock period

$$\begin{aligned} t_{DL\overline{\Phi}(MR)} &= \overline{MREQ} \text{ delay from falling edge of clock.} \\ t_{S\overline{\Phi}(D)} &= \text{Data setup time to rising edge of clock during op code fetch cycle.} \end{aligned}$$

$$\text{let: } t_c = 400\text{ns}; \ t_{DL\overline{\Phi}(MR)} = 100\text{ns}; \ t_{S\overline{\Phi}} = 50\text{ns}$$

$$\text{then: } t_{ACCESS\ OP\ CODE} = 450\text{ns}$$

$$(2) \ t_{ACCESS\ MEMORY\ READ} = 4(t_c/2) \cdot t_{DL\overline{\Phi}(MR)} \cdot t_{S\overline{\Phi}(D)}$$

where: t_c = Clock period

$$\begin{aligned} t_{DL\overline{\Phi}(MR)} &= \overline{MREQ} \text{ delay from falling edge of clock} \\ t_{S\overline{\Phi}(D)} &= \text{Data Setup time to falling edge of clock} \\ \text{let: } t_c &= 400\text{ns}; \ t_{DL\overline{\Phi}(MR)} = 100\text{ns}; \ t_{S\overline{\Phi}(D)} = 60\text{ns} \\ \text{then: } t_{ACCESS\ MEMORY\ READ} &= 640\text{ns} \end{aligned}$$

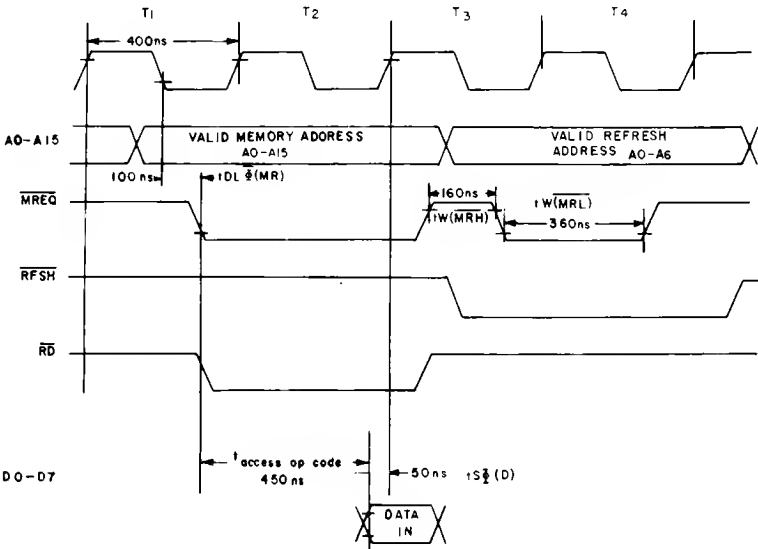
The access times computed in equations 1 and 2 are overall worst case access times required by the CPU. The overall access times must include all TTL buffer delays and the access time for the memory device. For example, a typical dynamic memory design would have the following characteristics, (see Figure 2).

The example in Figure 2 shows an overall access time of 336ns. This would more than satisfy the 450ns required for the op code fetch and the 640ns required for a memory read.

CPU \overline{MREQ} buffer delay	12ns (8T97)
Memory gating and timing delays	40ns
Memory device access time	250ns (MK4027/4116-4)
Memory data bus buffer delay	17ns (8T28)
CPU data bus buffer delay	17ns (8T28)
	<u>336ns</u>

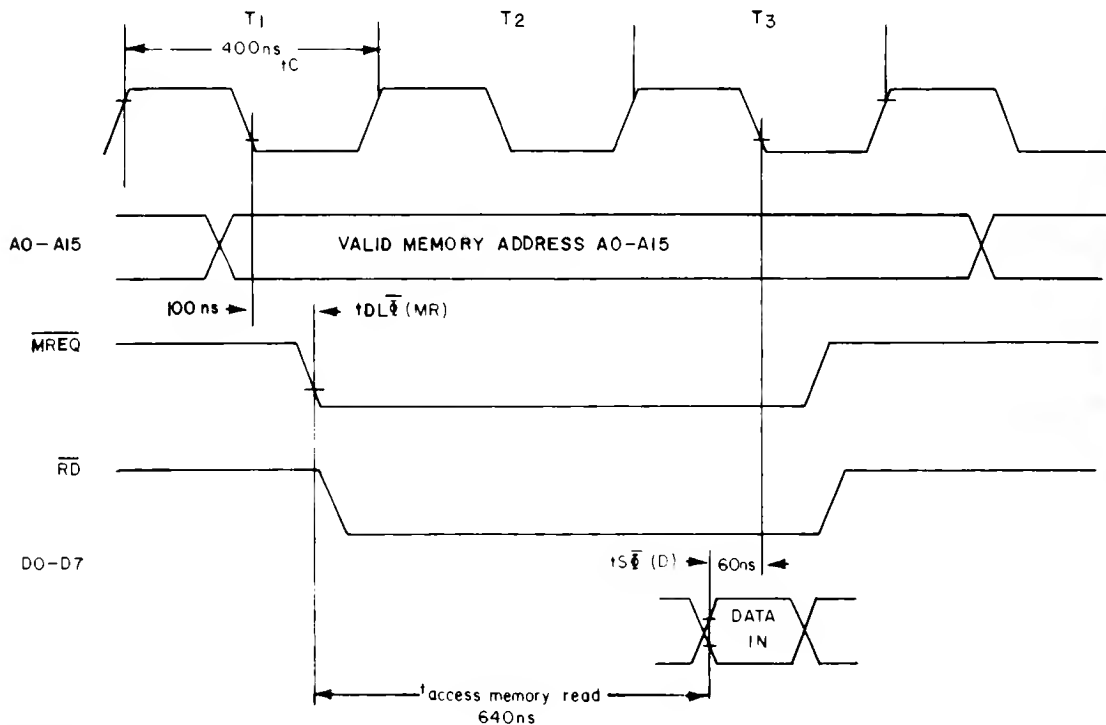
OP CODE FETCH TIMING

Figure 1a.



MEMORY READ TIMING

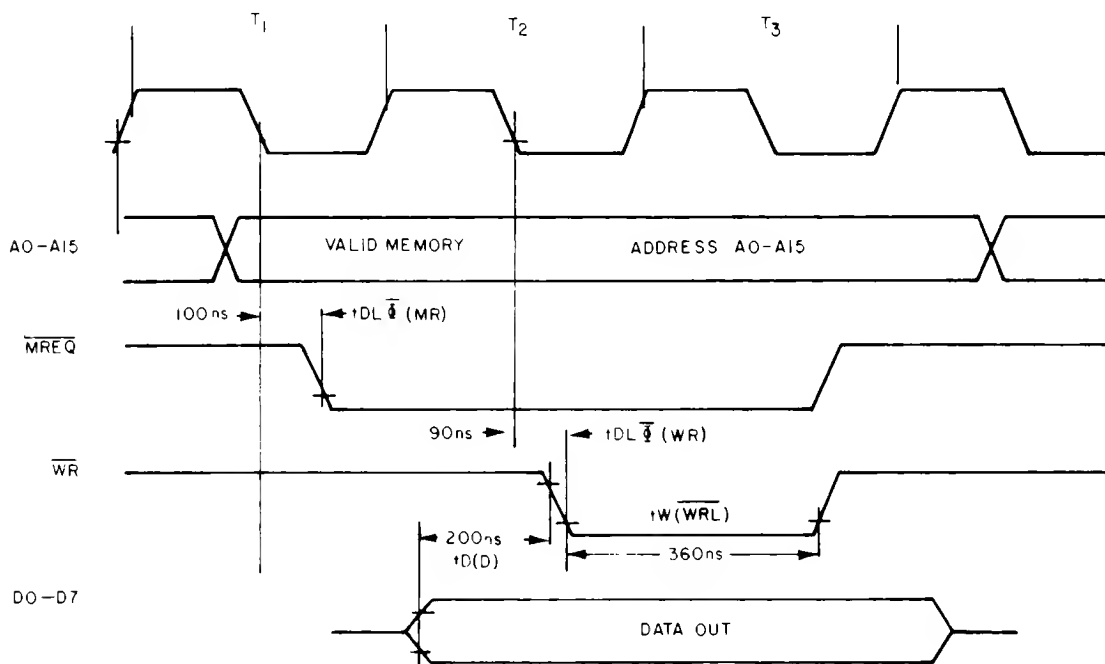
Figure 1b.



DYNAMIC
RAMS

MEMORY WRITE TIMING

Figure 1c.



Z80 REFRESH CONTROL AND TIMING

One of the most important features provided by the Z80 for interfacing to dynamic memories is the execution of a refresh cycle every time an op code fetch cycle is performed. By placing the refresh cycle in the op code fetch, the Z80 does not have to allocate time in the form of "wait states" or by "stretching" the clock to perform the refresh cycle. In other words, the refresh cycle is "totally transparent" to the CPU and does not decrease the system throughput (see Figure 1a). The refresh cycle is transparent to the CPU because, once the op code has been fetched from memory during states T₁ and T₂, the memory would normally be idle during states T₃ and T₄.

Therefore, by placing the refresh in the T₃ and T₄ states of the op code fetch, no time is lost for refreshing dynamic memory. The critical timing parameters involving the Z80 and dynamic memories during the refresh cycle are: $t_W(MRH)$ and $t_W(MRL)$. The parameter known as $t_W(MRH)$ refers to the time that \overline{MREQ} is high during the op code fetch between the fetch of the op code and the refresh cycle. This time is known as "precharge" for dynamic memories and is necessary to allow certain internal nodes of the RAM to be charged-up for another memory cycle. The equation for the minimum $t_W(MRH)$ time period is:

$$(3) \quad t_W(MRH) = t_W(\Phi H) + t_f - 30$$

where: $t_W(\Phi H)$ is clock pulse width high
 t_f is clock fall time

let: $t_W(\Phi H) = 180\text{ns}$; $t_f = 10\text{ns}$
 then: $t_W(MRH) = 160\text{ns (min)}$

A $t_W(MRH)$ of 160ns is more than adequate to meet the worst case precharge times for most dynamic RAMs. For example, the MK4027-4 and the MK4116-4 require a 120ns precharge. The other refresh cycle parameter of importance to dynamic RAMs is $t_W(MRL)$, (the time that \overline{MREQ} is low during the refresh cycle). This time is important because \overline{MREQ} is used to directly generate \overline{RAS} . The equation for the minimum time period is:

$$(4) \quad t_W(MRL) = t_c - 40$$

where: t_c is the clock period

let: $t_c = 400\text{ns}$
 then: $t_W(MRL) = 360\text{ns}$

A 360ns $t_W(MRL)$ exceeds the 250ns min \overline{RAS} time required for the MK4027-4 and the MK4116-4.

By controlling the refresh internally with the Z80, the designer must be aware of one limitation. The limitation is that to refresh memory properly, the Z80 CPU must be able to execute op codes since the refresh cycle occurs during the op code fetch. The following conditions cause the execution of op codes to be inhibited, and will destroy the contents of dynamic memory.

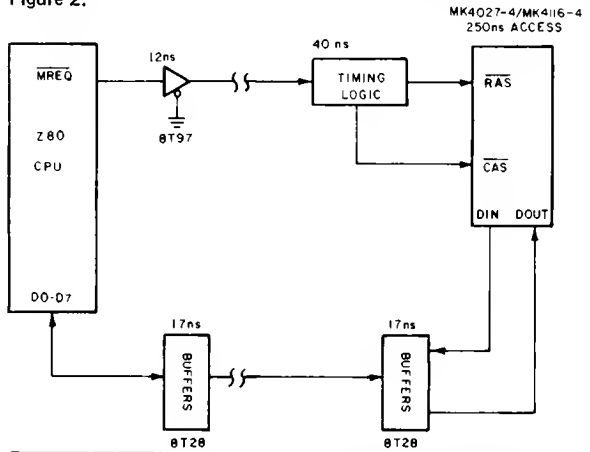
- (1) Prolonged reset > 1ms
- (2) Prolonged wait state operation > 1ms
- (3) Prolonged bus acknowledge (DMA) > 1ms
- (4) Φ clock of < 1.216 MHz for 16K RAMs
 < .608 MHz for 4K RAMs

The clocks rate in number 4 are based on the Z80 continually executing the worst case instruction which is an EX (SP), HL that executes in 19 T states. Therefore, by operating the Z80 at or above these clocks frequencies, the user is ensured that the dynamic memories in the system will be refreshed properly.

Remember to refresh memory properly, the Z80 must be able to execute op codes!

DELAY FOR A TYPICAL MEMORY SYSTEM

Figure 2.



SUPPORT CIRCUITS FOR DYNAMIC MEMORY INTERFACE

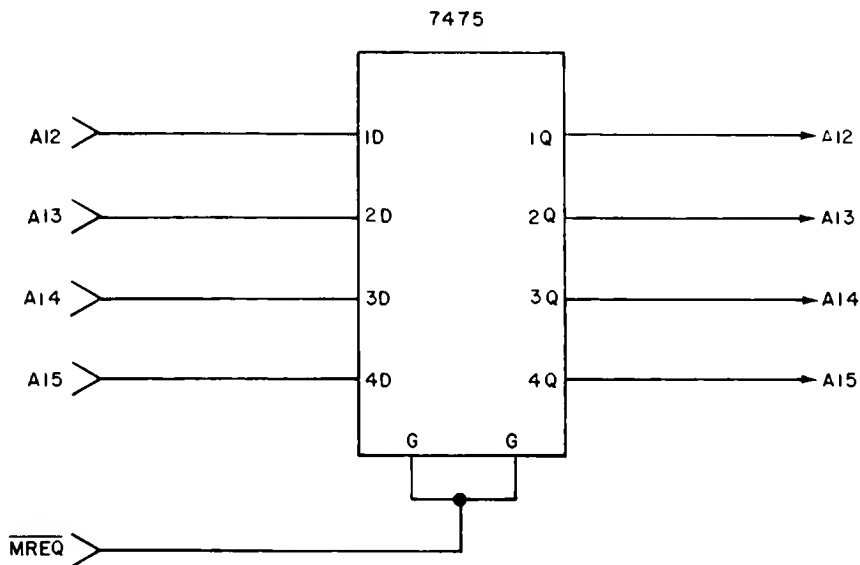
Two support circuits are necessary to ensure reliable operation of dynamic memory with the Z80.

The first of these circuits is an address latch shown in Figure 3. The latch is used to hold addresses A₁₂-A₁₅ while \overline{MREQ} is active. This action is necessary because the Z80 does not ensure the validity of the address bus at the end of the op code fetch (see Figure 4). This action does not directly affect dynamic memories because they latch addresses internally. The problem comes from the address decoder which generates \overline{RAS} . If the address lines which drive the decoder are allowed to change while \overline{MREQ} is low, then a "glitch" can occur on the \overline{RAS} line or lines (if more than one row of RAMs are used) which may have the effect of destroying one row of data.

The second support circuit is used to generate a power on and short manual reset pulse. Recall from the discussion under Z80 Timing and Memory Con-

ADDRESS LATCH

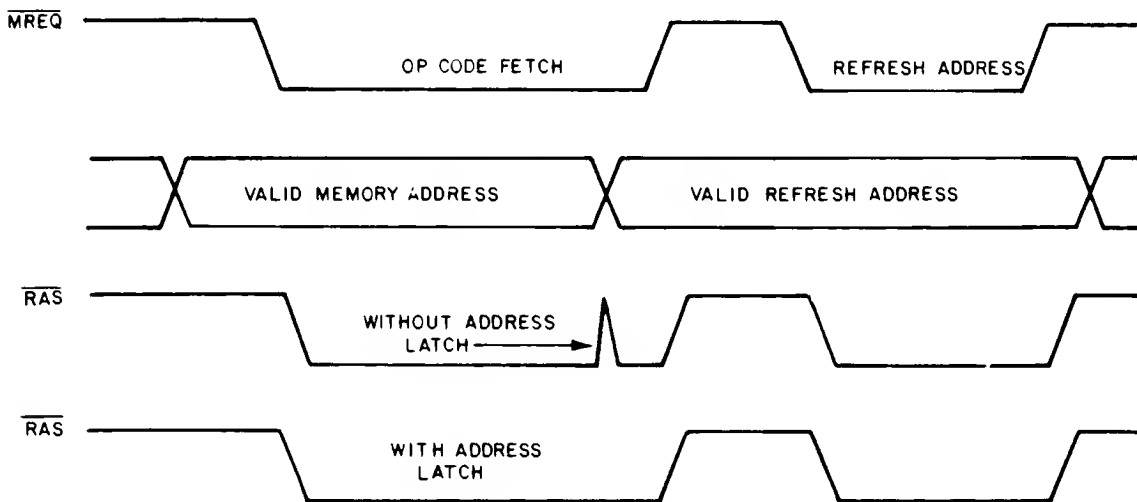
Figure 3.



DYNAMIC
RAMS

RAS TIMING WITH AND WITHOUT ADDRESS LATCH

Figure 4.



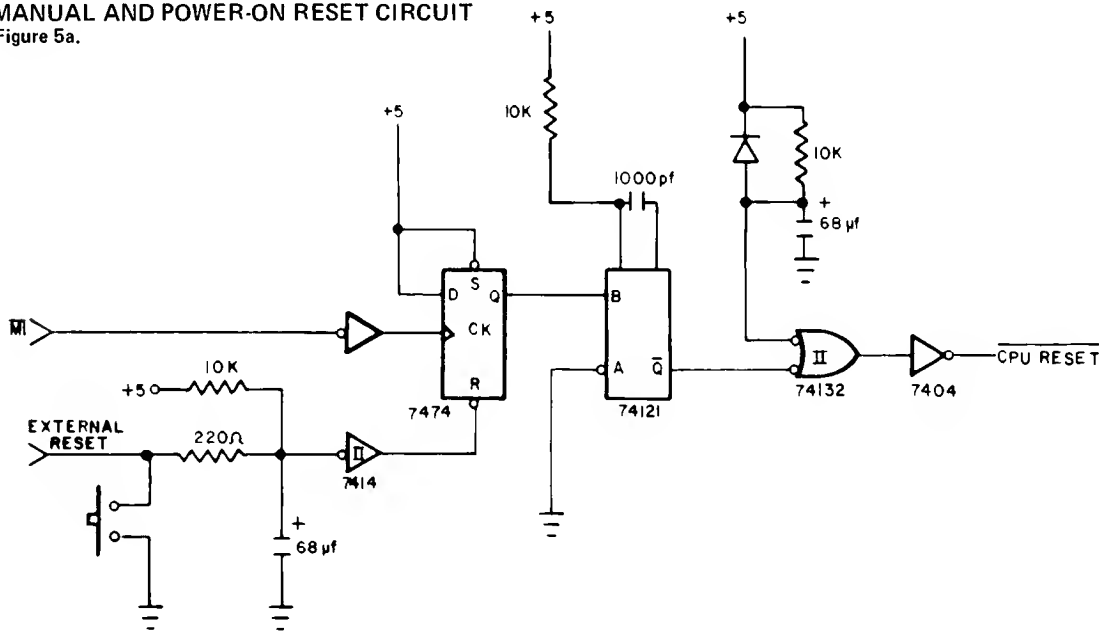
control Signals that one of the conditions that will cause dynamic memory to be destroyed is a reset pulse of duration greater than 1ms. The circuit shown in Figure 5a can be used to generate a short reset pulse from either a push button or an external source. Additionally the manual reset is synchronized to the start of an M1 cycle so that the reset will not fall during the middle of a memory cycle. Along with

the manual reset, the circuit will also generate a power on reset.

If it is not necessary that the contents of the dynamic memory be preserved, then the reset circuit shown in Figure 5b may be used to generate a manual or power on reset.

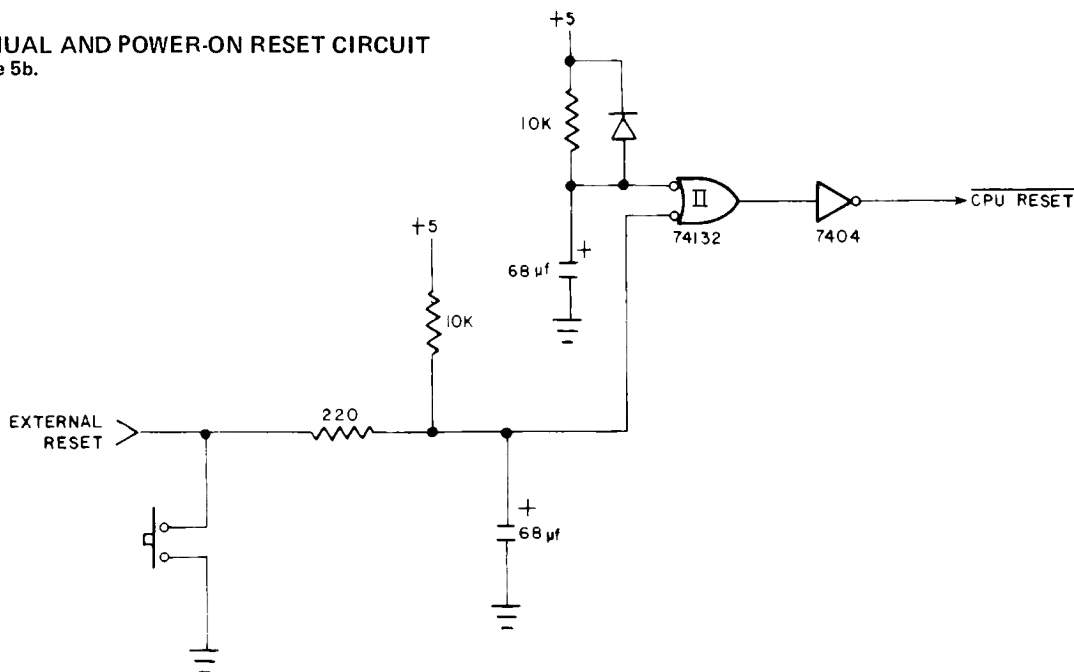
MANUAL AND POWER-ON RESET CIRCUIT

Figure 5a.



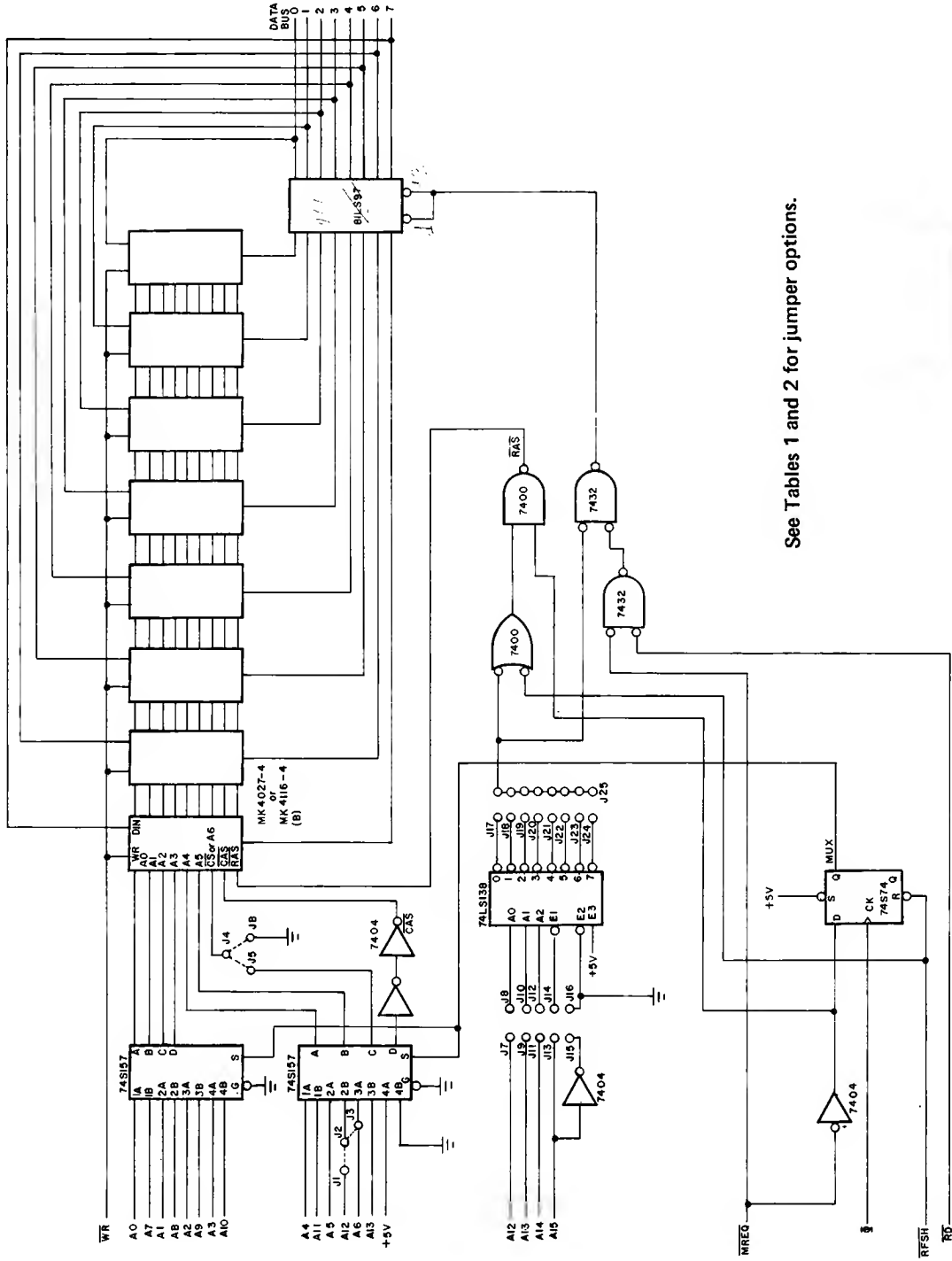
MANUAL AND POWER-ON RESET CIRCUIT

Figure 5b.



DESIGN EXAMPLE NO. 1 SCHEMATIC DIAGRAM

Figure 6.



See Tables 1 and 2 for jumper options.

DYNAMIC
RAMS

DESIGN EXAMPLES FOR INTERFACING THE Z80 TO DYNAMIC MEMORY

To illustrate the interface between the Z80 and dynamic memory, two design examples are presented. Example number 1 is for a 4K/16Kx8 memory and the example number 2 is a 16K/64Kx8 memory.

Design Example Number 1: 4K/16Kx8 Memory

This design example describes a 4K/16Kx8 memory that is best suited for a small single board Z80 based microcomputer system. The memory devices used in the example are the MK4027 (4,096x1 MOS Dynamic RAM) and the MK4116 (16,384x1 MOS Dynamic RAM). A very important feature of this design is the ease in which the memory can be expanded from a 4Kx8 to a 16Kx8 memory. This is made possible by the use of jumper options which configure the memory for either the MK4027 or the MK4116. See Table 1 and 2 for jumper options.

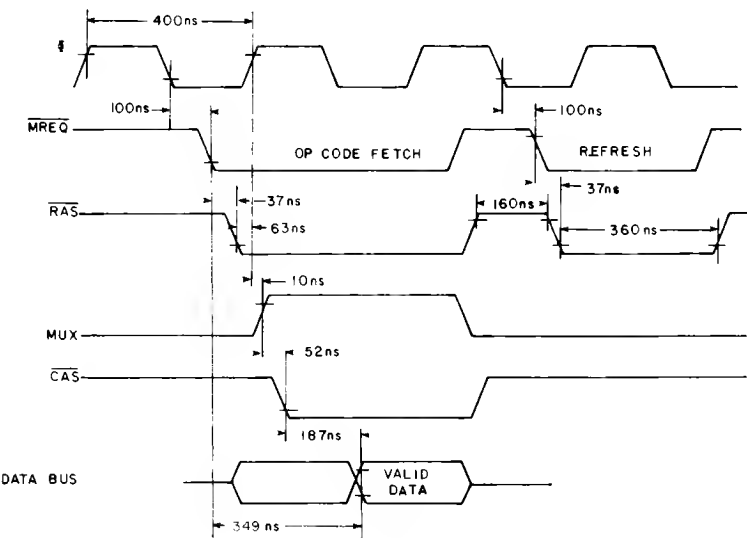
Figure 6 shows the schematic diagram for the 4K/16Kx8 memory. A timing diagram for the Z80 control signals and memory control signals is shown in Figure 7. The operation of the circuit may be described as follows: \overline{RAS} is generated by NANDing \overline{MREQ} with $\overline{RFSH} + \text{ADDRESS DECODE}$. \overline{RFSH} is generated directly from the Z80 while address decode comes from the 74LS138 decoder. Address decode indicates that the address on the bus falls within the memory boundaries of the memory. If an op code fetch or memory read is being executed the 81LS97 output buffer will be enabled at approximately the same time as \overline{RAS} is generated for the memory array. The output buffer is enabled only

during an op code fetch or memory read when $\overline{\text{ADDRESS DECODE}}$, \overline{MREQ} , and \overline{RD} are all low. The switch multiplexer signal (MUX) is generated on the rising edge of Φ after \overline{MREQ} has gone low during an op code fetch, memory read or memory write. After MUX is generated and the address multiplexers switch from the row address to column address, \overline{CAS} will be generated. \overline{CAS} comes from one of the outputs of the multiplexer and is delayed by two gate delays to ensure that the proper column address set-up time will be achieved. Once \overline{RAS} and \overline{CAS} have been generated for the memory array, the memory will then access the desired location for a read or write operation.

7404	22ns	} Generate \overline{RAS} from \overline{MREQ}
7400	15ns	
	63ns	\overline{RAS} to rising edge of Φ
74S74	10ns	Φ to MUX
74S157	15ns	} Generate \overline{CAS} from MUX
7404	22ns	
7404	15ns	
t _{CAC}	165ns	\overline{CAS} access time
81LS97	22ns	Output buffer delay
	349ns	Worst case access

DESIGN EXAMPLE NO. 1 MEMORY TIMING

Figure 7.



The worst case access time required by the CPU for the op code fetch is 450ns (from equation 1); therefore, the circuit exceeds the required access time by 101ns (worst case).

The circuit shown in Figure 6 provides excellent performance when used as a small on board memory. The memory size should be held at eight devices because there is not sufficient timing margin to allow the interface circuit to drive a larger memory array.

Design Example Number 2: 16Kx8 Memory

This design example describes a 16K/64Kx8 memory which is best suited for a Z80 based microcomputer system where a large amount of RAM is desired. The memory devices used in this example are the same as for the first example, the MK4027 and the MK4116. Again as with the first example, the memory may be expanded from a 16Kx8 to a 64Kx8 by reconfiguring jumpers. See Table 3 and 4 for jumper options.

Figure 8 shows the schematic diagram for the 16K/64K memory. A timing diagram is shown in Figure 9. The operation of the circuit can be described as follows: \overline{RAS} is generated by NANDing MREQ with ADDRESS DECODE (from the two 74LS138s) + RFSH. Only one row of RAMs will receive a \overline{RAS} during an op code fetch, memory read or memory write. However, a \overline{RAS} will be generated for all rows within the array during a refresh cycle. \overline{MREQ} is inverted and fed into a TTL compatible delay line to generate MUX and \overline{CAS} . (This particular approach differs from the method used in example number 1 in that all memory timing is referenced to MREQ, whereas the circuit in example number 1 bases its

memory timing from both \overline{MREQ} and the clock. Both methods offer good results, however, the TTL delay line approach offers the best control over the memory timing.) MUX is generated 65ns later and is used to switch the 74157 multiplexers from the row to the column address. The 65ns delay was chosen to allow adequate margin for the row address hold time t_{RAH} . At 110ns, \overline{CAS} is generated from the delay line and NANDed with RFSH, which inhibits a \overline{CAS} during refresh cycle. After \overline{CAS} is applied to the memory, the desired location is then accessed. A worst case access timing analysis for the circuit shown in Figure 8 can be computed as follows:

74LS14	22ns	}	Generate \overline{RAS} from \overline{MREQ}
74LS00	15ns		
delay line	50ns	}	MUX from \overline{RAS}
delay line	45ns		
7400	20ns	}	\overline{CAS} delay from MUX
t_{CAC}	165ns		
8833	30ns		Access time from \overline{CAS}
			Output buffer delay
	347ns		

The required access time from the CPU is 450ns (from equation 1). This leaves 103ns of margin for additional CPU buffers on the control and address lines. This particular circuit offers excellent results for an application which requires a large amount of RAM memory. As mentioned earlier, the memory timing used in this example offers the best control over the memory timing and would be ideally suited for an application which required direct memory access (DMA).

DYNAMIC RAMS

4K x 8 CONFIGURATION(MK4027) JUMPER

Table 1

CONNECT: J13 to J14		Connect: J2 to J3		CONNECT: J14 to J15	
ADDRESS	CONNECT	J4 to J6		ADDRESS	CONNECT
0000-0FFF	J17 to J25	J7 to J8		8000-8FFF	J17 to J25
1000-1FFF	J18 to J25	J9 to J10		9000-9FFF	J18 to J25
2000-2FFF	J19 to J25	J11 to J12		A000-AFFF	J19 to J25
3000-3FFF	J20 to J25			B000-BFFF	J20 to J25
4000-4FFF	J21 to J25			C000-CFFF	J21 to J25
5000-5FFF	J22 to J25			D000-DFFF	J22 to J25
6000-6FFF	J23 to J25			E000-EFFF	J23 to J25
7000-7FFF	J24 to J25			F000-FFFF	J24 to J25

16K x 8 CONFIGURATION (MK4116) JUMPER CONNECTIONS

Table 2

CONNECT:	J1 to J2	ADDRESS	CONNECT
	J4 to J5		
	J8 to J11	0-3FFF	J17 to J25
	J10 to J13	4000-7FFF	J18 to J25
	J12 to J16	8000-BFFF	J19 to J25
	J14 to J16	C000-FFFF	J20 to J25

16K x 8 CONFIGURATION (MK4027)

Table 3

CONNECT: J1 to J3
J5 to J6
J7 to J8
J9 to J10
J11 to J12
J13 to J14

ADDRESS: 0-3FFF	ADDRESS: 4000-7FFF	ADDRESS: 8000-BFFF	ADDRESS: C000-FFFF
CONNECT: J24 to J25	CONNECT: J16 to J17	CONNECT: J40 to J41	CONNECT: J32 to J33
J26 to J27	J18 to J19	J42 to J43	J34 to J35
J28 to J29	J20 to J21	J44 to J43	J36 to J37
J30 to J31	J22 to J23	J46 to J47	J38 to J39

64K x 8 CONFIGURATION(MK4116)

Table 4

CONNECT: J1 to J2	ADDRESS: 0-FFFF
J4 to J5	CONNECT: J32 to J33
J8 to J11	J34 to J35
J10 to J13	J36 to J37
J12 to J15	J38 to J39
J14 to J15	

SYSTEM PERFORMANCE CHARACTERISTICS

Table 5

The system characteristics for the preceeding design examples are shown in Table 5.

EXAMPLE #	MEMORY CAPACITY	MEMORY ACCESS	POWER REQUIREMENTS
1	4K/16Kx8	349ns max.	+12V @ 0.0250 A max. +5V @ 0.422 A max. * -5V @ 0.030 A max.
2	16K/64Kx8	347ns max.	+12V @ 0.600 A max. +5V @ 0.550 A max. * -5V @ 0.030 A max.

*All power requirements are max.; operating temperature 0°C to 70°C ambient, max +12V current computed with Z80 executing continuous op code fetch cycles from RAM at 1.6 μ s intervals.

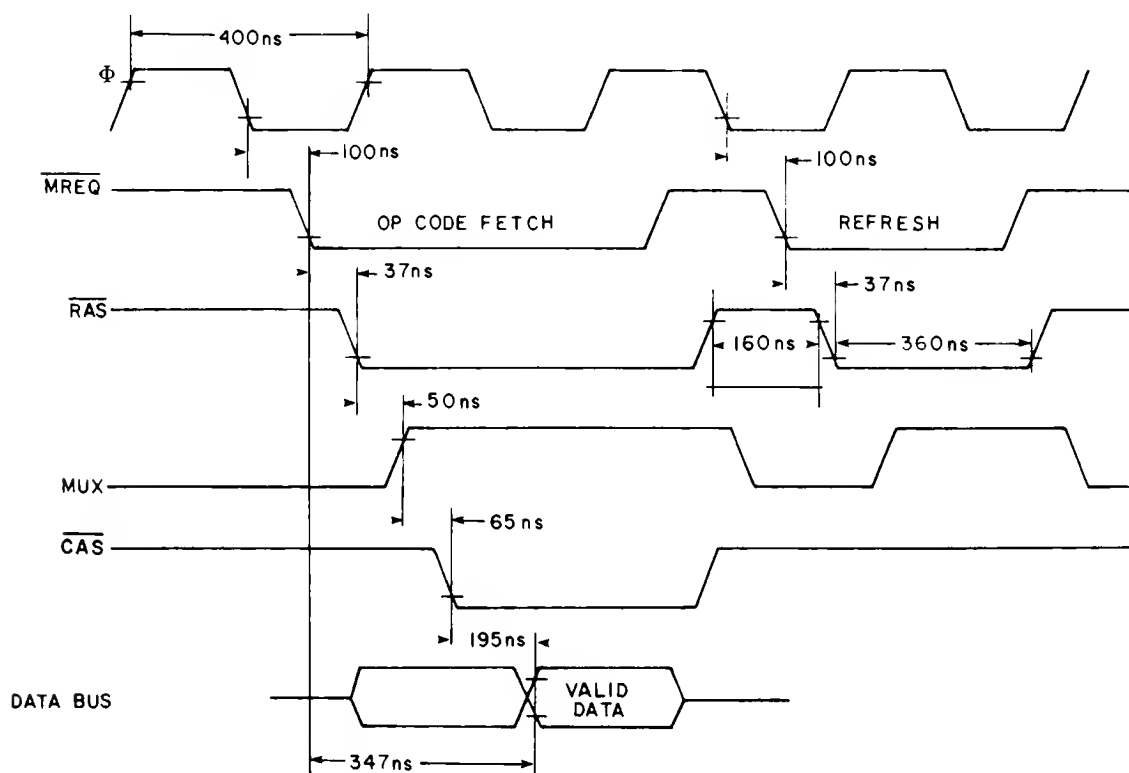
Figure 8.



X-49

DESIGN EXAMPLE NO. 2 MEMORY TIMING

Figure 9.



PRINTED CIRCUIT LAYOUT

One of the most important parts of a dynamic memory design is the printed circuit layout. Figure 10 illustrates a recommended layout for 32 devices. A very important factor in the P.C. layout is the power distribution. Proper power distribution on the V_{DD} and V_{BB} supply lines is necessary because of the transient current characteristics which dynamic memories exhibit. To achieve proper power distribution, V_{DD} , V_{BB} , V_{CC} and ground should be laid out in a grid to help minimize the power distribution impedance. Along with good power distribution, adequate capacitive bypassing for each device in the memory array is necessary. In addition to the individual by-passing capacitors, it is recommended that each supply (V_{BB} , V_{CC} and V_{DD}) be bypassed with an electrolytic capacitor 20 μ F.

By using good power distribution techniques and using the recommended number of bypassing capacitors, the designer can minimize the amount of noise in the memory array. Other layout considerations

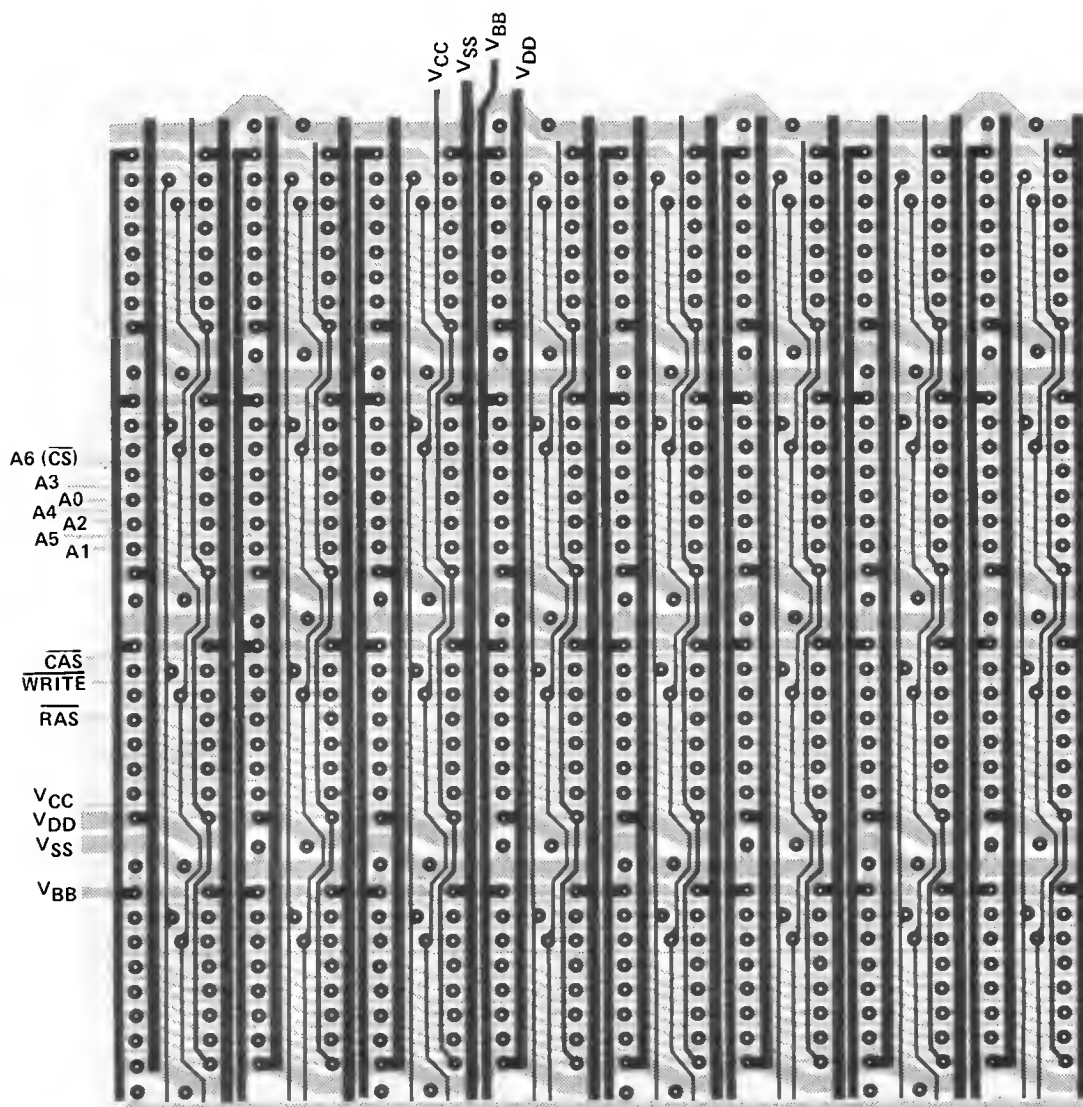
are the placement of signal lines. Lines such as address, chip select, column address strobe, and write should be bussed together as rows; then, bus all rows together at one end of the array. Interconnection between rows should be avoided. Row address strobe lines should be bussed together as a row, then connected to the appropriate \overline{RAS} driver. TTL drivers for the memory array signals should be located as close as possible to the array to help minimize signal noise.

For a large memory array such as the one shown in design example number 2, series terminating resistors should be used to minimize the amount of negative undershoot. These resistors should be used on the address lines, \overline{CAS} and \overline{WRITE} , and have values between 20 Ω to a 33 Ω .

The layout for a 32 device array can be put in a 5" x 5" area on a two sided printed circuit board.

SUGGESTED P. C. LAYOUT FOR MK4027 or MK4116

Figure 10.



DYNAMIC
RAMS

4MHz Z80 DYNAMIC MEMORY INTERFACE CONSIDERATIONS

A 4MHz Z80 is available for the microcomputer designer who needs higher system throughput. Considerations which must be faced by the designer when interfacing the 4MHz Z80 to dynamic memory are the need for memories with faster access times and for providing minimum RAM precharge time. The access times required for dynamic memory interfaced to a 4MHz Z80 can be computed from equations 1 and 2 under Z80 Timing and Memory Control Signals.

Access time for op code fetch for 4MHz Z80,
 let: $t_C = 250\text{ns}$; $t_{DL\overline{\Phi}(MR)} = 75\text{ns}$; $t_{S\overline{\Phi}(D)} = 35\text{ns}$
 then: $t_{\text{ACCESS OP CODE}} = 265\text{ns}$
 Access time for memory read for 4MHz Z80,
 let: $t_C = 250\text{ns}$; $t_{DL\overline{\Phi}(MR)} = 75\text{ns}$; $t_{S\overline{\Phi}(D)} = 50\text{ns}$
 then: $t_{\text{ACCESS MEMORY READ}} = 375\text{ns}$

The problem of faster access times can be solved by using 200ns memories such as the MK4027-3 or MK4116-3. Depending on the number of buffer delays in the system, the designer may have to use 150ns memories such as the MK4027-2 or MK4116-2. The most critical problem that exists when interfacing dynamic memory to the 4MHz Z80 is the RAM precharge time (trp). This parameter is called $t_W(MRH)$ on the Z80 and can be computed by the following equation.

$$(4) \quad t_W(MRH) = t_W(\Phi H) + t_f \cdot 20\text{ns}$$

let: $t_W(\Phi H) = 110\text{ns}$; $t_f = 5\text{ns}$
 then: $t_W(MRH) = 95\text{ns}$

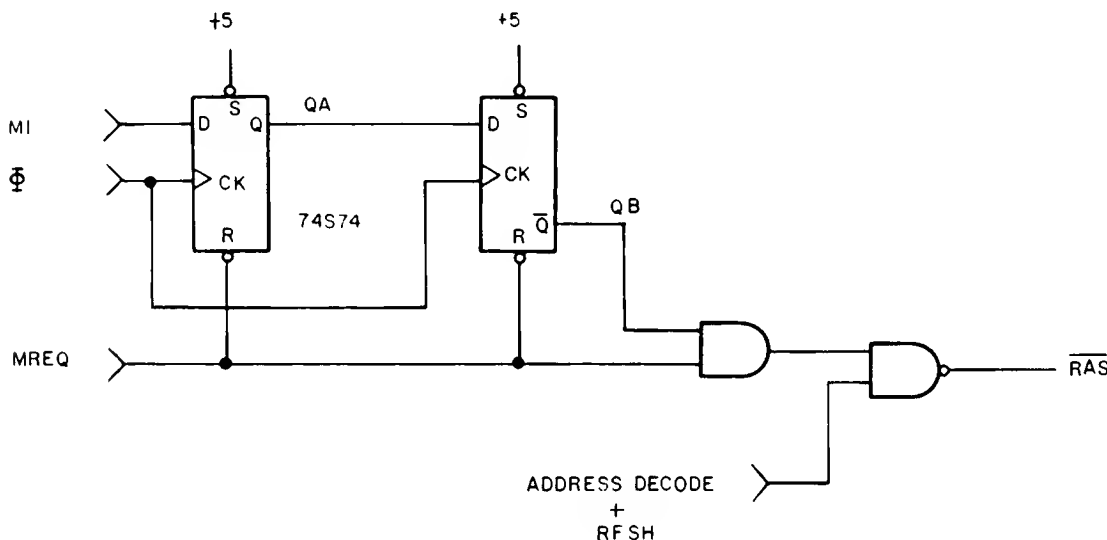
A $t_W(MRH)$ of 95ns will not meet the minimum precharge time of the MK4027-2 or MK4116-2 which is 100ns. The MK4027-3 and MK4116-3 require a 120ns precharge. Figure 11 shows a circuit that will lengthen the $t_W(MRH)$ pulse from 95ns to a minimum of 126ns while only inserting one gate delay into the access timing chain. Figure 12 shows the timing for the circuit of Figure 11. The operation of the circuit in Figure 11 can be explained as follows: The D flip flops are held in a reset condition until MREQ goes to its active state. After MREQ goes active, on the next positive clock edge, the D input of U1 and U2 will be transferred to the outputs of the flip flops. Output QA will go high if M1 was high when Φ clocked U1. Output QB will go low on the next positive going clock edge, which will cause the output of U3 to go low and force the output of U4, which is $\overline{\text{RAS}}$, high. The flip flops will be reset when MREQ goes inactive.

The circuit shown in Figure 11 will give a minimum of 126ns precharge for dynamic memories, with the Z80 operating at 4MHz. The 126ns $t_W(MRH)$ is computed as follows.

110ns	$t_W(\Phi H)$ - clock pulse width high (min)
5ns	t_f - clock full time (min)
20ns	$t_{DL\overline{\Phi}(MR)}$ - MREQ delay (min)
-9ns	74S74 delay (min)
<hr/>	
126ns	$t_W(MRH)$ modified (min)

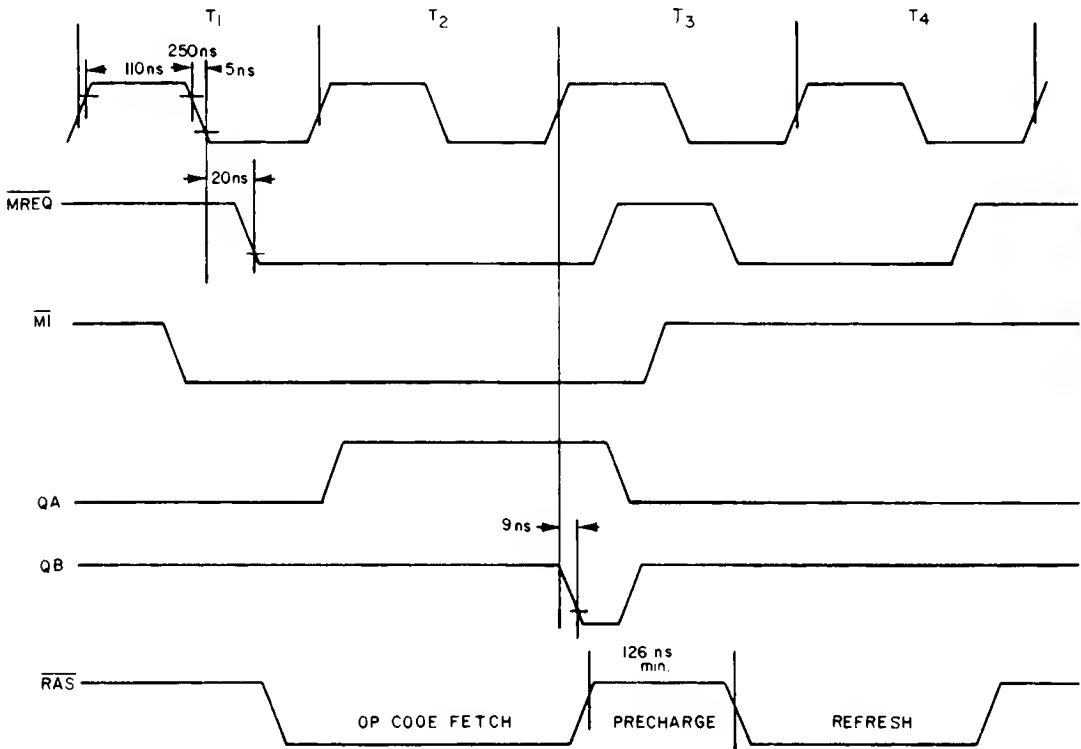
4MHz Z80 PRECHARGE EXTENDER FOR DYNAMIC MEMORIES

Figure 11



TIMING DIAGRAM FOR 4MHz Z80 PRECHARGE EXTENDER

Figure 12



DYNAMIC RAMS

APPENDIX

MEMORY TEST ROUTINE

This section is intended to give the microcomputer designer a memory diagnostic suitable for testing memory systems such as the ones shown in Section VI.

The routine is a modified address storage test with an incrementing pattern. A complete test requires 256₁₀

passes, which will execute in less than 4 minutes for a 16Kx8 memory. If an error occurs, the program will store the pattern in location '2C'H and the address of the error at locations '2D'H and '2E'H.

The program is set up to test memory starting at location '2F'H up to the end of the block of memory defined by the bytes located at '0C'H and '0D'H. The test may be set up to start at any location by modifying locations '03'H - '04'H and '11'H - '12'H with the starting address that is desired.

			MYRTS LISTING	PAGE	0001
LOC	OBJ CODE	STMT	SOURCE STATEMENT		
		0001	;TRANSLATED FROM DEC 1976 INTERFACE MAGAZINE		
		0002	;		
		0003	;THIS IS A MODIFIED ADDRESS STORAGE TEST WITH AN		
		0004	;INCREMENTING PATTERN		
		0005	;		
		0006	;256 PASSES MUST BE EXECUTED BEFORE THE MEMCRY IS		
		0007	;COMPLETELY TESTED.		
		0008	;		
		0009	;IF AN ERROR OCCURS, THE PATTERN WILL BE STORED		
		0010	;AT LOCATION '002C'H AND THE ADDRESS OF THE		
		0011	;ERROR LOCATION WILL BE STORED AT '002D'H AND		
		0012	;'002E'H.		
		0013	;		

MEMORY TEST ROUTINE (Cont'd.)

```

0014 ;THE CONTENTS OF LOCATIONS '000C'H AND '001D'H
0015 ;SHOULD BE SELECTED ACCORDING TO THE FOLLOWING
0016 ;MEMORY SIZE TO BE TESTED
0017 ;
0018 ;TOP OF MEMORY TO
0019 ;BE TESTED                                VALUE OF EPAGE
0020 ;
0021 ;      4K                                '10'H
0022 ;      8K                                '20'H
0023 ;     16K                                '40'H
0024 ;     32K                                '80'H
0025 ;     48K                                'C0'H
0026 ;     64K                                'FF'H
0027 ;
0028 ;THE PROGRAM IS SET UP TO START TESTING AT
0029 ;LOCATION '002F'H. THE STARTING ADDRESS FOR THE
0030 ;TEST CAN BE MODIFIED BY CHANGING LOCATIONS
0031 ;'0003-0004'H AND '0011-0012'H.
0032 ;
0033 ;TEST TIME FOR A 16K X 8 MEMORY IS APPROX. 4 MIN
0034 ;
0000      0000      0035      ORG      0000H
0000      0600      0036      LD      B,0      ;CLEAR B PATRN MODIFIER
0002      212F00      0037 ;LOAD UP MEMORY
0005      7D          0038 LOOP:   LD      HL,START ;GET STARTING ADDR
0006      AC          0039 FILL:  LD      A,L      ;LOW BYTE TO ACCM
0007      A8          0040      XOR      H      ;XOR WITH HIGH BYTE
0008      77          0041      XOR      B      ;XOR WITH PATTERN
0009      23          0042      LD      (HL),A    ;STORE IN ADDR
000A      7C          0043      INC      HL      ;INCREMENT ADDR
000B      FE10       0044      LD      A,H      ;LOAD HIGH BYTE OF ADDR
000D      C20500     0045      CP      EPAGE    ;COMPARE WITH STOP ADDR
0010      212F00     0046      JP      NZ,FILL   ;NOT DONE,GO BACK
0013      7D          0047 ;READ AND CHECK TEST DATE
0014      AC          0048      LD      HL,START ;GET STARTING ADDR
0015      A8          0049 TEST:   LD      A,L      ;LOAD LOW BYTE
0016      BE          0050      XOR      H      ;XOR WITH HIGH BYTE
0017      C22500     0051      XOR      B      ;XOR WITH MODIFIER
001A      23          0052      CP      (HL)     ;COMPARE WITH MEMORY LOC
001B      7C          0053      JP      NZ,EXIT   ;ERROR EXIT
001C      FE10       0054      INC      HL      ;UPDATE MEMORY ADDRESS
001E      C21300     0055      LD      A,H      ;LOAD HIGH BYTE
0021      04          0056      CP      EPAGE    ;COMPARE WITH STOP ADDR
0022      C30200     0057      JP      NZ,TEST   ;LOOP BACK
0025      222D00     0058      INC      B      ;UPDATE MODIFIER
0028      322C00     0059      JP      LOOP      ;RST WITH NEW MODIFIER
002B      76          0060 ;ERROR EXIT
002C      002C       0061 EXIT:   LD      (BYTE),HL ;SAVE ERROR ADDRESS
002D      002D       0062      LD      (PATRN),A ;SAVE BAD PATTERN
002F      2F00       0063      HALT          ;FLAG OPERATOR
0030      0030       0064 PATRN:  DEFS      1
0031      0031       0065 BYTE:   DEFS      2
0032      0032       0066 START:  DEFW      S
0033      0033       0068 EPAGE:  EQU      10H      ;SET UP FOR 4K TEST
0034      0034       0069      END

```

LOC	OBJ CODE	STMT	SOURCE STATEMENT	MXRTS LISTING	PAGE	0002
0022	C30200	0059	JP	LOOP		
		0060	ERROR EXIT			
0025	222D00	0061	EXIT: LD	(BYTE),HL		
0028	322C00	0062	LD	(PATRN),A		
002B	76	0063	HALT			
002C		0064	PATRN: DEFS	1		
002D		0065	BYTE: DEFS	2		
002F	2F00	0066	START: DEFW	S		
		0068	EPAGE: EQU	10H		
		0069	END			

Today several semiconductor manufacturers are moving 16384 bit dynamic MOS memories into volume production. The circuit will be the most cost-effective method of providing medium performance, large capacity randomly accessible data storage over the next several years and will in all likelihood be shipped in larger volume to more users than has any previous memory chip. This burgeoning market will confront many engineers with the problems of performing comparative evaluations, writing incoming device tests, system and diagnostic tests, and field troubleshooting and repair of memory systems containing many 16K chips. A thorough understanding of the device permits the engineer to evaluate the adequacy of manufacturers' outgoing screens and, if necessary, to institute efficient incoming tests which comprehend the differences or shortcomings in the individual designs or outgoing test procedures.

Since the 16K has established the state-of-the-art in MOS design and processing at this point in time, the test sequences utilized must be carefully considered to keep test times to a reasonable minimum while at the same time adequately screening out marginal devices. The testing considerations themselves are applicable to earlier 1K and 4K circuits as well; the penalties for inadequacy are greater.

A brief description of manufacturing test procedures which relate ultimately to the quality and reliability of the memory chip would include characterization tests, in which the processing constraints and operating limits of a specific design are determined; reliability tests, which subject production lots to abnormal stresses in order to convert latent defects into failures prior to the final test; and the final test itself in which the manufacturer must always tread a thin line between test throughput (minimum test cost per device) and thoroughness. The quality of these tests varies from manufacturer to manufacturer and is manifested in the quality of their shipped product. Good design and quality processing are not enough, alone, to guarantee reliability; they must always be augmented by adequate testing.

BASIC CONSIDERATIONS

The storage element in all 16K RAMs is an MOS capacitor with data transfer and isolation controlled by a single transistor. This is the well known single

transistor (1T) cell, used for the first time in the 4K memory devices which have been available for several years. The small size of the cell (about 0.7 mil² when fabricated in the double level polysilicon process) is sufficient inducement that the disadvantages are tolerated by the designer. Read-out is destructive, requiring an internal restore operation after each read. Available signal levels are dictated by the ratio of cell to digit line capacitance and are on the order of one to two hundred millivolts. Charge storage is of course dynamic in nature, since the charge stored on the capacitor will eventually leak off.

Storage time is an intrinsic device parameter; refresh time (more properly refresh interval) is a timing parameter which specifies the maximum allowable interval separating two operations on the same storage location which will re-establish the full charge on a partially-decayed high level.

The storage time of any dynamic MOS RAM may be expressed by the empirical equation

$$t_{\text{STORAGE}} = A \exp(-BT)$$

where

T is junction temperature in °C

B is a variable relating the magnitude of the generation-recombination current to the junction temperature (units of 1/°C)

and

A is a scaling constant reflecting such variables as junction area, bulk defect density, and sense amplifier design.

Note that the term "B" in the equation is not a constant. Conventionally it is assumed that the storage time doubles for every 10 °C decrease in junction temperature, which is equivalent to assuming that B = 0.069. Data shows that a typical value for B is 0.055, but that it does in fact vary at least 30% from this typical value. This equation is graphed in Figure 1 for several different values of B, arbitrarily assuming a minimum storage time of 2 milliseconds at T_J = 100 °C. The storage time at T_J = 25 °C for this hypothetical device will lie somewhere between 50 milliseconds and 381 milliseconds. If room temperature testing is to be attempted, the refresh interval would have to be set at 381 milliseconds, since any lesser value would not guarantee 2 milliseconds at 100 °C. The devices which failed such a test would

not necessarily be failures at 2 ms, 100°C, and would therefore have to be rescreened at the 100°C temperature. The efficiency of this procedure depends upon the number of good devices found by the first screen, but in general the number of units requiring a second test is so great that the first screen may as well be eliminated in favor of a 100% screen at the maximum junction temperature.

Storage time is of course not the only parameter of interest. Other parameters which need to be verified over the temperature range include access time, power dissipation, and input/output levels. Access time and power dissipation are functions of transistor gain. Gain is temperature dependent through carrier mobility and is about 25% lower at 100°C than at 0°C. Access time is therefore worst-case at elevated temperatures. The memory will dissipate more power at low temperature, although much of the power required is capacitive and therefore frequency rather than temperature related. Signal levels are functions of transistor threshold voltage, which decreases about two millivolts for every 1°C increase in temperature. Input high levels and output high and low levels are normally worst-case at low temperature and must be guardbanded if tested only at high temperature. (One 16K RAM, the MOSTEK MK 4116, utilizes an integrated reference voltage for address and data inputs which removes the threshold voltage dependence and therefore the temperature dependence of these inputs.) As will be discussed later, a few timing parameters become worst-case as the memory becomes faster, and need to be guardbanded if testing only at high temperature. On balance, however, due primarily to the extreme variation of storage time with temperature, it is most practical to conduct tests at the maximum junction temperature only and guardband non-worst-case parameters.

The two junction temperatures singled out in Figure 1 were not chosen at random. The equation describing temperature rise over an ambient is

$$T_J - T_A = \Delta T = \theta_{JA} P_D$$

where

θ_{JA} is the junction to ambient thermal resistance (for 16 pin ceramic DIP mounted in a socket on a double-sided PC board, the most widely accepted value is 70°C/watt)

and

P_D is the power dissipation of the device under the conditions of interest.

To calculate ΔT , assume the following specified values:

$$\begin{aligned} I_{DD} \text{ (ACTIVE)} &= 35 \text{ MA} \\ I_{DD} \text{ (STANDBY)} &= 1.5 \text{ MA} \\ V_{DD} \text{ (MAXIMUM)} &= 13.2 \text{ V} \\ t_{\text{cycle}} &= 375 \text{ ns} \end{aligned}$$

and assume that the refresh test is conducted by writing 16384 bits at the 375 ns cycle rate, pausing in the standby condition for the refresh interval, then reading all bits again at 375 ns. The rise in junction temperature can now be calculated:

$$\begin{aligned} t_{\text{REFRESH}} &= 2\text{ms}; \text{ duty factor (DF)} = \\ &= \frac{2(16384)375\text{ns}}{2(16384)375\text{ns} + 2\text{ms}} = 0.86 \end{aligned}$$

$$\begin{aligned} \Delta T &= \theta_{JA} (P_D \text{ ACTIVE (DF)} + P_D \text{ STANDBY} \\ &\quad (1 - \text{DF})) \\ &= 70^\circ\text{C/W} (0.035 (13.2) 0.86 + 0.0015 \\ &\quad (1 - 0.86)) \\ &= 28^\circ\text{C} \end{aligned}$$

$$\begin{aligned} t_{\text{REFRESH}} &= 381\text{ms}; \text{ duty factor (DF)} = \\ &= \frac{2(16384)375\text{ns}}{2(16384)375\text{ns} + 381\text{ms}} = 0.03 \end{aligned}$$

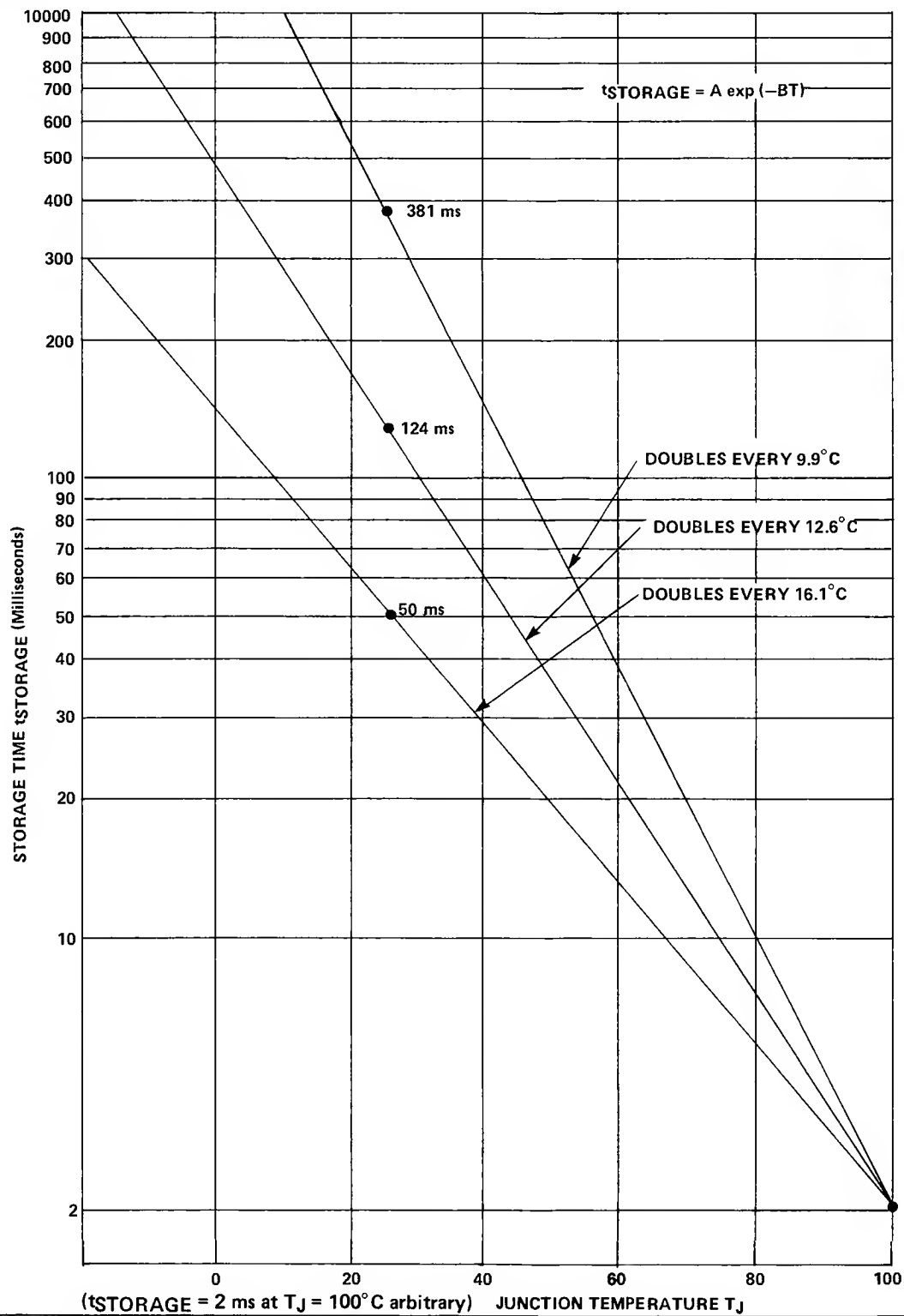
$$\begin{aligned} \Delta T &= 70^\circ\text{C/W} (0.035 (13.2) 0.03 + 0.0015 \\ &\quad (13.2) (1 - 0.03)) \\ &= 2.3^\circ\text{C} \end{aligned}$$

The junction temperature of a device executing a 381 ms refresh test at $T_A = 25^\circ\text{C}$ would rise only 2.3 degrees to 27.3°C, while the same device executing a 2ms refresh test at $T_A = 70^\circ\text{C}$ would have a junction temperature of 98°C.

Strictly speaking, the foregoing calculations are true only if the refresh test in question is run in a continuous mode allowing the junction temperature to stabilize. The thermal mass of the device is not negligible; in fact θ_{JA} is a function of time and has a time constant of approximately 60 seconds in most test situations. Much of the effectiveness of the N2 test patterns can be attributed to higher junction temperatures due simply to the test length. An N2 pattern, with N equal to 16384 and a cycle time of 375ns, requires 100 seconds. The value of θ_{JA} after 100 seconds of testing is about 80% of its final

STORAGE TIME VS JUNCTION TEMPERATURE

Figure 1



DYNAMIC RAMS

value. The junction rise for $P_D = 462$ milliwatts is

$$\Delta T = \theta_{JA} P_D = (0.8) (70^\circ \text{C/W}) (.462) = 26^\circ \text{C}$$

and this rise has occurred during the test. The storage time of the device may be reduced by as much as a factor of 6 and the device speed is approximately 10% less. These benefits can of course be attained without resorting to the use of N^2 patterns by precalculating the final junction temperature and setting the temperature chamber accordingly. This approach is common but not without its pitfalls. If the construction of the test chamber is such that heat is maintained throughout the test, the self-heating must be considered; if the device is held in an elevated ambient prior to the test, then removed and inserted into the test socket, the combined effects of heat loss in the socket and self-heating during the test must be characterized.

An accurate method for measuring junction temperature uses the device itself as a temperature reference. All signal inputs connect to pn^+ diodes which may be calibrated by utilizing the fact that if diode current is held constant, diode voltage is linearly proportional to temperature. Calibrate an input on a reference device by stabilizing the device at an accurately measured reference temperature, injecting a constant current, and measuring the diode drop (from the input to the V_{BB} pin). When this has been performed at several temperatures a calibration curve of diode voltage versus temperature may be constructed and the device used to measure unknown temperatures by injecting current, measuring the diode voltage, and referring to the calibration chart. The procedure requires care, but once calibrated the device is capable of profiling heat loss at the test site or junction temperature rise during operation with great accuracy. Several hints: a good value for the current is $100 \mu\text{A}$; the voltage measurement requires millivolt accuracy; the measurement cannot be made while the device is operating because of noise in the substrate (operate the device, then switch out the functional inputs and switch in the measurement circuitry). Each device must be calibrated separately since the magnitude and slope of the relationship varies.

RELIABILITY TESTING

Although the user may not resort to reliability screening himself, relying solely on the manufacturer to choose appropriate tests and apply them wisely, he should be familiar with the basic failure mechanisms

and methods employed to screen them out prior to shipment.

Published data on 4K and 16K silicon gate MOS memories (1)(2) indicate that two failure mechanisms account for between 50% and 85% of all reported RAM failures. These two mechanisms, oxide defects and defects caused by foreign contamination, vary in the type of screen required for elimination.

Oxide defects are imperfections in the SiO_2 gate oxide introduced during the manufacturing process which can rupture when subjected to an electrical field for some period of time. This failure mode may be screened by subjecting all devices to an overvoltage stress; the effectiveness of the screen is directly dependent upon the field intensity, hence the voltage applied, and to a lesser degree on time. One screen employed by several manufacturers subjects the RAM to an operational test in which the magnitude of the supply voltages is increased by approximately 50% over nominal. This may occur in the testing prior to burn-in, at the burn-in itself, or in the final test prior to shipment. If the overstress occurs at the burn-in itself it may last for 12 to 24 hours, while an overstress during a functional test sequence normally would last less than one second. A commonly-accepted rule of thumb is that the effectiveness of the oxide defect screen varies with $E\sqrt{t}$. A 24 hour burn-in would, according to this rule, be about 17 times as effective as a one-second test assuming both were run at the same voltage, however, increasing the voltage (field strength E) by 50% increases the efficiency of the screen by the same 50%. Clearly the overvoltage screen is necessary; it is incumbent upon the manufacturer to perform such a screen himself as it is doubtful he would authorize the user to stress the RAM beyond the data-sheet limits.

The second large category of failures are those caused by contamination of the device by some mobile impurity ion such as sodium. These impurities can move under applied voltage and temperature conditions to some point in the circuit where they can alter the threshold voltage of the MOS transistor. For an N channel 16K memory, the threshold voltages will be lowered if the contaminant is a positive ion and failures can occur either on normal transistors or on spurious field oxide transistors. This failure mode is widely known and reported, and is accelerated by thermal stress. The rate of acceleration is predicated by the equation (3),

$$R = R_0 \exp \left(-\frac{E_A}{KT_k} \right)$$

where

R is reaction rate

R_0 is a constant

E_A is activation energy in electron volts (eV)

K is Boltzmann's constant (8.63×10^{-5} eV/oK)

T_k is temperature in degrees Kelvin (oK).

The activation energy for contamination-related failures is approximately 1.0 eV, and therefore such failures are subject to removal by high-temperature burn-in, and most manufacturers perform an operating burn-in at 125°C for some number of hours (normally 12 - 24 hours) to reduce the incidence of field failures. On the other hand, the acceleration rate for gate oxide failures is reported to be between 0.1 - .05 eV and the high-temperature screen would be marginally effective for gate oxide defects.

At least one manufacturer has combined the overvoltage and high temperature screens and is currently subjecting all 16K RAM's to a 24 hour burn-in at 125°C with the device power supplies at 50% overvoltage (+18 v, -7 v). Here again, such testing is properly done by the manufacturer, but the user should satisfy himself as to the adequacy of the reliability screens performed by the various manufacturers.

Reliability can be greatly impacted by proper design techniques. As an example, consider the equation given for thermal acceleration of failures. Rewriting the equation to allow a comparison of reaction rates at two different temperatures T_{k1} and T_{k2} , we have:

$$\frac{R_1}{R_2} = \exp \left(-\frac{E_A}{K} \left(\frac{T_{k2} - T_{k1}}{T_{k1} T_{k2}} \right) \right).$$

Now the effect of power dissipation upon reliability can be evaluated. For two 16K RAMS, one dissipating 900 milliwatts and one dissipating 450 milliwatts while operating at $T_A = 70^\circ\text{C}$,

$$T_{J1} = 70^\circ\text{C} + (70^\circ\text{C/W}) (0.900 \text{ W}) = 133^\circ\text{C}$$

$$T_{J2} = 70^\circ\text{C} + (70^\circ\text{C/W}) (0.450 \text{ W}) = 101.5^\circ\text{C}$$

and assuming that $E_A = 1$ eV,

$$\frac{R_1}{R_2} = \exp \left(-\frac{1}{8.63 \times 10^{-5}} \left(\frac{133 - 101.5}{(133+273)(101.5+273)} \right) \right)$$

$$\frac{R_1}{R_2} = 0.097$$

which predicts a failure rate for the 900 milliwatt device of about 11 times that of the 450 milliwatt device, due to the 31.5°C difference in junction temperature.

MULTIPLEXED DEVICES

All 16K devices announced to date have followed the pinout and address multiplexed architecture pioneered by MOSTEK for their 4K RAM in 1973. The reduction in number of address lines from 14 to 7 (for the 16K) is bought at the expense of a more complex cycle with more timing parameters(4).

Some of these parameters must be examined in detail, as a proper understanding of their interrelationship is necessary. The timing diagram of Figure 2 shows the timing parameters necessary for standard write and read operations. The data output signal is shown for both the MOSTEK and Intel designs.

Three clocks, $\overline{\text{RAS}}$ (Row Address Strobe), $\overline{\text{CAS}}$ (Column Address Strobe), and $\overline{\text{WRITE}}$, must be provided along with seven multiplexed address lines and the D_{IN} (data in) if the memory is to execute a write cycle. Most of the testing difficulties arise from the relationship of $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$, from the relationships of the addresses to $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$, and from the relationships of the addresses to $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$, and from $\overline{\text{CAS}}$ to the D_{OUT} (data output).

$\overline{\text{RAS}}$ initiates the cycle by going from the high state to the low state. It must have remained high long enough for internal nodes to be precharged to a known initial state prior to initiation of a new cycle; if the parameter t_{PP} is violated (made too short) internal clocks, address buffers, decoders, and sense amplifiers are not adequately initialized. Once $\overline{\text{RAS}}$ goes low it must remain low long enough (t_{RAS}) for the selection of the accessed cells, sense operation, and restoration of the destroyed data (the 1T cell reads out destructively). When $\overline{\text{RAS}}$ goes low it clocks in the seven row addresses if the row address setup and hold specifications (t_{ASR} and t_{RAH}) have been met. For the Intel design, if $\overline{\text{CAS}}$ is low when $\overline{\text{RAS}}$ goes low, a refresh-only operation is initiated; for the MOSTEK design, $\overline{\text{CAS}}$ may be low at the $\overline{\text{RAS}}$ transition (may in fact stay low for some time after the $\overline{\text{RAS}}$ transition since the parameter t_{CRP} is

negative) without prejudicing the new cycle, which may be either a read or write cycle. The Intel ability to perform a 64 cycle refresh hinges on this timing parameter. If RAS finds $\overline{\text{CAS}}$ low, the most significant row address bit along with all column address bits are ignored. This causes the selection of one row in each 8K half of the array and activation of all 256 sense amplifiers. Refresh may then be performed as though the array were organized as 64 rows by 256 columns. For the MOSTEK part, and for the Intel part if $\overline{\text{RAS}}$ finds $\overline{\text{CAS}}$ high, refresh must be performed on all 128 rows.

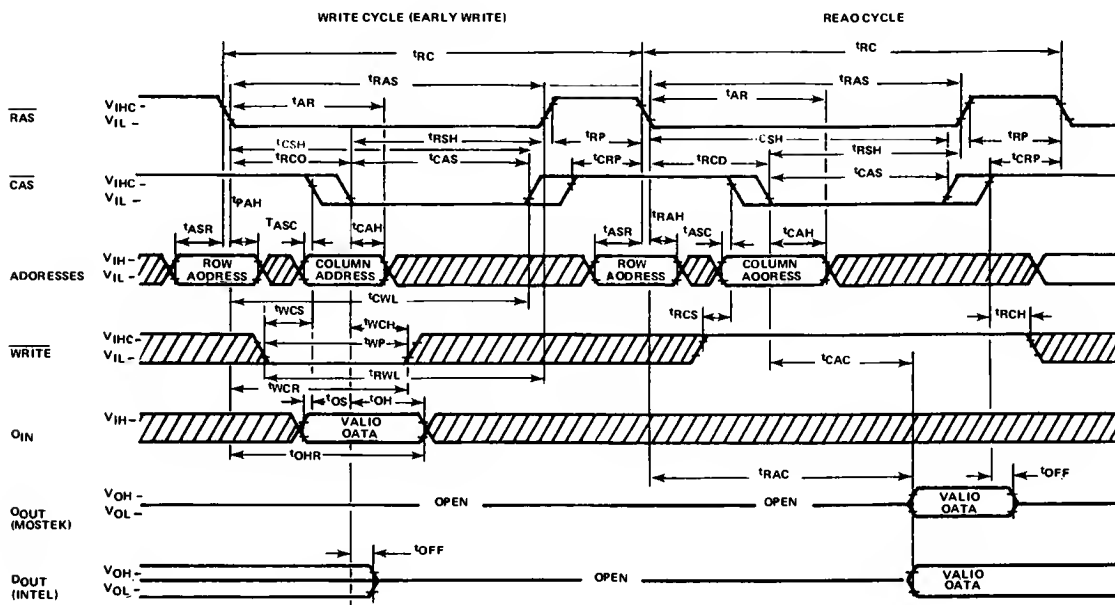
$\overline{\text{CAS}}$ is used to clock the column addresses, select one of the 128 active sense amplifiers and transfer its data to the output in a read or read/write cycle. The high to low transition of $\overline{\text{CAS}}$ latches the column addresses if the column address setup and hold specifications (t_{ASC} and t_{CAH}) have been met. To prevent the $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ timing from intruding into the access time specification, 16K designs allow $\overline{\text{CAS}}$ to go active as soon as the row address hold time has been met and the column address is established on the address inputs. In fact, a negative specification on the column address setup allows switching $\overline{\text{CAS}}$ low even during the multiplex time. This negative specification becomes harder to meet as the part becomes faster (higher V_{DD} , lower

temperature) and in any event is one of the more trying parameters to test, since the slowest of the seven address signals (with respect to $\overline{\text{CAS}}$) determines the actual value of t_{ASC} . Even though $\overline{\text{CAS}}$ can go negative at t_{RAH} , it is not required to do so until somewhat later in the cycle. The latest time for the $\overline{\text{CAS}}$ transition with respect to $\overline{\text{RAS}}$ is given by the parameter $t_{\text{RCD}}(\text{max})$ — note that $t_{\text{RCD}}(\text{min})$ equals the row address hold time t_{RAH} . The parameter $t_{\text{RCD}}(\text{max})$ is actually a pseudo-limitation, since the only effect of exceeding $t_{\text{RCD}}(\text{max})$ is to extend the access time specification (actually the row access) t_{RAC} by the actual value of t_{RCD} minus $t_{\text{RCD}}(\text{max})$.

Manufacturers are willing to live with the limitations posed by the negative value for column address setup time in order to provide a more usable part. The amount of time available to the user to switch his multiplexer without artificially delaying $\overline{\text{CAS}}$ and thereby degrading access time is simply the value of the maximum allowable $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay minus the required row address hold time, minus the required column address setup time (Multiplex time = $t_{\text{RCD}}(\text{max}) - t_{\text{RAH}} - t_{\text{ASC}}$). If t_{ASC} is a negative number it adds to rather than decreases the multiplex time. In order to guarantee this specification, the

TIMING DIAGRAM

Figure 2



KEY PARAMETERS OF CURRENTLY AVAILABLE 16K RAMS

Figure 3

MANUFACTURER	INTEL	MOSTEK
PART NUMBER	2116-2	4116-2
$\overline{\text{RAS}}$ ACCESS	200 ns	150 ns
$\overline{\text{CAS}}$ ACCESS	125 ns	100 ns
MULTIPLEX TIME	40 ns	40 ns
PRECHARGE TIME	75 ns	100 ns
NUMBER OF REFRESH CYCLES	64 or 128	128
NUMBER OF SENSE AMPS	256	128
DIE AREA	33930 mils ²	22330 mils ²
V_{DD} TOLERANCE	$\pm 10\%$	$\pm 10\%$
I_{DD} CURRENT (MAXIMUM)	69 mA	35 mA
POWER DISSIPATION (MAXIMUM)	911 mW	462 mW

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manufacturer must place a minimum access time requirement on his testing — that is, parts which are too fast must be rejected, as they will not meet the negative t_{ASC} specification. It is to be expected that as faster 16K designs become available, this negative parameter will become smaller, or possibly will go to zero.

In addition to clocking the column addresses, $\overline{\text{CAS}}$ controls the state of the data output. The MOSTEK version open-circuits the output with the low to high transition of $\overline{\text{CAS}}$. Intel uses the high to low edge of $\overline{\text{CAS}}$ for the same purpose. This allows compatibility with the earlier 4K designs which also used the high to low edge of $\overline{\text{CAS}}$. The 4K's have, however, an extra chip select input which can be used in conjunction with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ to deselect the output. With the Intel 16K the only way to guarantee a deselected output is to insert an extra cycle which leaves $\overline{\text{RAS}}$ high while clocking $\overline{\text{CAS}}$. MOSTEK overcomes this difficulty by unlatching the output with the rising edge of $\overline{\text{CAS}}$. This makes the output state independent of the previous cycle and eliminates the need for the "CAS-only" deselect cycle. If the MOSTEK part is operated in a minimum cycle with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ going high at the same time, the output is only valid for the deselect time (t_{OFF}) plus the amount that the speed of the actual device exceeds the specified speed (if any). To overcome this difficulty, MOSTEK allows the user to leave $\overline{\text{CAS}}$ low while $\overline{\text{RAS}}$ goes into precharge, thereby

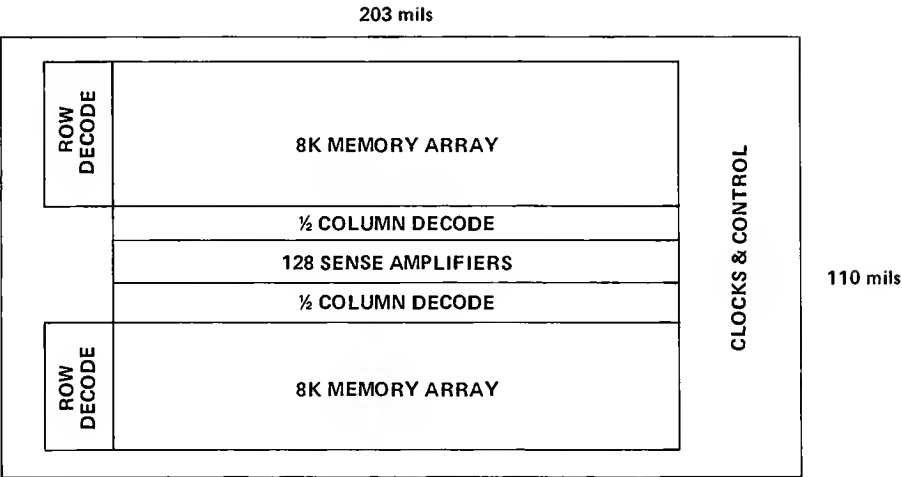
prolonging the output and, incidentally, adding the second major timing difference, that of the state of $\overline{\text{CAS}}$ when $\overline{\text{RAS}}$ goes low, which was discussed earlier.

CHIP ARCHITECTURE AND CELL LAYOUT

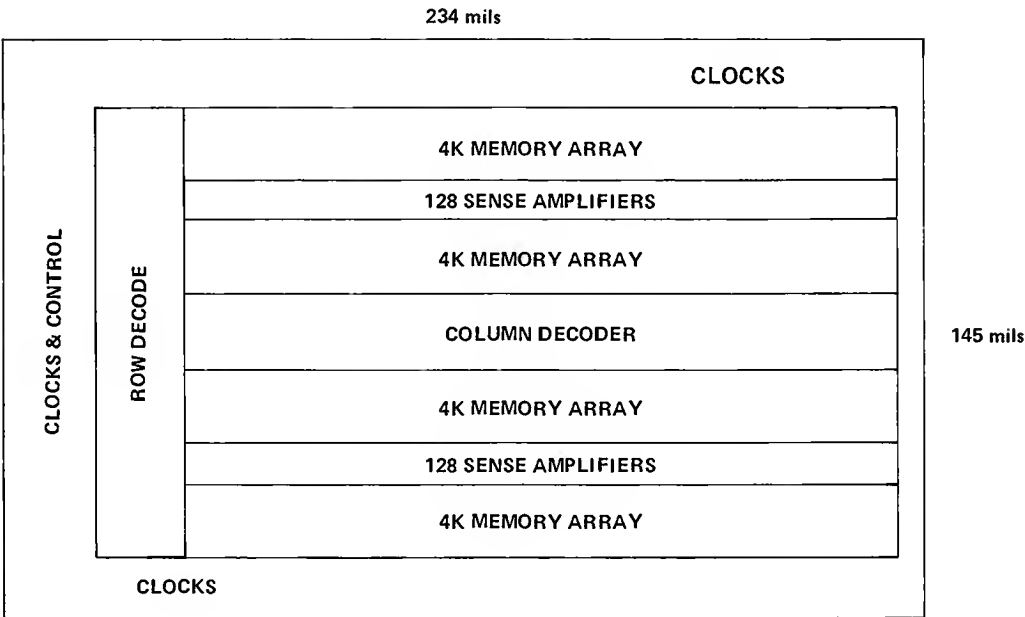
The architecture of the chip can have a direct bearing on the types of tests which should be conducted, as can the layout of the storage cell. Precise details are difficult to acquire as most manufacturers consider them proprietary. Interest in the 16K has prompted the generation of several articles and papers which give some details useful in testing considerations(5)(6)(7). Figure 4 gives a gross overview of two chip architectures which nevertheless provide some useful information.

The most obvious difference is in the division of the 16K array into two 8K halves serviced from the middle by 128 sense amplifiers (MOSTEK MK 4116), or into four 4K quadrants, each pair serviced by 128 sense amplifiers (for a total of 256) from their respective centers (Intel 2116). All other factors being equal, in particular assuming approximately equal cell capacitances (reported by MOSTEK and Intel as 0.04 pF and 0.03 pF, respectively), the extra subdivision on the Intel chip means that the digit lines are only half as long as in the MOSTEK chip

TWO 16K RAM CHIP ARCHITECTURES
 Figure 4



MOSTEK MK 4116



INTEL 2116

PROCESS COMPARISON

Figure 5

SINGLE LEVEL POLYSILICON GATE PROCESS FLOW	DOUBLE-LEVEL POLYSILICON GATE PROCESS FLOW
INITIAL OXIDE/NITRIDE	INITIAL OXIDE/NITRIDE
MASK 1 DEFINES ACTIVE AREA	MASK 1 DEFINES ACTIVE AREA
FIELD OXIDATION	FIELD OXIDATION
GATE OXIDATION	GATE OXIDATION
DEPOSIT POLYSILICON	DEPOSIT POLYSILICON
	MASK 2 DEFINES POLY I
	INSULATING OXIDE
	DEPOSIT POLYSILICON
MASK 2 DEFINES POLY	MASK 3 DEFINES POLY II
PHOSPHOROUS DIFFUSION	PHOSPHOROUS DIFFUSION
INSULATING OXIDE	INSULATING OXIDE
MASKS 3 & 4 DEFINE CONTACTS	MASKS 4 & 5 DEFINE CONTACTS
ALUMINUM	ALUMINUM
MASK 5 DEFINES METALLIZATION	MASK 6 DEFINES METALLIZATION
TOP GLASS	TOP GLASS
MASK 6 OPENS PAD AREAS	MASK 7 OPENS PAD AREAS

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and, since signal varies with the ratio of digit line to cell capacitance, that the Intel sense amplifier should have twice the available signal as does the MOSTEK version. Since the digit line halves (or quarters) are precharged during the \overline{RAS} inactive time (t_{RP}) to (hopefully) equal voltage, and since any difference in the starting values of the digit line voltages subtract directly from the available signal, MOSTEK may be rather more concerned about the precharge time than Intel, and, in fact, the value of t_{RP} for the MOSTEK 150 nanosecond part is specified to be 100 nanoseconds, while the t_{RP} value for the Intel 200 nanosecond part is actually smaller (75 nanoseconds).

On the other hand, the substrate (back of the chip) may be considered a noise collector which couples all areas of the circuit together. Since the clocks and decoders, prime noise generators, are strung along the short dimension of both chips, a reasonable estimate of the substrate noise would be that it peaks in the center of the short axis, falling to

zero toward the edges. The sense amplifiers in the MOSTEK design are located in the center and would presumably see a balanced noise coupling onto the digit lines, while the Intel sense amplifiers, located at the one quarter and three quarter points, might see more noise coupled onto the digit line quarters near the chip center than on the outer digit line quarters.

Since the sense amplifier naturally inverts one of the digit lines, it would be convenient if the test equipment made provision for exclusive - OR'ing either the most significant row address bit (for the MOSTEK design) or the second most significant row address bit (for the Intel design) with data into and out of the device under test such that a programmed input of all "ones" would be stored by the chip as all "highs". This facility would greatly simplify refresh and disturb tests. Of course, the sense amplifier inversion is logically removed by the chip itself so that it is transparent to the user, but the capability would be extremely useful in a test environment.

Both MOSTEK and Intel have resorted to the double-level polysilicon gate process to reduce the area of the memory cell. The process is basically an extension of the single-level polysilicon gate process common in the semi-conductor industry for years. Figure 5 is a basic comparison of the POLY IITM process as implemented by MOSTEK, and the standard single level poly process. There is only one additional mask required, plus one extra deposition and one extra oxidation step. Figure 6 depicts a cross-section through the cell and the cell schematic. The transfer gate (POLY II transistor) is used only in the cell; the threshold voltage for this transistor may be adjusted independently of the threshold voltage of the peripheral transistors. The ratio of digit line to cell capacitance is about 20:1 for the MOSTEK design and approximately 13:1 for the Intel.

MK4116 CELL AND CROSS-SECTION

Figure 6

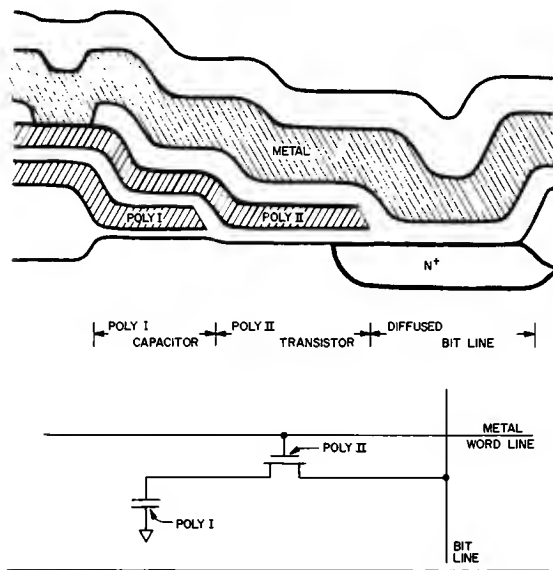


Figure 7 shows the cell layout which with minor variations, is used by both MOSTEK and Intel. The adjacent cells are located either on the same row or on rows separated by one word line and are always on adjacent columns. The first level polysilicon sheet which forms the common capacitor plate for all cells also forms the gate of an MOS field transistor which links neighboring cells. It may therefore be necessary to check for cell to cell interactions due to less than ideal field threshold voltage of this device. Also, the channel length of the transfer gate is determined by the relative alignment of first poly to second. If the misalignment is too great, the threshold voltage of the transfer gate may be reduced due to

short channel effects, making it advisable to check carefully for data loss due to the inability to keep deselected cells from leaking through the transfer gate to the digit line.

TEST PATTERNS

The problem of developing test patterns to test memories for various pattern sensitivities has been extensively reported in the literature (8)(9)(10). More recently, the emphasis has shifted towards analysis of the design and adoption of test sequences which exploit possible weaknesses (11). This approach is necessary if test times for 16K RAM's are to be kept within practical bounds. The following information, although believed to be general, applies specifically to the MOSTEK design.

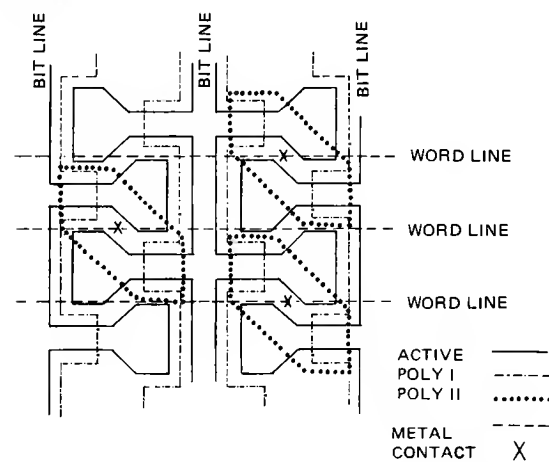
The 16K RAM is basically a synchronous machine built around a rectangular memory array, the coordinates of which are "rows" and "columns". The synchronous machine provides the timing control for the input latches, row decoder, sense amplifier, column decoder, write circuitry, and output latch. In contrast to earlier, asynchronous RAM's, the 16K nearly always fails digitally. That is, if a problem exists with the input latches, the wrong output will be generated (but not a "late" output which is correct but delayed by, for example, poor input levels). There is no "worst-case" pattern for access time since access time is controlled by the internal clock generators. This greatly simplifies the testing of gross functionality, which must only assure cell uniqueness and output validity over the specified timing and power supply ranges.

On the other hand, the memory array and sense amplifiers must still be checked for pattern sensitivities. Considering the signal detection capabilities of the sense amplifier, and its precharge requirements, a probable "worst-case" pattern for a sense amplifier is a single bit of DATA in a field of DATA. If such a pattern is run in a "row fast" mode, each sense amplifier will be required to perform some number of reads of DATA, a single detection of DATA, and complete the scan reading DATA. If the DATA bit occupies, at some time, each of the locations along the digit line, the ability of the sense amplifier to pick signal out of noise and to remove completely any influence of the preceding cycles on the present cycle will have been checked. Note that this pattern would require only as many scans as there are bits per

sense amplifier, and that all columns can be checked simultaneously.

MK4116 CELL LAYOUT

Figure 7



Considering the row select function, noise coupling considerations indicate that here too a worst case pattern might be either a single DATA bit in a field of $\overline{\text{DATA}}$, or, perhaps, a solid field. Here also the word "field" has a restricted meaning, applying only to all cells connected to a single row select line.

Several patterns check for the above failure modes efficiently; one of particular interest is the $2N^{3/2}$ "Moving Diagonal" pattern, which requires 128 write-read scans through the entire array. On the first scan, all bits are written to $\overline{\text{DATA}}$ with the exception of the 128 bits along the major diagonal which are written to DATA. The read scan verifies the correct operation of the array under these conditions. On each succeeding scan, the position of the diagonal of DATA is shifted until, on the 128 scan, it has occupied every possible position in the array. Each cell has once been the only DATA cell in a row and column of $\overline{\text{DATA}}$. This pattern has proven to be quite effective in screening the 16K RAM.

Refresh tests can be separated into two categories: still and dynamic. Still refresh tests are per-

formed by writing all locations, pausing for the refresh interval with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ inactive (high), and reading all cells. The inactive pause allows the cells to leak low but also allows internal nodes which are bootstrapped above V_{DD} by the trailing edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ to decay so that both the cells and the dynamic periphery are tested. Unfortunately, such a test normally is not worst case for the cell, as noise generated during active cycles can contribute to the loss of data in the cell. The dynamic refresh tests write data into some subset of cell (normally half of the cells) and, during the refresh interval, perform either read or write cycles on the cells not being tested, the intent being to couple charge-degrading noise onto the unaccessed test cells. Both tests are necessary to completely guarantee functionality of the 16K.

During the active portion of a cycle, 127 of the 128 rows are not selected, and must remain at OFF to prevent partial selection of a transfer gate. A test with maximum active time provides greatest opportunity for such partial selection to occur. This test might perform a write scan with minimum precharge times (t_{RP}) and maximum active time (t_{RAS}), followed by a read-modify-write scan under the same basic timing conditions, followed by a read scan to verify the "modify-write" operation. This important test is often overlooked but is in fact worst-case for many of the internal circuits.

For users desiring a basic but adequate test sequence, the above patterns provide a good starting point. Figure 8 summarizes such a sequence which should provide a reasonable degree of confidence in any RAM which passed. Special timing modes and certain timing parameters would be left unchecked, but could be easily added if desired. This test sequence requires $(28N + 4N^{3/2})$ cycles, of which all but 8N may be at the fastest allowable cycle rate. The 8N are at the slowest allowable cycle rate (maximum cycle length). If the cycle times are 375 nanoseconds and 10 microseconds, respectively, this sequence would execute in just over 4.5 seconds, exclusive of tester overhead and power supply settling times.

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POSSIBLE MINIMUM TEST SEQUENCE FOR 16K RAM

Figure 8

TEST DESCRIPTION	DATA PATTERN	FUNCTION	POWER SUPPLIES V _{DD} V _{BB}		CYCLE COUNT
MAXIMUM CYCLE	DIAGONAL	FUNCTIONALITY	13.2	-4.5	2N (t cyc = 10 μS)
	DIAGONAL		13.2	-5.5	2N (t cyc = 10 μS)
	DIAGONAL		10.8	-5.5	2N (t cyc = 10 μS)
	DIAGONAL		10.8	-4.5	2N (t cyc = 10 μS)
LOAD READ	PARITY and PARITY		10.8	-5.5	2N
			10.8	-4.5	2N
			13.2	-5.5	2N
			13.2	-4.5	2N
LOAD READ	CHECKERBOARD and CHECKERBOARD	BIT INTERACTIONS	10.8	-5.5	2N
			10.8	-4.5	2N
			13.2	-5.5	2N
			13.2	-4.5	2N
MOVING DIAGONAL	DIAGONAL	FUNCTIONALITY	10.8	-5.5	2N ^{3/2}
			13.2	-4.5	2N ^{3/2}
DYNAMIC REFRESH	ALTERNATE ROWS	DATA RETENTION	10.8	-5.5	1N + 2 mS
DYNAMIC REFRESH	ALTERNATE ROWS	DATA RETENTION	10.8	-5.5	1N + 2 mS
STILL REFRESH	ALL HIGHS	DATA RETENTION	10.8	-5.5	2N + 2 mS

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OPTIMIZED TESTING OF 16K RAMS

Testing

The new generation of 16K dynamic MOS memories places a much greater burden on the test engineer than did the earlier 1K and 4K designs. The size of the memory means that generalized test sequences which test these devices as black boxes will be far too expensive in terms of test time per device. Even though the semiconductor industry appears to have standardized on one compatible pin-out with the major controversies being decided in favor of 128 — cycle refresh and output latch controlled by the column address strobe as in the MOSTEK MK 4116, there are pitfalls for the user who does not appreciate the fact that vendor design and testing differences will result in devices with different characteristics. Test sequences which do not comprehend these differences will not be successful in eliminating marginal devices. Therefore, the test engineer must acquire an in-depth knowledge of each vendor's device and the test sequences utilized must reflect this knowledge.

The following table illustrates graphically the test time penalties paid in moving from 4K to 16K:

	Test times for various test patterns (375 ns cycle)	
	N=4096	N=16384
2N (Load-Read)	3 mS	12 mS
2N ^{3/2} (Moving pattern, row or column ping-pong)	197 mS	1.6 Sec
2N ² (Ping-pong) GALPAT)	12.6 Sec	201 Sec

When testing the 4K RAM, the test engineer could treat the device as a black box, generate all address transitions by using N² patterns, and hope for the best. Using such an approach on the 16K would result in a tester throughput of fewer than 400 parts per day.

TEST TEMPERATURE

The single most important decision to be made concerning dynamic RAM testing is test temperature. MOS devices have three basic parameters which are functions of temperature: threshold voltage, carrier mobility, and leakage currents. For N-channel silicon gate processes, threshold voltage is typically 200 millivolts lower at 100°C than at 0°C. Carrier mobility, which relates to transistor gain and therefore to circuit speed, is about 25% lower at 100°C than at 0°C. The effects of these two variables, once charac-

terized for a particular device, may be easily included by adjusting parameters such as input and output levels for the temperature range variations expected. A third variable, leakage current, is more dramatic in its effect on the device.

The refresh time of any dynamic MOS Memory may be expressed by

$$t_{REF} = A e^{-BT}$$

where T is junction temperature in °C
B is a variable relating the magnitude of the generation — recombination current to the junction temperature (units of 1/°C)

and A is a scaling constant reflecting such variables as junction area, sense amplifier design, bulk defect density.

Typical values for the variable B range from 0.053/°C to 0.060/°C implying a temperature behavior in which refresh time is halved for every 11.6°C to 13.1°C increase in junction temperature.

Testing should be conducted at elevated temperatures in order that this large variation may be tested without having to extrapolate from some non-worst-case temperature. (Since mobility is also worst-case at elevated temperature, most timing parameters are also worst-case at elevated temperatures and need not be guardbanded.)

Most 16K RAMS are specified over the temperature range 0 °C to 70 °C ambient. The junction temperature T_J depends, however, on the power dissipation (P_D) of the device by the equation

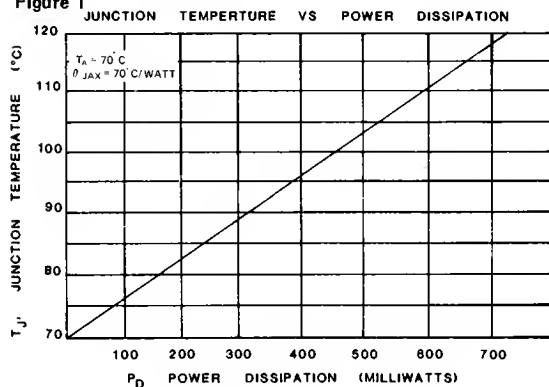
$$T_J = T_A + P_D \theta_{JAX}$$

Where θ_{JAX} is the thermal impedance between the device junction and system ambient. Figure 1 graphs this equation for $\theta_{JAX} = 70^\circ\text{C per watt}$ (standard 16 pin ceramic dual in line package).

If the device junction temperature is stabilized by using a long warm-up cycle prior to the first test, the proper test temperature is the system ambient temperature. If the test is short enough that the junction temperature does not rise appreciably under test, the proper test temperature is the junction temperature given in Figure 1. For example, a device which dissipates 430 mW must be tested at T_J=100°C in order to guarantee functionality at T_A=70°C.

JUNCTION TEMPERATURE VS. POWER DISSIPATION

Figure 1

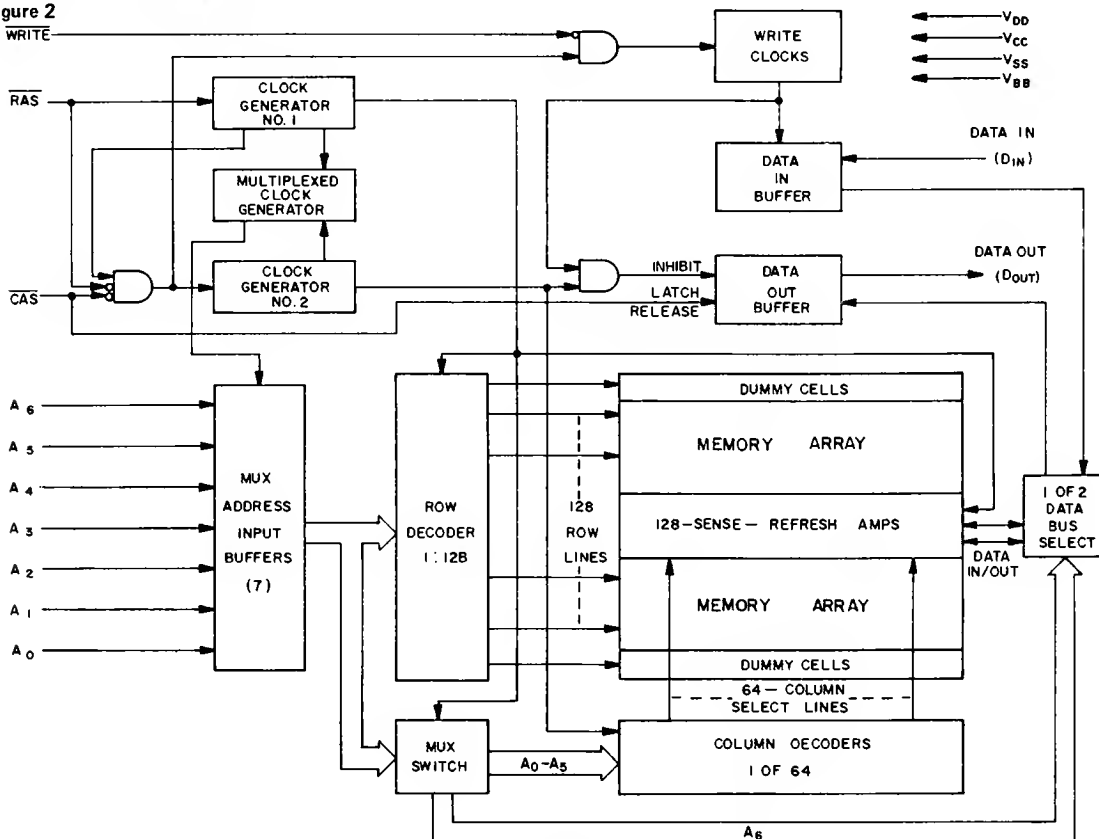


THE MOSTEK MK 4116

The block diagram of the MOSTEK MK 4116 (Figure 2) may be examined for testing implications. Note that the address input buffers are shared while the row and column decoders are independent. An addressing scheme which provides the maximum possible number of bit reversals per cycle will check

BLOCK DIAGRAM MK4116

Figure 2



for possible interactions due to the previous address. This can be accomplished efficiently in a basic load-read (2N) test by using one of the addressing schemes variously referred to as "address complement", "address select", or "MAEST".

Note further that the data out buffer is timed exclusively by an internal clock generator driven by CAS. There is no reason, then, to search for some test sequence or data pattern which is "worst-case" for the access time. Access time is absolutely determined by clock delays internal to the circuit and is only influenced by influencing these delays. Access time, along with most other timing parameters is worst-case at low V_{DD} (+10.8 volts). V_{BB} has almost no influence on access time.

Still referring to Figure 2, note that there are two 8K sub-arrays split by the sense-refresh amplifiers in the middle and having "dummy cells" at each side. These establish a voltage reference for the balanced sense amplifiers. One of the array halves, therefore, inverts data and will store an input "one" as a low level in the storage cell (a second inversion is performed by the output circuitry so that this internal inversion is not seen at the device terminals). This inversion must be taken into account when performing a refresh test.

The layout of the storage cell in the MK 4116 is shown in Figure 3. This is a conventional one-transistor dynamic storage cell, although implemented by using MOSTEK's double-level polysilicon (Poly II™) process. The row (word) select lines are metal, eliminating concern over propagation delays down the long 80 mil word lines. Data transfer to and from the cell is through the diffused column (digit) lines. The top plate of the storage capacitor is VDD (first level of polysilicon) which allows charge to be stored in the depleted region beneath this level. Metal word lines contact the second poly level which forms the gate of the transfer device isolating the storage cell from the digit line. The cell is relatively insensitive to variations in the doping level of both first and second poly. In fact, performance of the cell is primarily influenced by junction depth, oxide thickness, and mask geometry, all parameters which tend to remain constant.

MK4116 CELL LAYOUT

Figure 3

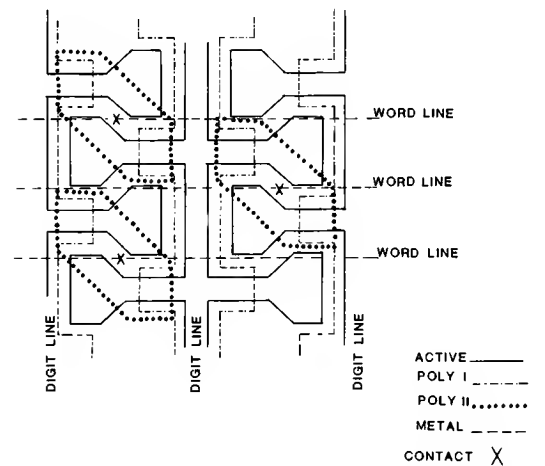
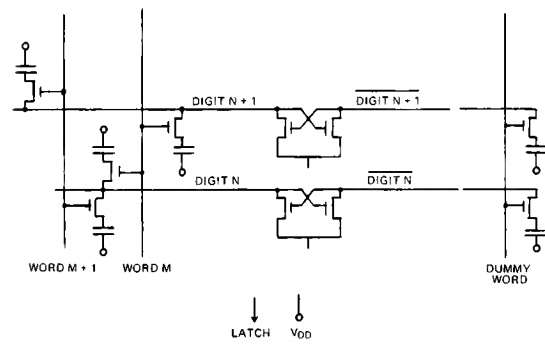


Figure 4 relates the cell, sense amplifier, and dummy cells. This figure provides a measure of topological information in addition to the electrical schematic. Capacitor-to-capacitor adjacencies in Figure 4 were carefully drawn to reflect the physical relationship of the actual layout.

MK4116 CELL, DUMMY CELL, SENSE AMPLIFIER

Figure 4



Because of the cell layout, tests to eliminate bit-to-bit sensitivities need to be considered carefully. The conventional "checkboard" pattern will result in an alternating bit-by-bit data pattern, as usual, but a "vertical bar" pattern consisting of alternate columns of highs and lows will accomplish the same result.

Two neighboring bits which might influence one another may be located on the same row or be separated by one row, but will not be on adjacent rows. Such bits must be on adjacent columns. There is also a topological mapping in the decoder layout which must be considered if rows and columns are to be accessed in a sequential manner.

SENSE AMPLIFIER MARGIN

Sense amp operation is straightforward:

1. Digit and $\overline{\text{Digit}}$ lines are precharged high, word lines and the dummy cell are precharged low, and LATCH is precharged high.
2. The selected word line turns on to VDD along with the dummy word line accessing the dummy cells in the array half which does not contain the accessed cells. The accessed cells are thus connected via the transfer gates to the digit and $\overline{\text{digit}}$ lines. Charge redistribution between the cells and digit lines causes a voltage drop on the digit line of zero to 0.3 volts if the cell contained a high level (depending on the amount of decay in the cell since the last access), or of about 0.5 volts if the cell was initially low. The dummy cell pulls the $\overline{\text{digit}}$ line down by 0.4 volts.
3. Latch is driven to ground allowing the balanced sense amplifier to discharge the digit or $\overline{\text{digit}}$ line, whichever started at the lower voltage.

Accessing a stored low level requires that the digit line be discharged by the cell, whereas accessing a stored high level is accomplished whenever the digit line is relatively undisturbed.

Design and layout of the storage array and sense amplifier is complicated by the presence on critical nodes of noise which adds to or subtracts from signal voltages, causing a data-dependent reduction in overall margin. The data pattern which creates worst-case coupling and smallest margins in the MK 4116 is a solid field of discharged cells.

Insufficient precharge of the sense amplifier, which can arise from several distinct types of processing defects, causes the result of the current cycle to depend upon the preceding cycle. One data pattern which efficiently checks for such failure modes is the "major diagonal" or its extension, the $2N^{3/2}$ "moving diagonal". Beginning with a major diagonal of ones in a field of zeroes, each successive pass through the memory moves the diagonal up one

position such that in 128 passes it has occupied every possible position. Each bit has then been the only high in a row and column of low bits.

REFRESH TESTING

Refresh tests may be roughly divided into two subgroups — active and static. Active refresh indicates that the device is continuously operated for the period during which the unaddressed row or rows is allowed to decay.

Such a test provides an opportunity for increased cell leakage, either by sub-threshold conduction through transfer gates whose word line has been driven slightly positive due to noise coupling, by cell to cell leakage if the disturbing cycles are conducted on adjacent cells, or by charge carriers injected into the substrate by some nearby node. On the other hand, a static refresh test in which both \overline{RAS} and \overline{CAS} remain inactive for the entire refresh interval allows internally precharged nodes to decay. Such a test insures that, in addition to data being retained for the refresh interval, the peripheral circuits are also functioning after the pause.

If the refresh tests are being conducted at elevated temperatures with a stable junction temperature, the worst voltage corner for refresh is low V_{DD} (10.8 volts) and high V_{BB} (–5.5 volts). If the devices are allowed to self-heat prior to testing, then the high V_{DD} (13.2 volt) corner provides maximum power dissipation, maximum junction temperature, and minimum refresh time. In any event, high V_{BB} results in higher leakage current and shorter refresh times.

DECODER AND I/O

In addition to functional tests to check for the failure modes just described it is, of course, necessary to verify proper operation of the decoders and the input and output of data. Here no special techniques are required beyond those widely utilized in industry 1K and 4K RAM testing since this functionality may be proven with simple 2N tests. In fact, testing of the MK 4116 with its data output latch controlled exclusively by \overline{CAS} is much simpler since there is no influence on the current cycle by a previous cycle as is the case for latched output designs. Parametric tests verifying input and output leakage specifications are also identical to that required by 4K devices, although here again the control of data out by \overline{CAS} simplifies the output leakage measurement.

SUMMARY

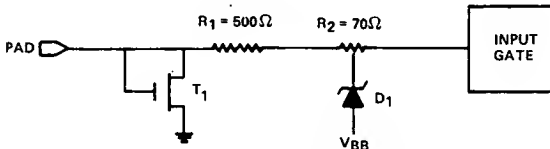
Some of the basic failure mechanisms of the MK 4116 have been explained, along with suggested tests which efficiently isolate each mechanism. The only other required tests check the remaining data sheet timing parameters at the specified voltage limits to verify minimum and maximum values, and are simple load-read patterns. It should be possible to implement a highly effective device screen which takes no longer than 20 seconds per device and still provides high confidence that defective devices will be eliminated.

INPUT PROTECTION CIRCUIT

All signal inputs to the MK 4116 have the input protection circuit shown in Figure 1 integrated onto the chip. The purpose of the circuit is to protect the device from damage caused by static voltages that may be encountered during shipping and handling.

INPUT PROTECTIVE CIRCUITRY

Figure 1



T_1 is a metal gate field transistor having a threshold voltage of approximately 12 volts, and D_1 is a $N^+ - P$ diode whose breakdown is lowered by the presence of a gate electrode at substrate (V_{BB}) potential on the periphery of the diode.

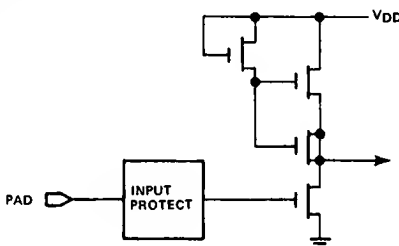
Conventional testing of the electrostatic protection devices using a 50–100 picofarad capacitor charged to some variable potential in the range of 500 to 1000 volts and discharged into the input through a 1K-2K ohm resistor have been performed by MOSTEK and demonstrate that the protection is adequate. Customer tests of the protective devices should be limited to 50 picofarads, 500 volts discharged through a 1K ohm resistor. Exposure to conditions exceeding these may affect reliability of the device.

All power supply inputs (V_{DD} , V_{CC} , V_{SS}) are essentially large area N^+ diffusions to the P-type substrate (V_{BB}).

The functional circuitry for the clock inputs (\overline{RAS} , \overline{CAS} , \overline{WRITE}) looks like:

CLOCK INPUT CIRCUIT

Figure 2

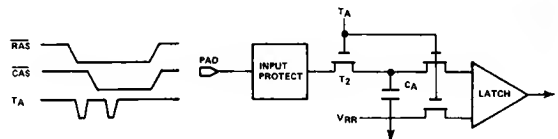


which is a fairly conventional MOS inverter. When determining the input capacitance of any such circuit, the power supplies should be at normal operational levels and, if an AC signal is supplied at the input, the amplitude of this signal should be normal (0–3 volts) to reduce the voltage gain and therefore the Miller capacitance of the input stage.

The input stage for address and data input signals is:

ADDRESS AND DATA INPUTS

Figure 3

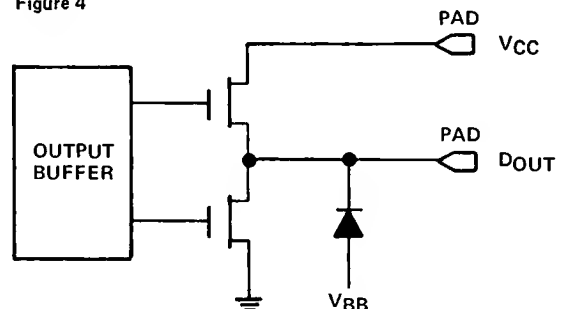


where T_A is an internally generated clock and V_{RR} an internally generated reference voltage (approximately one-eighth of V_{DD}). T_A isolates the storage capacitor C_A from the external signal as soon as possible after \overline{RAS} or \overline{CAS} , allowing the applied signal to change during the operation of the internal latch. Note that, if the external signal switches to a level more than one threshold voltage below ground (or has negative undershoot going more than one threshold below ground) the transistor T_2 may turn back on at the improper moment, allowing the discharge of capacitor C_A and resulting in improper operation of the input latch. This is the reason that the V_{IL} of all signals is limited to -1.0 volts in the negative direction.

The data output circuitry is given in Figure 4.

DATA OUTPUT CIRCUITRY

Figure 4



In general, extreme care must be exercised when making measurements on the $DOUT$ that both the transistors of the output stage are turned "OFF". It is sufficient on the MK 4116 (although not on the earlier MK 4027 which has a latched output) to have

V_{DD} and V_{BB} within the normal operating range and the \overline{CAS} level above 2.7 volts ($V_{IH\overline{C}}$). Under these conditions, both transistors will be held "OFF" and leakage measurements may be made on the output pin.

ADDRESSING CONSIDERATIONS WHEN TESTING THE MK4116

Testing

Customer engineers responsible for evaluation and incoming testing of Random Access Memories normally require a description of the internal topology of a device in order to check for "worst case" patterns or to optimize test sequences. This paper will provide such information for the MK 4116 16-kilobit dynamic RAM.

Due to the complexity of the part, this information is not quite so straightforward as in earlier RAMs produced by MOSTEK. It is necessary that the test engineer keep in mind four separate topological alterations:

1. Address Topology

The labels for address pins as given on the MK 4116 data sheet were selected for marketing convenience and do not reflect the internal least significant bit (LSB) to most significant bit (MSB) layout. It is necessary to relabel the seven address lines according to Figure 1.

All references in this paper to a particular address are understood to refer to the actual MK 4116 address, not the data sheet address.

2. Decode Topology

Efficient layout of the row and column decoders results in a scramble of the address inputs which must be observed if, for example, it is required that rows and columns be accessed in a "nearest neighbor" manner. The logic necessary to descramble this decode topology is given in Figure 2. Note carefully that Figure 2 gives addresses in terms of their row (R_N) and column (C_N) components. The multiplexing of R_N and C_N such that R_N is valid at \overline{RAS} time and C_N is valid at \overline{CAS} time produces the address input A_N .

3. Data Polarity

Utilization of a balanced sense amp located between rows 6310 and 6410 of the matrix requires that one of the two halves of the matrix invert data (this inversion is comprehended by internal circuitry so that it is

transparent to the user). If it is necessary, for example, to write all 16 kilobits to a charged state, the data polarity of Figure 3 must be observed.

4. Bit Topology

Maximum utilization of silicon real estate required that the matrix layout be done as indicated by Figure 4.

Note that instead of "conventional" layouts which have all cells on the same side of the bit line, the cells of the MK 4116 are laid out in pairs, one on each side of the bit line. Also, in contrast to "conventional" layouts having the transfer gates in one row, the transfer gates associated with one word line in the MK 4116 occur in pairs, one above and one below the (metal) word line. This layout has implications for the test engineer. For example, a data pattern which writes alternate columns to the same data state (called by MOSTEK "VBAR") will perform a check for bit-to-bit shorts as well as the conventional "checkerboard" pattern. The addressing sequences required to perform a "nearest neighbor disturb" are therefore a function of both the decode and the bit topology.

For the sake of completeness, although not strictly necessary, Figure 5 relates the location of inputs and the individual bits to the actual chip.

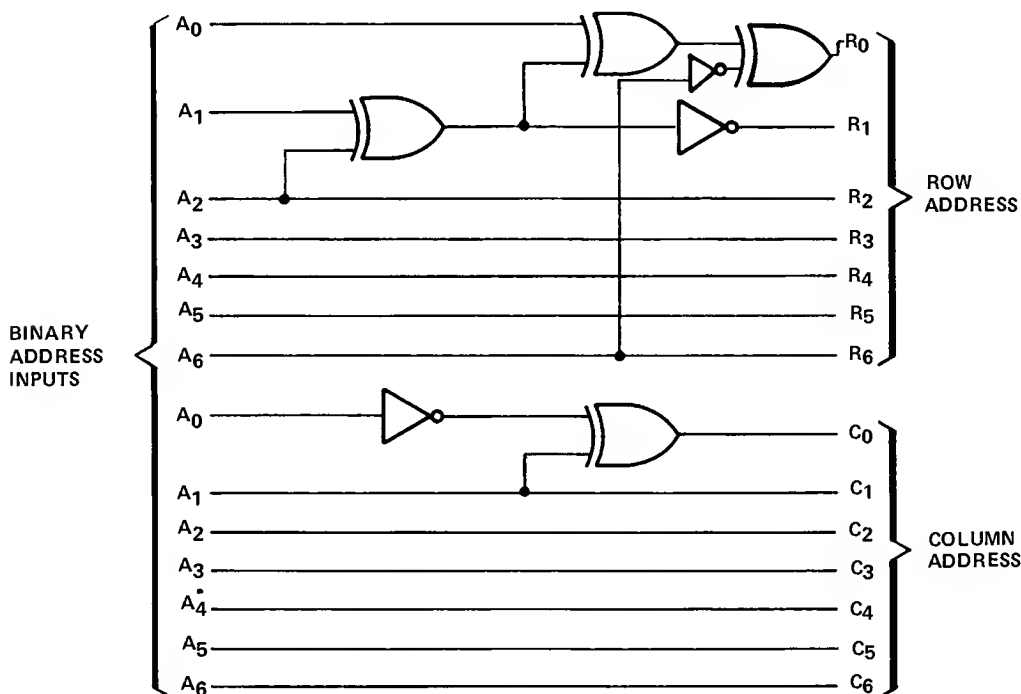
TRANSFORMATION FROM DATA SHEET PIN NAMES TO MK4116 INTERNAL PIN NAMES

Figure 1

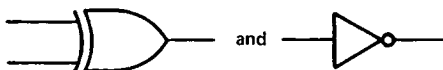
<u>PIN NUMBER</u>	<u>MK 4116 DATA SHEET</u>	<u>MK 4116 ACTUAL</u>
13	A6	A0
10	A5	A1
11	A4	A2
12	A3	A3
7	A1	A4
6	A2	A5
5	A0	A6

EXTERNAL ADDRESS TRANSFORMATION REQUIRED TO DESCRAMBLE MK4116 INTERNAL DE-CODER (MULTIPLEXER NOT SHOWN)

Figure 2



NOTE: The logic symbols



are used solely to indicate the logic function "Exclusive - OR" and "NOT", respectively; The above figure is not a suggested implementation of logic.

EXTERNAL TRANSFORMATION NECESSARY TO COUNTERACT THE INTERNAL INVERSION OF DATA WITHIN THE MK4116

Figure 3



NOTE: The same transformation will be required on the D_{OUT} of the MK 4116. This data inversion is transparent to the user and need be considered only in testing of the MK 4116.

NOTE: The logic symbol

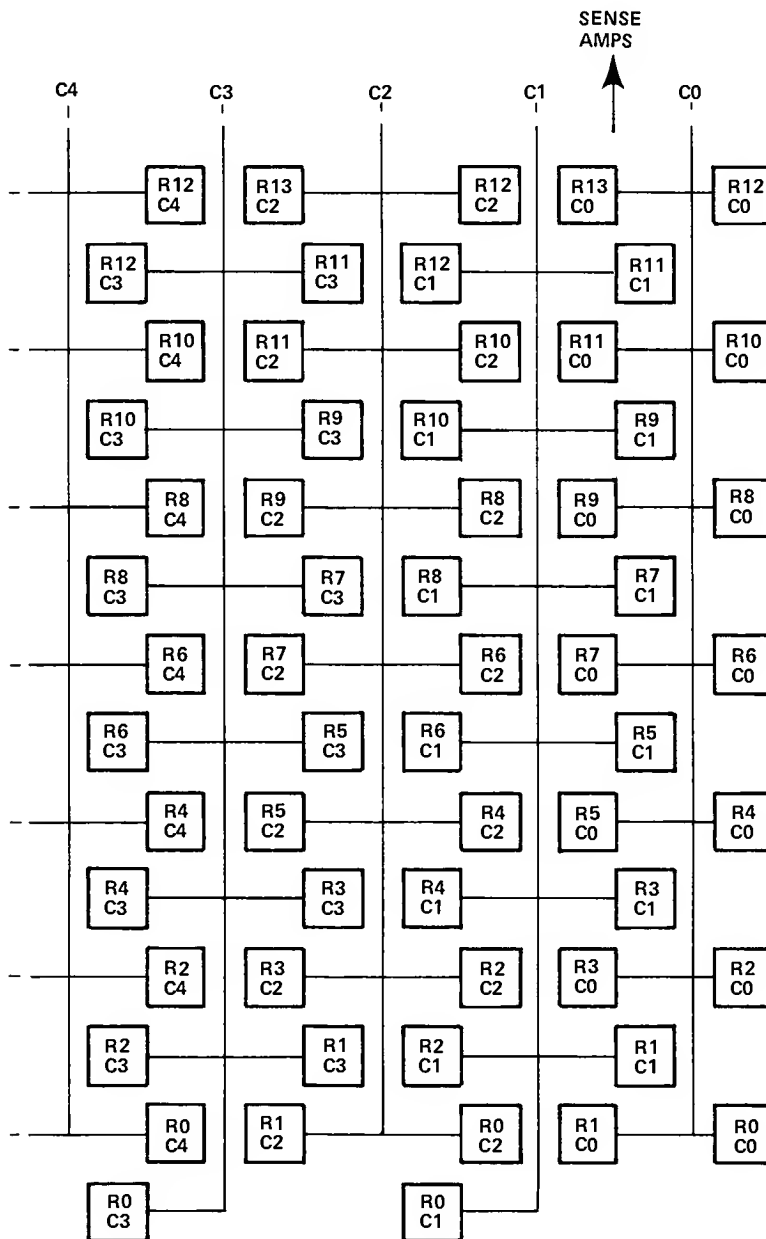


is used solely to indicate the logic function

"Exclusive - OR". The above figure is not a suggested implementation of logic.

INTERNAL BIT TOPOLOGY OF THE MK4116

Figure 4

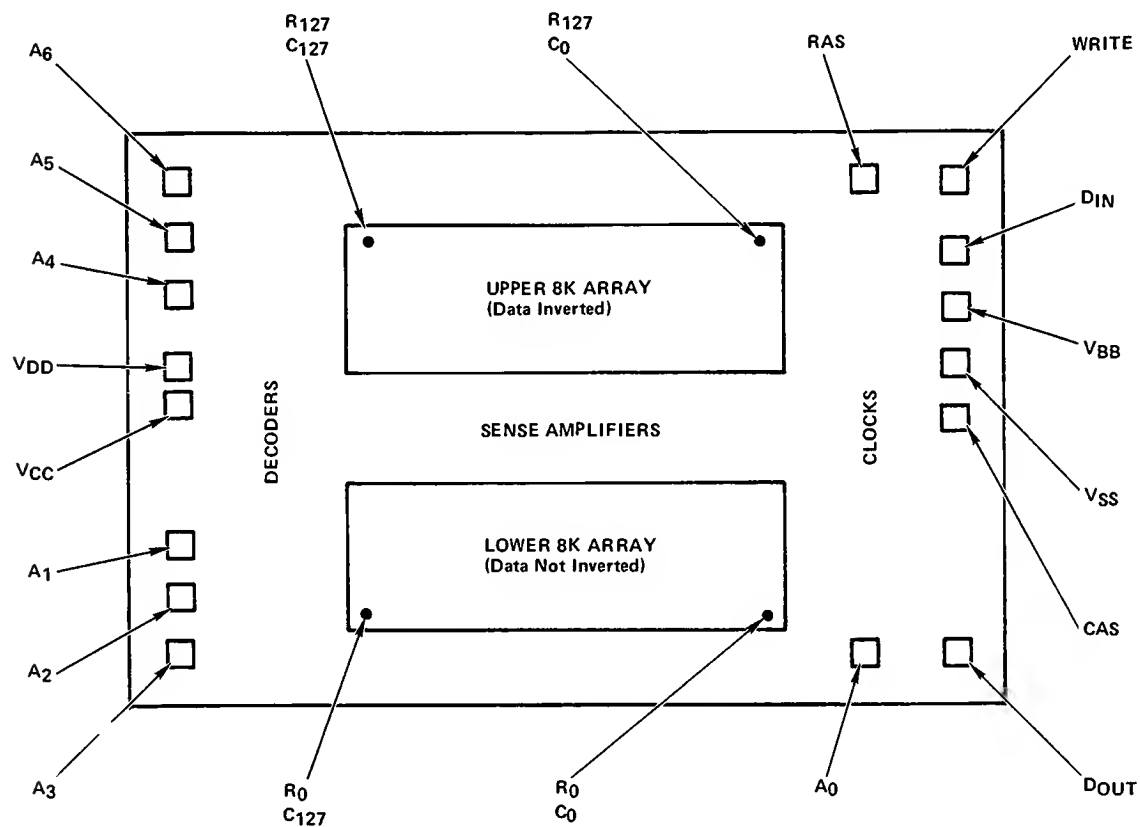


DYNAMIC
RAMS

The area represented here is physically located in the lower right hand corner of the bottom half array. (See Figure 5)

INTERNAL TOPOLOGY OF THE MK4116

Figure 5



This defines the functional test sequence used by MOSTEK for post burn-in final testing of its 16384 bit dynamic random-access memory, the MK 4116. The same sequence, with Test No. 4 deleted, is used for the QC audit performed immediately prior to shipment, and for periodic readings during all life test studies performed by MOSTEK. The testers used for all such testing at MOSTEK are Siemens 203 (or an earlier version of the same basic tester, the Computest V200).

The test temperature is an equivalent junction temperature for operation at 70°C continuous still air ambient as calculated from the equation

$$T_J = T_A + P_D \theta_{JX}.$$

Any parameter which is not worst-case at the elevated temperature is compensated to account for variation over the 0°C–70°C specified operating temperature range.

All timing edges are set to data sheet limits plus or minus guardband deltas where appropriate; the power supplies are set to the minimum and maximum data sheet limits plus or minus appropriate guardband deltas (with the exception of V_{CC} which

set to the minimum data sheet level only). Input levels are

V_{IH} = minimum data sheet limit minus guardband delta.

V_{IHC} = minimum data sheet limit minus guardband delta.

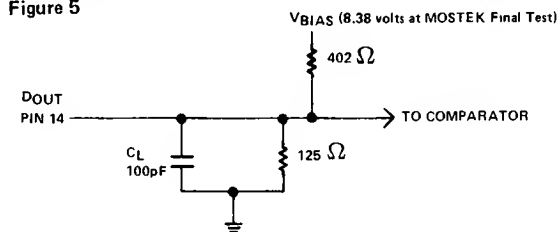
V_{IL} = maximum data sheet limit plus guardband delta.

unless otherwise noted. The output load is as shown in the attached figure.

MOSTEK reserves the right to make changes in this test sequence at any time and without notice.

OUTPUT LOAD

Figure 5



TEST NO.	TITLE	DESCRIPTION	REASON
1	Continuity (low bias)	Force — 0.7 volts relative to V _{BB} on each pin in turn, and check for a current of 100 μ A or greater on each pin. If a pin fails continuity, High Bias Continuity (Test 2) is attempted.	
2	Continuity (high bias- attempted only if Test 1 fails)	Force — 5.0 volts relative to V _{BB} on each pin in turn, and check for a current of 100 μ A or greater on each pin. If all pins pass this test, the part is rejected as a 'high substrate resistance' part.	
3	Pre-stress	An address parity data pattern is written into the matrix using a binary addressing sequence (rows fast). The data pattern is immediately read back using the same addressing sequence. The write and read sequences are repeated for data complement.	This test checks for minimum functionality.
4	Stress	Multiple runs are made using a procedure the same as Test 3 except that errors are ignored and the voltage between the power supplies is increased.	Places maximum field intensity across gate oxides.
5	Post-stress	Same as Test 3	This test checks to see if the stress either destroyed or latched up the part.
6	I _{DD} operating (average) (IDD1)	With V _{BB} at the data sheet minimum and V _{DD} at the data sheet maximum, measure I _{DD} (average) while repetitively writing "zero" at location (0,0) at minimum t _{RC} . Reject the part of the measured value exceeds I _{DD2} (max).	
7	Substrate Leakage (IBB2)	All pins other than V _{BB} are grounded. V _{BB} is biased at —20 volts through the meter and checked for less than 10 μ A leakage current.	

TEST NO.	TITLE	DESCRIPTION	REASON
8	Input Leakage (I_{IL})	V _{BB} is biased at -5 volts with respect to all other supplies, ground, and the output pin. All inputs are forced to 0 volts and the current measured on each individual input is considered a failure if it exceeds 7 μ A magnitude. 10 volts is then forced sequentially on each input, and the current is again measured to the same fail condition.	
9	I _{DD} Standby	The device is powered up with minimum V _{BB} , maximum V _{DD} , and maximum V _{CC} . The output is left floating and unused inputs are forced to 0 volts. Multiple toggles between 5 volts and 0 volts are applied to \overline{RAS} and \overline{CAS} ; after toggling \overline{RAS} and \overline{CAS} are at 5 volts. The maximum I _{DD} in the standby state is then measured.	
10	Output Leakage (I_{OL})	The device is powered up with maximum V _{DD} , maximum V _{CC} , and minimum V _{BB} . Unused inputs are forced to 0 volts. Multiple toggles between 5 volts and 0 volts are applied to \overline{RAS} and \overline{CAS} ; after toggling, \overline{RAS} and \overline{CAS} are at 5 volts. 5.5 volts is connected to the output pin through the meter, and the current is measured against a failure condition of leakage greater than 7 μ A. The output pin is then forced to 0 volts and the current is again measured against the same failure conditions.	
11	VBUMP	At minimum V _{DD} and maximum V _{BB} the entire matrix is written to discharge cells. The V _{DD} and V _{BB} supplies are then slewed in the positive direction, and the entire matrix is read for discharge cells.	This test verifies proper sense amp margins for detection of low storage states.
12	Start-up - Address Parity	After powering up all supplies from 0 volts, eight \overline{RAS} -only cycles at maximum cycle time are executed before the entire matrix is written with complement data using a binary addressing sequence (rows fast). It is then read for complement data, written with true data, and finally read for true data using the same addressing sequence.	This test checks that the internal circuitry is adequately initialized with 8 preliminary cycles.

TEST NO.	TITLE	DESCRIPTION	REASON
13	TMOD-Diagonal	The entire matrix is written to a background of complement data. Using a binary addressing sequence (rows fast) the matrix is written using cycles with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active pulse widths of 10 μSEC . There is a standby stall executed after each column has been written to finish the refresh limit interval. The matrix is then read using the same length cycles and addressing scheme with no standby stalls. The procedure is repeated for complement data.	This test checks both the ability to write and the validity of the output data at the end of a long active cycle. It checks the ability of the row decoders to hold the 127 non-selected row lines "OFF" during a long active cycle, and the ability of the sense amplifiers to read a single bit in a field of complement data.
14	YFAST-Rows 0, 63, 64, 127	Using a binary addressing sequence in a column fast mode, the matrix is written with data until the refresh limit interval is reached. At that time each row is refreshed using a single $\overline{\text{RAS}}$ -only cycle. The entire matrix is written, read, written with complement data, and read for complement data is this matter.	This test checks for column decoder noise effects on the sense amps and for the other noise related failure modes.
15	Page Mode-Address Parity	Using a binary addressing sequence (rows fast), the entire matrix is written to a background of zeroes. For the number of page cycles that can be executed during the $\overline{\text{RAS}}$ active time of 10 $\mu\text{seconds}$, each row is written with true data. A portion of all 128 rows is written, read, written with complement data, and read for complement data using page mode. This procedure is repeated for a new set of addresses until the entire matrix has been finished. Finally using a normal cycle binary addressing sequence (rows fast) the entire matrix is read for complement data.	This test checks reading, writing, and duration of page mode operation. It also checks the refresh limit interval.
16	Early $\overline{\text{CAS}}$, Late $\overline{\text{Write}}$ -Displaced double checker-board	Using a binary addressing sequence (rows fast) throughout this test, the entire matrix is written with complement data, written with true data,	This test checks for the refresh limit during an inactive stall as well as "Early

TEST NO.	TITLE	DESCRIPTION	REASON
17	Address Complement-Horizontal Bars	<p>read for true data, and written with complement data using normal cycles. Using a late write cycle, the matrix is read for complement data and written with true data in the same cycle. After the entire matrix is written, a standby stall is executed for the refresh limit interval. Using a late write cycle, the matrix is read for true data and written with complement data in the same cycle. Another standby stall for the refresh limit interval follows. The matrix is read for complement data using normal cycles. Finally, the entire matrix is written with true data, read, written with complement data, and read for complement data using cycles with minimum t_{RCD}.</p> <p>Using a rows fast, complement addressing sequence (address, address complement, address + 1, . . .), the entire matrix is written, read, written with complement data, and read for complement data.</p>	<p>CAS" and "Late Write" modes of operation.</p> <p>This test checks the integrity of the address latches and decoders using an addressing sequence which generates many transitions on all address inputs.</p>
18	March-Ones	<p>Using a binary addressing sequence (rows fast), the entire matrix is written with true data. The matrix is then scanned by first reading a cell, then writing it with complement data, and finally reading it for complement data before proceeding to the next cell location. The memory is scanned again by reading a cell for complement data, then writing it with true data, and finally reading it for true data before proceeding to the next cell location. The procedure is then repeated with the addresses complemented during an identical data and data complement sequence.</p>	Checks for address uniqueness.
19	March-Checkerboard	Same as Test 17.	

TEST NO.	TITLE	DESCRIPTION	REASON
20	High Impedance Output State	Using a binary addressing sequence (rows fast), the entire matrix is written with ones and the output is checked to be in an open-circuit state. Next, while the entire matrix is read, the output is checked to be in an open-circuit state during the time CAS is in precharge. The procedure is repeated with zeroes as the data.	This test checks the open-circuit state of DOUT.
21	Vertical Bar	Using a binary addressing sequence (rows fast), the entire matrix is written to a background of complement data. Then the matrix is written with complement data, and finally read for complement data.	Checks for column decoder or adjacent bit interactions.
22	Vertical Bar; Wide inputs	This test is the same as Test 20 except input signal levels are at the data sheet extremes.	
23	Double Checkerboard	Same as Test 20	
24	Ones	Same as Test 20	
25	Walking Diagonal	This is the same as Test 20 except the test is run with the diagonal in all 128 possible positions.	
26	Matrix High	Using a binary addressing sequence (rows fast), all the cells in the matrix are written to a charged state. For the refresh limit interval an attempting write made to disturb half the matrix by generating write cycles which use column fast complement addressing. The test half of the matrix is then read for charged cells. The other half of the matrix is tested for the refresh with the same procedure (the disturbs generated use column fast addressing).	This test checks refresh in a dynamic disturb environment.

TEST NO.	TITLE	DESCRIPTION	REASON
27	Matrix Low	This is the same as Test 25 except the cells in the matrix are written to the discharged state and the disturb time is 100 milliseconds.	This test checks for faulty gate oxides which allow discharged cells to leak toward VDD.
28	tCRP-Address Parity	This is the same as Test 20 except that $\overline{\text{CAS}}$ goes into precharge (logic 1) after $\overline{\text{RAS}}$ goes active (logic 0), and the output is checked for a continued valid condition for the duration of the CAS active time.	This test checks that the output remaining is dependent only on $\overline{\text{CAS}}$ remaining active (logic 0) and is independent of $\overline{\text{RAS}}$ returning to the inactive (precharge: logic 1) state.

TEST NUMBER

All functional Tests
(additional parameters
are listed below)

PARAMETERS CHECKED

t_{RAC} , t_{CAC} , t_{RP} , t_{RAS} (min), t_{RSH}
 t_{CSH} , t_{CAS} (min), t_{RCD} (max), t_{RSH}
 t_{RAH} , t_{ASC} , t_{CAH} , t_{WP} , t_{DS} , t_{DH}

Test 11

t_{RWL} , t_{CWL}

Test 12

t_{RAS} (max), t_{CAS} (max), t_{RWL} , t_{CWL} , t_{REF}

Test 13

t_{RWL} , t_{CWL} , t_{REF}

Test 14

t_{RCS} , t_{RCH} , t_{WCH} , t_{CP} , t_{REF} , t_{RAS} (max)

Test 15

t_{RCD} (min), t_{RCS} , t_{RCH} , t_{WCH} , t_{WCR} , t_{DHR} , t_{REF} ,
 t_{CWD} , t_{RWD}

Test 16, 17, 18
20, 21, 22
23, 24, 26

t_{RCS} , t_{RCH} , t_{WCH} , t_{WCR} , t_{DHR}

Test 19

t_{OFF} (max), t_{WCS}

Test 25

t_{RCS} , t_{RCH} , t_{WCH} , t_{WCR} , t_{DHR} , t_{REF}

Test 27

t_{CRP}

As the delivery of a new generation of 16K dynamic MOS random access memories reaches higher volume stages, new and more complex problems are confronting both the device test engineer and the test equipment manufacturer. Economically feasible solutions to many of the problems will require the adoption of new and sometimes controversial philosophies regarding memory testing. Certainly a more thorough characterization and knowledge of each device type is required in order to insure adequate testing within reasonable test time limits.

TESTING PROBLEMS

Probably the most obvious problem associated with testing 16K RAMs is that of test times. Since many commonly used pattern sensitivity tests vary in length as a function of the number of bits in the memory (N) by a factor of $N^{3/2}$ or N^2 , test time considerations for production testing of 16K RAMs can be quite significant. The following table illustrates the test time penalties paid in moving from 4K RAM testing to 16K RAMs:

TEST TIMES FOR VARIOUS TEST PATTERNS (CYCLE RATE = 375ns)		
	N=4096	N=16384
2N(load-read)	3ms	12ms
2N ^{3/2} (moving pattern, row or column Ping-Pong)	197ms	1.6sec.
2N ² (Ping-Pong GALPAT)	12.6sec.	201sec.

The test times listed assume only one pass testing. Testing at multiple voltage corners, timing sets, temperatures, etc. will increase the test times listed for each pattern accordingly.

A second problem which is aggravated by higher speed specifications for 16K RAMs is that timing accuracies on presently available memory test equipment are often not adequate to test particular timing specifications. For example, higher speed 16K RAM specifications call for a row address setup time specification of 0ns and a row address hold time specification of 15ns relative to the row address strobe input. For a tester specified at ± 1 ns accuracy on any

timing edge from the programmed value including internal clock skews, cables, driver, and transition times, the actual value of a row address hold time programmed to be 15ns could be as little as 13ns or as much as 17ns and still be within the tester specification. Since the actual device speed distribution for this parameter may be less than 10ns wide, a ± 2 ns tester accuracy could result in significant correlation problems between testers if an attempt were made to specify and test this parameter to the actual device capabilities.

A potentially more severe problem affecting 16K RAM test correlation is power supply, input, and output noise during functional testing. Power dissipation on 16K dynamic RAMs is dynamic in nature with power supply current transients sometimes in excess of 100ma occurring synchronously with internal device clock edges charging and discharging the capacitive loads of internal circuit nodes. As seen in Figure 1, the rise and fall times of these current transients can sometimes be as short as 10ns. Because of these transients, it is extremely important that proper power supply decoupling techniques be used

TYPICAL CURRENT WAVEFORMS FOR MK4116

Figure 1



and that the amount of resistance and inductance in the power supply leads from the tester be minimized to insure relatively "clean" signals at the device during functional testing. However, even with extensive engineering precautions it is sometimes impractical to achieve less than two or three hundred millivolts of peak-to-peak noise on power supply and signal inputs at the device during functional testing especially when a temperature controlled handler is also involved. Temperature controlled handlers usually complicate the problem of minimizing inductance and decoupling power supplies as near to the device as possible and therefore can add significantly to the magnitude of noise at the device.

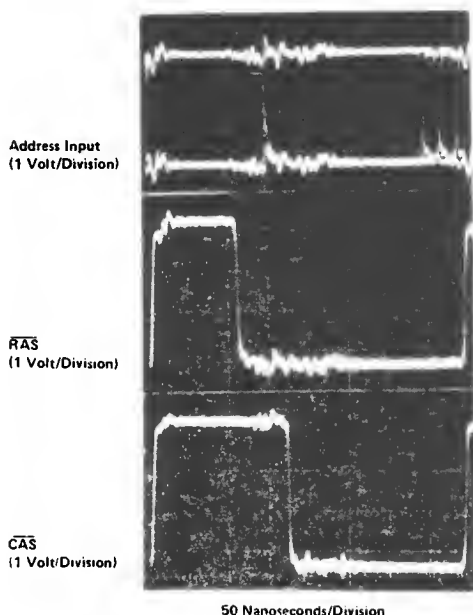
Figures 2 and 3 are examples of the relative integrity of the input signals measured at the device during functional testing of a 16K RAM with the device under the test being physically located first at the test head and then at the end of the handler interface connections. For the example shown, the total lead length for each handler interface signal connection including contactor is approximately 2 inches.

The effects of noise during functional testing vary depending on device type and test conditions. However, in general, noise problems become more severe

on higher speed devices. Since the internal clocks of these devices operate at a higher speed, the current transients on the power supplies increase in magnitude and thus induce more noise than slower devices. Also the "windows" during which data is sampled become shorter on faster devices enabling noise of short durations to have a more severe effect. For example, consider a previous generation 4K RAM with a minimum specified access time of 250ns and a minimum address valid time of 60ns versus a new generation 16K RAM with a minimum specified access time of 120ns and a minimum address valid time of 15ns. The 250ns 4K RAM typically requires that the addresses be valid for a minimum of 30ns in order to interpret the address data correctly. However, on the faster 16K RAM design, in order to allow more time for system address multiplexing, a circuit was developed capable of interpreting valid addresses in less than 5ns. For the 4K RAM the effects of a noise transient of a 5ns duration on an address input during the valid address sampling time would probably be insignificant since it's magnitude would be integrated over a 30ns period but for the 16K RAM the effects of the same noise transient during it's address sampling time would obviously be much more significant. Noise transients should not cause failures in 16K RAM operation unless the peak voltages of the transients violate the specified dc opera-

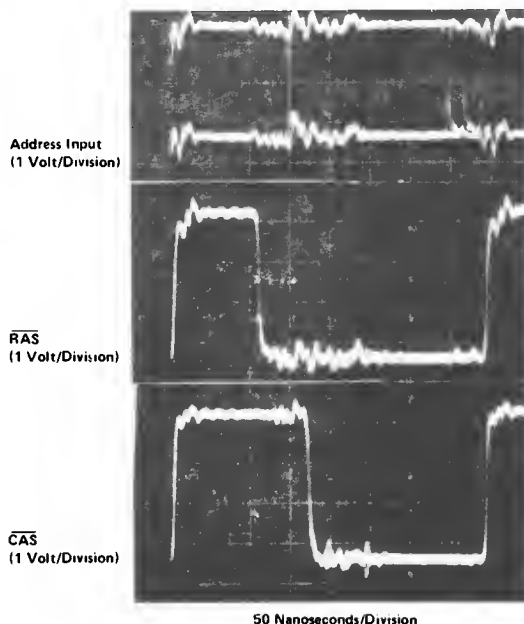
16K RAM INPUT TEST SIGNALS AT TEST HEAD

Figure 2



16K RAM INPUT TEST SIGNALS AT TEST SITE OF TEMPERATURE HANDLER

Figure 3



tion conditions for the device. Therefore for a system having a dc logic "0" level of 0.4 volts, a positive 400 millivolt noise transient should have no effect on the operation of 16K RAMs in the system specified to operate with an input logic "0" level of 0.8 volts maximum. However, under "worst case" test conditions with the dc logic "0" input level set at 0.8 volts, transients of even smaller magnitudes can cause device failures resulting in tester correlation problems.

As 16K RAM designs continue to achieve higher performance goals, the problems of distinguishing device failures versus failures induced by noise transients or timing inaccuracies of the test equipment are reaching a new order of significance. Attempts to do "worst case" testing of all specified device parameters simultaneously will usually result in the failure of some quantity of devices that actually, will meet specifications. In many cases a thorough characterization of the device design and process to be utilized can eliminate the need for 100% testing for all specified limits and conditions.

CHARACTERIZATION

The success of any characterization and resulting economically feasible production test program for a particular 16K RAM device type is highly dependent upon the RAM design. If the device is marginal and subject to complex pattern, data, temperature, or voltage sensitivities the development of a comprehensive and economically practical production test procedure could prove to be impossible. Unlike previous 1K and 4K RAM designs, deficiencies such as N² pattern sensitivities cannot be tolerated in 16K RAMs. When proper techniques are utilized, it is possible for 16K dynamic RAMs to be designed so that sensitivities due to process variations and weaknesses can be detected using relatively simple and economical address and data pattern test sequences.

The goal of a 16K RAM device characterization should be to identify any sensitivities of the particular 16K RAM design over the full production range of process parameters and the resulting production tests required that are comprehensive in screening for device sensitivities, optimized in terms of test time and economics, and operate within the constraints of the available test equipment. One of the first and most important steps in such a characterization is the selection of the sample to be analyzed. The sample should be large enough to contain a variety of process weaknesses and cover several different fabrication weeks to allow for a maximum of process parameter variation. For some tests such as timing and input voltage parameter characterization, a few hundred devices are probably sufficient, but for other tests such as pattern characterization where

more random types of sensitivities can occur, several thousand devices may be required. In order to insure that particular device characteristics do not change over a period of time, it is advisable to periodically repeat portions of the characterization sequence.

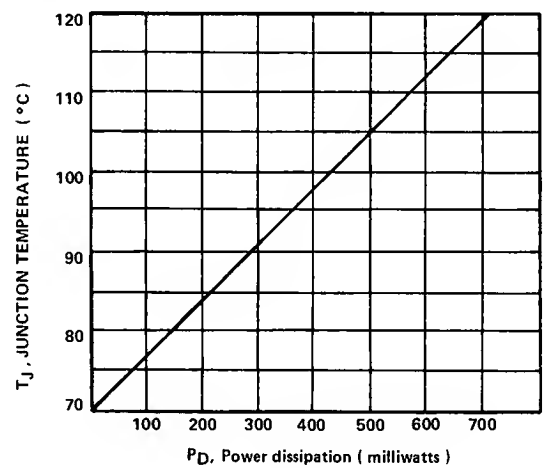
Since virtually all characterization tests will be repeated at the specified temperature extremes for the device, the junction temperature at which each device should be tested in order to guarantee the specified maximum ambient temperature for that device type should be first determined. Most 16K RAMs are specified over the temperature range 0°C to 70°C ambient. The junction temperature (T_J) of each device depends on the power dissipation (P_D) of that device by the equation:

$$T_J = T_A + P_D \theta_{JAX}$$

θ_{JAX} is the thermal impedance between the device junction and system ambient. Figure 4 is a graph of this equation for $\theta_{JAX} = 70^\circ\text{C per watt}$ which is standard for a 16 pin ceramic dual-in-line package. In order to calculate the proper junction test temperature for a 70°C ambient, the power dissipation on a sample of 16K RAMs must be measured operating continuously at an ambient temperature of 70°C and at the maximum specified frequency.

JUNCTION TEMPERATURE VS. POWER DISSIPATION FOR T_A = 70°C

Figure 4



If the device junction temperature is stabilized by using a long warm-up period at the maximum specified operating frequency prior to the first test, the proper test temperature is the specified maximum ambient temperature. If the test is only a few seconds long, then the junction temperature will rise during test only by a few degrees and the proper test temperature should be nearer to the calculated value for junction temperature.

The first stages of the characterization tests should include an extensive analysis of the voltage, power dissipation, and timing characteristics and margins of the device. The test patterns used for these tests will generally be very simple such as a load-read checkerboard or diagonal pattern. For input voltage and timing testing, each device should first be tested at the specified limits for all parameters at the four voltage corner extremes of V_{DD} and V_{BB} . V_{CC} margin testing is usually not necessary since this power supply is connected only to the device output. Each input timing and voltage parameter should then be varied separately until a failure occurs, recording the last passing value of the parameter being tested. If during these tests any parameter evaluated appears to fail or be marginal to a specified limit, then the reason for this condition should be further evaluated with the cause being isolated to a design process or tester fault. A typical example of this type of condition for a 16K RAM might be an indication from the initial characterization data that the maximum input zero level specification of 0.9 volts on the address inputs is marginal when in fact further investigation isolates the problem to noise on the address inputs at the device during the times at which the row and column addresses were being strobed into the device. In this case it would be necessary to correct the problem on the test equipment or compensate the input zero voltage level so that the data from further characterization tests would not be erroneously influenced.

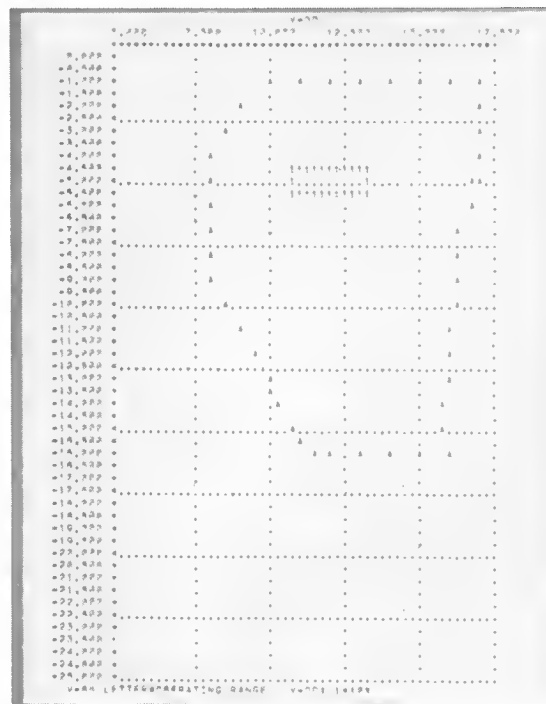
A widely used and highly effective method of characterizing power supply margins is to run a V_{DD} vs. V_{BB} schmo plot. This method involves holding V_{DD} or V_{BB} at a fixed value while searching for the failure limits of the other power supply followed by changing the fixed value of the supply to a new value and repeating the procedure. All parameters except V_{DD} and V_{BB} should be held at the specified limits during the tests. Figure 5 is an example of a typical schmo plot for a 16K RAM. Again any indication of a failing or marginal condition to a specified limit should be investigated further and the cause isolated.

Probably the most lengthy portion of a 16K RAM device characterization is the pattern sensitivity evaluation. In the case of many 1K and 4K RAM evaluations this portion of the characterization was not completed. Instead lengthy pattern sensitivity tests were inserted into production test programs with the hope that these tests would be effective in screening for any pattern sensitivities that might exist. This philosophy can obviously not be economically applied to 16K RAM testing.

A thorough 16K RAM pattern sensitivity characterization should include a variety of pattern tests designed to screen for different types of failure

V_{DD} VS. V_{BB} SCHMOO PLOT FOR 16K DYNAMIC RAM

Figure 5



modes and sensitivities of RAMs. These tests are usually referred to by names such as load-read, address complement, march, active refresh, still refresh, walking columns, walking diagonal, galloping rows, galloping columns, write disturb, surround disturb, column disturb, and galpat. It is usually sufficient to run most of the pattern tests at maximum specified frequency but a sample of patterns such as march, address complement, and walking diagonal should also be run at the slowest specified cycle rates. Each device in the characterization sample should be screened for pattern sensitivities at the four (4) corners of the V_{DD} and V_{BB} power supplies and at the specified temperature extremes. The test procedure should be such that all test patterns are tried on each device regardless of previous test pattern failures for the device under test with the test conditions recorded on all failures. Because of test time constraints it should be sufficient to run the longer N^2 pattern tests such as galpat on a sample of a few hundred devices covering a wide range of process parameters, while screening a larger sample of devices to the remaining pattern tests. By analyzing the data gathered from the test described, it should be possible to define a set of test patterns and conditions that is optimal in terms of test time without sacrificing test integrity. The result of an optimized test flow is that pattern tests

are run only at the power supply voltage corners that have been identified as "worst case" for that pattern, and lengthy pattern sensitivity tests are utilized only when the device sensitivities that these patterns detect cannot be identified using shorter test patterns.

When sensitivities of a device to lengthy test pattern sequences are discovered, it is often possible to develop alternate test methods and patterns that result in dramatically reduced test times and are designed specifically to screen for device related failure modes. The development of such a procedure usually requires that the failure mechanism be well understood in relation to the particular device design.

A successful example of a test procedure developed to screen for a particular device sensitivity is presently being used in the production testing of one 4K RAM device. During the characterization of this device a sensitivity to a disturb type of pattern was discovered. The pattern used consisted of writing the full memory with "1's" followed by writing a "0" two thousand times at the base location. The entire memory, excluding the base cell, was then read checking for an all "1's" pattern. The base location was then written to a "1" and the entire procedure repeated with the base cell incrementing through all possible memory locations. Assuming a 500ns cycle rate, the test time for this sequence was greater than 20 seconds. Initial investigation of the problem revealed that after each base cell had been written 2000 times it was necessary to read only the column of the base location instead of the entire array in order to generate the failure mechanism, which reduced the test time to 4 seconds. Upon further investigation it was found that the failures were caused by voltages slightly in excess of the device threshold voltage being coupled onto the row select line connected to the gates of the one transistor storage cells for that row. Since the base cell on the failing column was repeatedly being written to a "0" causing the column digit bus to be low each cycle, the voltage coupled onto the failing row was sufficient to cause the stored "1" level on the failing cell to be discharged through the cell transistor somewhat each cycle. When enough disturb cycles had occurred to discharge the cell sufficiently, the failure resulted. Since the failure mechanism is highly dependent on the threshold voltage of the cell transistor which varies as a function of the V_{BB} supply voltage, it was possible to reduce the number of disturb write cycles of the base location required from 2000 to 100 cycles by implementing the test at a V_{BB} supply voltage 0.5 volts more positive than the specification normally allows, further reducing the test time requirement to approximately 200 milliseconds. In order to prevent an unnecessary yield loss due to the abnormal supply voltage conditions, a relaxation of the input "0" voltage level was required for the test.

PRODUCTION-TESTING

Once the initial 16K RAM device characterization is completed enough data concerning the characteristics and sensitivities of the particular design should be available to establish a logical and comprehensive production test sequence. Since single temperature production testing is economically desirable, the characterization data must be analyzed for the feasibility of insuring that all devices' specifications are met over the entire operating temperating range for the device while testing at a single temperature. The high temperature extreme virtually always proves to be the only practical choice for a single test temperature because of refresh and parameter margin characteristics of 16K dynamic RAMs. The "worst case" condition for pattern sensitivities power supply margins and timing parameters is typically at high temperatures, but the lower temperature limits can be "worst case" for some device parameters such as input levels and power dissipation. For the device parameters that prove to be the "worst case" at the lower temperature extreme, it should be possible to determine the proper guardbands to be used for high temperature testing from the characterization data.

An important factor which is too often not thoroughly comprehended in establishing the production test conditions for high performance 16K dynamic RAMs is the characteristics and limitations of the production test equipment to be utilized. As discussed previously, tester timing skews of as little as ± 1 ns can be significant and cause severe correlation problems considering the large number of critical input timing specifications relative to the clock inputs for 16K RAMs. Because of variables such as internal tester clocks, skews, cables to remote temperature handlers, and individual driver characteristics, controlling input timing skews to a tighter specification often proves to be impractical. Fortunately, however, for most 16K dynamic RAM designs, virtually all critical input timing parameters track the column access time of the device as a relatively constant percentage, and by analyzing the device characterization data a correlation factor for each input timing parameter relative to column access time can usually be established. Since the specified column access times, even for higher performance 16K dynamic RAMs, is a relatively large value (typically 90ns or greater), a ± 2 ns maximum total measurement error is of much less significance. Therefore for most 16K RAM designs, testing for the proper column access times on each device and relaxing the programmed test conditions on input timing signals by a few nanoseconds so that even "worst case" tester timing skews will not violate the specified device limits is sufficient to guarantee that all device timing specifications are met without causing severe tester correlation problems.

The problems associated with variations in signal integrity and noise are usually among the most difficult test equipment related problems to be addressed in 16K dynamic RAM testing. The maximum effort practical should be extended to insure that the integrity of the signals applied to the device under test are the best possible, but often even this does not prevent noise related tester correlation problems. For most 16K dynamic RAMs, test equipment noise related failures occur when noise transients on the input signals at the device during functional testing exceed the "worst case" specified input logic level voltages for that device. Unless the noise levels are excessive, relaxing the programmed dc input voltage levels usually eliminates most failures of this type, but may not be desirable if input voltage level specifications for the device are to be guaranteed. Even though it is not always possible to eliminate noise related device failures when testing for "worst case" input voltage levels, it is possible to separate potential noise related failures by running a portion of the test patterns for each V_{BB} and V_{DD} power supply voltage corner tested at relaxed dc input levels and then change the input voltage levels to the specified "worst

case" limits for the remaining test patterns at that supply voltage. Devices which pass relaxed input levels tests and then fail when the specification dc limits are applied can be placed through the test program software into a separate physical bin. Devices in this bin would then require further analysis in order to determine if the failures were device or noise related.

CONCLUSION

In order to establish test conditions for higher speed 16K dynamic RAMs that are effective and economical, the particular characteristics and sensitivities of both the device and production test equipment to be utilized must be understood. Test flows that are optimized for the particular characteristics of a 16K RAM design can result in dramatic savings in production testing costs without sacrifices in test integrity. However, economic success of an optimized 16K dynamic RAM test flow depends upon performing a thorough and lengthy device characterization and the choice of a design that is not sensitive to a wide variety of complex test conditions.

MOSTEK®

16K- THE NEW GENERATION DYNAMIC RAM Technical Brief

DYNAMIC
RAMS

Extensive design effort has been expended in the development of 16K RAMs to insure that many of the problems and peculiarities of the previous generation RAMs (1K's and 4K's) have been eliminated. This paper will show how such undesirable device characteristics as excessive power dissipation, inadequate noise margins (at the input and output terminals), restrictive timing, and unexplained "soft errors", have all been designed out of the new generation 16K dynamic RAMs.

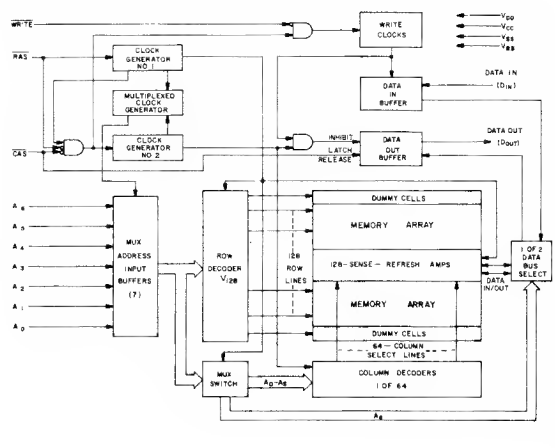
Looking back at some of the popular MOS RAMs of the early 1970's, one cannot help but remember the many different device configurations, each with its own peculiar operating modes and timing restrictions. Memory devices have emerged which require multiphase, high level clocks and others with multiplexed address inputs and/or multiplexed I/O. With a strong move towards standardization, the semiconductor memory industry is in a much more fortunate situation with 16K RAMs than with any previous memory product. Never before could the user experience such numerous benefits from a single memory device.

16K Technology Overview

Before delving into the user benefits and features of 16K RAMs, it is first necessary to take a look at two of the most important, yet most often ignored aspects of a device - chip architecture and process. These two elements combine to serve as a reference point for comparing any LSI device to a similar one, and for establishing a device as a "state-of-the-art" product.

MK 4116 FUNCTIONAL DIAGRAM

Figure 1.



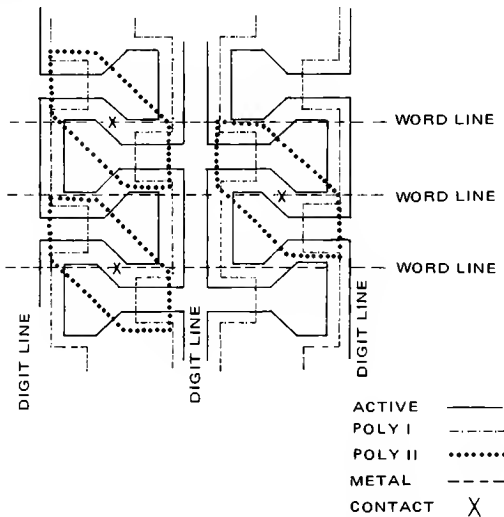
The block diagram (functional layout) of the MOSTEK MK 4116 appears in Figure 1. The chip is organized internally as two 8K sub-arrays which form a single 128x128 balanced array. The column decoder and sense-refresh amplifiers are in the middle of the matrix and "dummy cells" are located at each side. The "dummy cells" establish a voltage reference for the balanced sense amplifiers. One of the array halves inverts data and will store an input "one" as a low level in the storage cell (a second inversion is performed by the output circuitry so that this internal inversion is not seen at the device terminals). The control circuitry surrounding the array is controlled by networks of clock generators which are activated by the externally applied Row and Column Address Strobe (RAS and CAS) signals. Access time is determined exclusively by clock delays internal to the circuit and is influenced only by influencing these internal delays. This design feature can greatly impact testing since there is no reason to search for a test sequence or data pattern which is worst-case for access time. As a final comment, note that the address input buffers are multiplexed between row and column addresses while the row and column decoders are independent circuits. This greatly reduces the input capacitance at these terminals over previous multiplexed RAMs where each address pin was connected to two input buffer circuits.

As with most 16K RAM devices, the MOSTEK MK 4116 is fabricated with a two level N-channel polysilicon gate process and a single transistor dynamic storage cell. The two level polysilicon process greatly enhances circuit density without a substantial increase in process complexity over the standard single level N-channel polysilicon process. Both processes, however, allow independent adjustment of gate and field oxide thresholds by ion-implantation which maximizes performance, density, and reliability.

The layout of the storage cell in the MK 4116 is shown in Figure 2. This is a conventional one-transistor dynamic storage cell implemented with MOSTEK's double-level polysilicon (Poly II) process. The row (word) select lines are metal, eliminating concern over propagation delays down the long (80 mil) word lines. Data transfer to and from the cell is through the diffused column (digit) lines. The top plate of the storage capacitor is VDD (first level of polysilicon) which allows charge to be stored in the depleted region beneath this level. Metal word lines contact the second poly level which forms the gate of the transfer device isolating the storage cell from the digit line. The cell is relatively insensitive to variations in the doping level of both first and second poly. In fact, performance of the cell is primarily influenced by junction depth, oxide thickness, and mask geometry, all parameters which tend to remain constant.

MK 4116 CELL LAYOUT

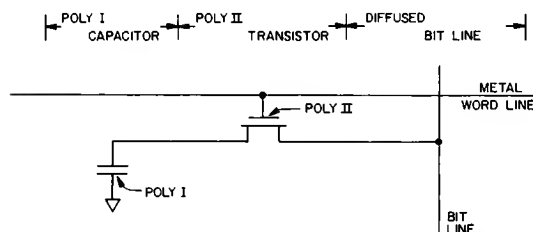
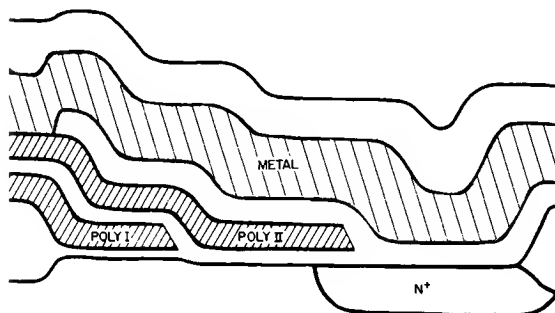
Figure 2.



A cross section of a single storage cell is shown in Figure 3. Using the standard silicon gate process this cell would be made of two elements—the pass transistor and a storage capacitor. However, because of the use of two levels of poly-silicon, no layout space is required to separate these components and, therefore, should be regarded as one component only. Actual dimensions of the double-poly cell are approximately $14.5 \mu\text{m} \times 30 \mu\text{m}$. It is estimated that by the end of 1977, further refinements of the basic five mask Poly II* process technology will produce 16K RAM devices with an overall chip area less than 18,000 mil².

MK 4116 CELL AND CROSS-SECTION

Figure 3.



* Actually, the Poly II process uses a total of seven mask steps. However, only five mask steps are required to define the product; the other two are very non-critical mask operations which enhance device reliability and improve yield.

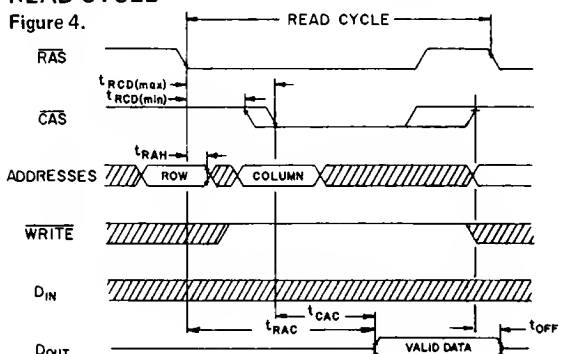
Timing Considerations

Although the multiplexed address 16K RAM requires two strobe signals ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$) for control purposes, the timing of these clocks is very flexible when compared to the original multiplexed RAM introduced in 1973. The original design made no allowances for the additional time required to perform the address multiplexing. Also, since the internal $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clock generators functioned totally independent of one another, several unnecessary restrictions were put on the "precharge" and "refresh" operations. Several 16K RAM designs (including MOSTEK's MK 4116) have overcome these timing inconveniences by enhancing the operation of the internal clock generators and implementing a feature called "gated $\overline{\text{CAS}}$ ".

The inclusion of the "gated $\overline{\text{CAS}}$ " feature allows for more flexible timing on the RAS to CAS delay time specification so that the system designer can compensate for timing skews and "uncertainties" that may be encountered in the multiplexing operation (refer to Figure 4).

READ CYCLE

Figure 4.

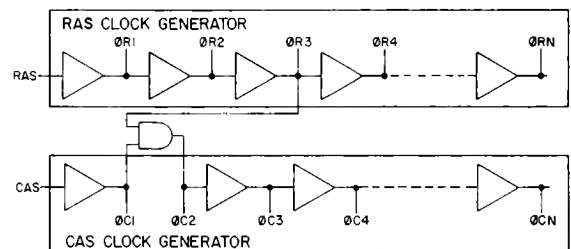


NOTE: D_{OUT} occurs at access time and remains valid while $\overline{\text{CAS}}$ is active.

Each of the control signals, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains, as illustrated in Figure 5, are linked together logically such that the address multiplexing operation is done outside of the critical path timing sequence for read data access.

GATED INTERNAL CLOCK CIRCUITRY

Figure 5.

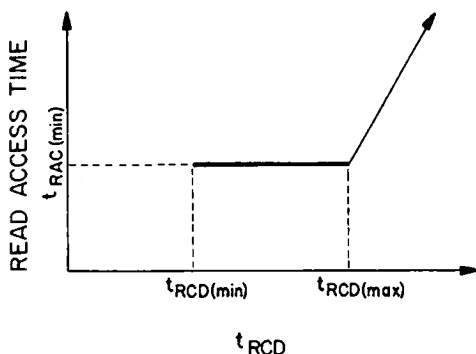


The later events in the $\overline{\text{CAS}}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{\text{RAS}}$ clock chain. This "gated CAS " feature allows the $\overline{\text{CAS}}$ clock to be externally activated as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from Row Address to Column Address information.

Note that $\overline{\text{CAS}}$ can be activated at any time after t_{RAH} and it will have no effect on the worst-case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing end-points result from the internal gating of $\overline{\text{CAS}}$ which are called $t_{\text{RCD}}(\text{min})$ and $t_{\text{RCD}}(\text{max})$. No data storage or reading errors will result if $\overline{\text{CAS}}$ is applied to the device at a point in time beyond the $t_{\text{RCD}}(\text{max})$ limit. However, access time will then be determined exclusively by the access time from $\overline{\text{CAS}}$ (t_{CAC}) rather than from $\overline{\text{RAS}}$ (t_{RAC}), and access time from $\overline{\text{RAS}}$ will be lengthened by the amount that t_{RCD} exceeds the $t_{\text{RCD}}(\text{max})$ limit. This relationship is depicted in Figure 6.

GATED CAS TIMING RELATIONSHIP

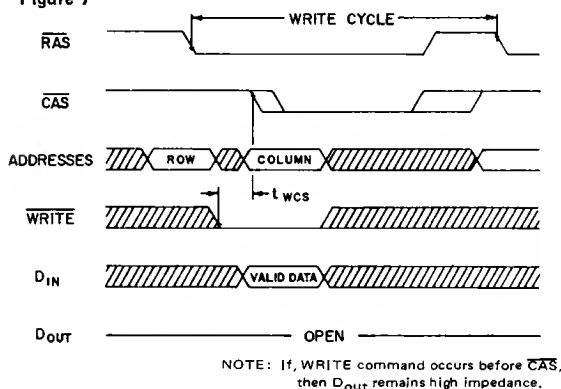
Figure 6.



Also, as a result of the intertwined clock generators, precharge of all internal circuitry is initiated by $\overline{\text{RAS}}$ going to the inactive state. This removes several timing restrictions from the trailing edge of $\overline{\text{CAS}}$, allowing the simplified "RAS only" refresh operation as well as improved operation of the Data Output.

WRITE CYCLE

Figure 7



Basically, Data Out of the "unlatched" type of 16K RAM is valid within the specified access time and will remain valid until the Column Address Strobe ($\overline{\text{CAS}}$) is taken to the inactive state. However, in early write cycles ($\overline{\text{WRITE}}$ active low before $\overline{\text{CAS}}$ goes low, see Figure 7) the data output will remain in the high impedance (open-circuit) state throughout the entire cycle. This type of output operation results in some very significant system implications.

Common I/O Operation — If all write operations are handled in the "early write" mode, then D_{IN} can be connected directly to D_{OUT} for a common I/O data bus.

Data Output Control — D_{OUT} will remain valid during a read cycle from t_{CAC} until $\overline{\text{CAS}}$ goes back to a high level (precharge), allowing data to remain valid from one cycle up until a new memory cycle begins with no penalty in cycle time. This makes the $\overline{\text{RAS}}/\overline{\text{CAS}}$ clock timing relationship very flexible.

Two Methods of Chip Selection — Since D_{OUT} is not latched, $\overline{\text{CAS}}$ and/or $\overline{\text{RAS}}$ can be decoded for chip selection. If both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are decoded, then a two dimensional (X,Y) chip select array can be realized.

Noise Margins

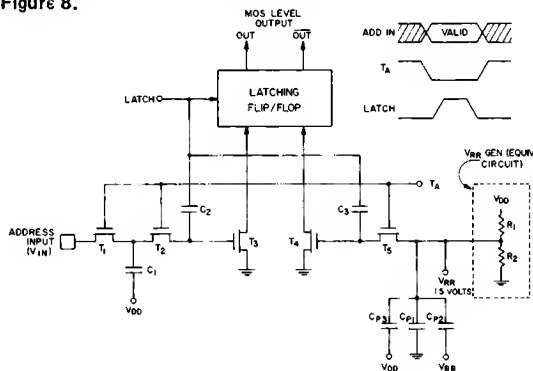
The ability of an MOS memory device to interface with logic families outside its own has always been a marginal situation. With the new generation 16K RAM, the problems of high capacitance, high level address inputs have been eliminated along with the old familiar design glitch which caused the address inputs of several popular RAM types to source current out of their input terminals. As veteran designers might recall, this condition injected a significant current spike on the address lines which decreased noise margin and prevented the use of Schottky address drivers in the system. To overcome these problems in 16K RAM design means, that for the first time, MOS memory elements can be surrounded by high performance logic families (Schottky TTL) in the system to achieve maximum performance with adequate noise margins.

To provide wide operating margins and noise immunity desired by users, a special input stage has been incorporated into the MK 4116 to detect true TTL input levels. A circuit schematic of this stage is shown in Figure 8. The principle behind this circuit is a simple differential amplifier which compares the incoming TTL level to an on-chip 1.5 volt reference level. This type of circuit can be designed to detect "one" levels greater than or equal to 2.2 volts and "zero" levels less than or equal to 0.8 volts.

In the circuit in Figure 8, a positive common mode voltage boost is capacitively coupled to the gates of transistors T3 and T4 to assure that at least one of them is turned on when the "latch" command is initiated from the control clock generator. Note that the input buffer will latch properly even though both the input and reference voltages may be less than the device threshold voltage. The addition of T1 and C1 in the V_{IN} path helps to increase the amount of negative undershoot on V_{IN} which can be tolerated between the time TA goes low and the time the latching action takes place. This type of input circuit

MK 4116 ADDRESS INPUT BUFFER

Figure 8.



requires the shortest possible address hold times and allows the input circuitry to function independent of device thresholds and other process parameters.

The output drive capability of a RAM is also a very important area of concern. Many times the load circuit which a vendor uses to measure the access time of a device is not representative of typical system loading conditions. If actual system loading is much greater than the load used by the manufacturer to measure access time, then the device will be marginal in the system. With typical system capacitance loading far in excess of 60pF, it is necessary for the new generation 16K RAMs to accommodate two TTL loads in addition to driving 100pF capacitance.

Power Dissipation

A major breakthrough in the reduction of active power dissipation in dynamic RAMs results from the use of dynamic circuitry throughout the entire device, specifically in the sense amplifiers. Without going into a detailed discussion of dynamic RAM design, it will suffice to say that dynamic flipflop type level detector is made possible by providing an access path to both the true and complement sense lines associated with each amplifier. This sense amplifier configuration does not require digit pull-up transistors which are the major source of active power dissipation in a dynamic RAM. Figure 9 is a comparison of the current waveforms (characteristics) of two similar RAMs, one incorporating the dynamic sensing approach and the other using static loads in the sense amp circuits.

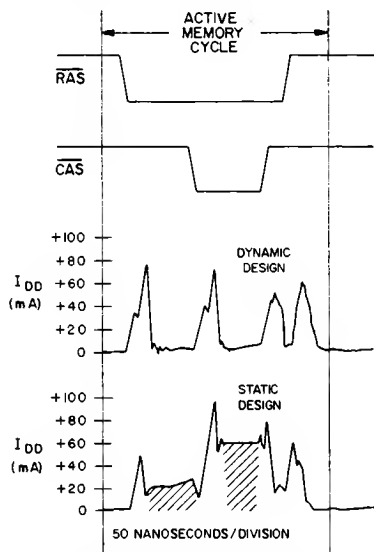
The user benefits derived from RAMs designed with dynamic sense amplifiers extends far beyond a simple reduction of the power dissipation. Although low power is of significant importance, even more important is the increased inherent reliability (which will be discussed later) and the impact that the dynamic current characteristics have on system design.

Since most of the power drawn by the MK 4116 is the result of an address strobe transition, the dynamic power is primarily a function of operating frequency rather than active duty cycle (as is the case with "static" sense amp designs). This dynamic current characteristic precludes inadvertent burn-out of the device in the event that the clock inputs become shorted to ground due to system

malfunction. With the old conventional design, maximum current is drawn by the device any time the strobe inputs are activated. This is the reason that many of the previous generation RAMs had restrictions on the maximum time the chip enable strobe could remain active.

STATIC VS. DYNAMIC SENSE AMP CHARACTERISTICS

Figure 9.



SUPPLY CURRENT VS. CYCLE RATE

Figure 10.

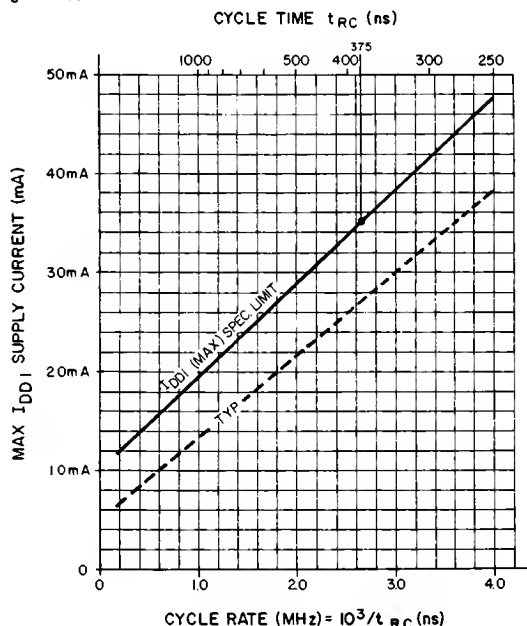


Fig. 10 Maximum I_{DD1} versus cycle rate for device operation at various frequencies. I_{DD1} (max) curve is defined by the equation:

$$I_{DD1} \text{ (max) [mA]} = 10 + 9.4 \times \text{cycle rate [MHz]}.$$

Not only does the dynamic current characteristic of this device prevent inadvertent burnout, it also allows the manufacturer of such devices to specify the operating power as a function of frequency rather than by a "fixed" condition. As illustrated in Figure 10, this allows the system designer to have a worst-case power specification, guaranteed by the manufacturer, which applies to real "use" conditions.

System Reliability

Reliability is certainly not a new buzz word in the MOS memory market. Reliability (or in some cases, the lack of it) has been an important topic for many years. As most of the "old-timers" will recall, many of the 1K and early 4K dynamic RAMs exhibited a phenomenon known as "soft failures" that drove even the experts into a state of panic. As 4K RAMs matured it became apparent that something had to be done to improve the reliability of dynamic RAMs and restore the credibility of the manufacturers before the advent of 16K devices.

In evaluating the problems of system reliability, it has been determined that there exists a strong correlation between memory devices which exhibit "soft failures" in systems and memory devices which are intolerant of power supply noise and/or marginal input levels. Discrete device testing may prove that the RAM is functional and meets all specifications; however, what is important to the user is the "real" system environment.

The new 16K RAM devices have overcome the problems associated with power supply noise by insuring proper operation over a wider power supply range — $\pm 10\%$ rather than $\pm 5\%$.

The basic nature of a dynamic RAM is such that the current drawn by the device during an active cycle can be several orders of magnitude greater than the current drawn while the device is in standby. This sudden change in current requirement can create seemingly incurable noise problems within a system if proper decoupling is not implemented.

Although no particular power supply noise restriction exists other than the supply voltages remain within the specified limits, adequate decoupling should be provided to suppress high frequency noise resulting from the transient current of the new 16K RAM devices. This insures optimum system performance and reliability. Bulk capacitance requirements are minimal since the MK 4116 draws very little steady state (DC) current. This characteristic of the 16K RAM can greatly reduce the expense and complexity of power supply design. This is especially important when costs of \$1 to \$1.50/watt are common for a good, quality power subsystem.

In addition to operating margin, memory component power consumption is also a major factor affecting reliability. As described earlier, the technology used to manufacture 16K RAMS produces low power devices which generate little heat and are less prone to failures induced by high temperature. Remember, system reliability is inversely proportional to operating temperature.

CONCLUSION

The new generation 16K RAM devices come closer to answering the needs and addressing the complaints of semiconductor memory users than any previous Random Access Memory Product. These emerging 16K RAM devices are designed and manufactured with the latest state-of-the-art processing techniques; one which requires few devices per memory cell; has simple, easily controlled, mature processing techniques, requires minimal, simple peripheral circuitry; dissipates little power; is free of intrinsic reliability problems; and is manufactured by responsible, careful, and experienced vendors.

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MOSTEK®

PRINTED CIRCUIT BOARD LAYOUTS FOR THE COMPATIBLE DYNAMIC RAM FAMILY Technology Brief

INTRODUCTION

In the past several years dynamic RAMs have dominated the large memory system marketplace. As new RAMs have been introduced, they have forced some users to redesign their memory boards to accommodate the new features and increased density. As a leader in dynamic RAM technology, Mostek has attempted to alleviate this redesign need by introducing a compatibility family concept in the N-bit by 1 dynamic RAM area. As new RAMs are introduced, they are packaged in the same pinout, or in a pinout which is so similar, that the changes between packages are minimized. Thus, increases in the density and function of the RAMs have been incorporated into existing systems without major redesign efforts. Memory systems can be designed to allow the interchange of 4K, 16K, 32K, 64K and 128K bit dynamic RAMs.

The key to the family concept of dynamic RAMs is based on address multiplexing. Mostek pioneered the multiplexed address dynamic RAM with the introduction of a 4096 bit, 16-pin DRAM in 1973. Many members of the memory

community felt that multiplexed addressing would not survive. Not only has the multiplexed address DRAM survived, it has become the industry standard for the 16K RAM, as well as for the next generation MK4164, 65536 bit DRAM.

Mostek has extended the address multiplexed dynamic RAM (DRAM) compatible family by offering double density DRAMs by using advanced packaging techniques. The double density DRAMs are constructed by mounting two leadless chip carriers on a single 18 pin substrate. The 18-pin package is pin compatible with its 16-pin counterpart, with the addition of two lower pins for the row and column select controls that access the second chip carrier device. This advanced package concept allows extension of memory density with the current technology devices until the next generation of devices become available and cost effective. When the next generation of devices become available, they can be packaged in a similar manner, to provide even higher density in the double density package. The 16/18-pin compatibility RAM family is shown in Figure 1.

DYNAMIC
RAMS

MOSTEK'S COMPATIBLE RAM CONCEPT PIN OUT TABLE

Figure 1

4526	4154	4532	4515	4332	4115	4027		4027	4115	4332	4516	4532	4164	4526
126K	54K	32K	16K	32K	16K	4K		4K	16K	32K	16K	32K	64K	126K
(5V)	(5V)	(5V)	(5V)								(5V)	(5V)	(5V)	(5V)
RFSH	RFSH	RFSH	RFSH	V66	V66	V66	1 (1)	VSS	VSS	VSS	VSS	VSS	VSS	VSS
DIN	DIN	DIN	DIN	DIN	DIN	DIN	2 (2)	CAS	CAS	CAS1	CAS	CAS1	CAS	CAS1
WRITE	WRITE	WRITE	WRITE	WRITE	WRITE	WRITE	3 (3)	DOUT	DOUT	DOUT	DOUT	DOUT	DOUT	DOUT
RAS1	RAS	RAS1	RAS	RAS1	RAS	RAS	4 (4)	CS	A6	A6	A6	A6	A6	A6
A0	A0	A0	A0	A0	A0	A0	5 (5)	A3	A3	A3	A3	A3	A3	A3
A2	A2	A2	A2	A2	A2	A2	6 (6)	A4	A4	A4	A4	A4	A4	A4
A1	A1	A1	A1	A1	A1	A1	7 (7)	A5	A5	A5	A5	A5	A5	A5
VCC	VCC	VCC	VCC	VDD	VDD	VDD	8 (6)	VCC	VCC	VCC			A7	A7
RAS2		RAS2		RAS2			(9)			CAS2		CAS2		CAS2
							(10)							

Parentheses Indicate Pin Number of 16 Pin Packages. 16 Pin Devices are Upper Justified in 16 Pin Socket

Differences between the RAMs in this compatible family, as well as techniques for designing memory boards which are useable across the family, will be presented as an aid to designers who are using present generation dynamic RAMs and are planning for future expansion.

The RAMs which will be considered include the following:

- MK4116 — 16K Three Supply DRAM
- MK4332 — 32K Three Supply DRAM
- MK4516 — 16K +5 Volt Only DRAM
- MK4532 — 32K +5 Volt Only DRAM (Double Density MK4516)
- MK4164 — 64K +5 Volt Only DRAM
- MK4528 — 128K +5 Volt Only DRAM (Double Density MK4164)

Some of these devices are not currently available. They demonstrate the expandability and memory system design versatility offered by the memory family concept.

Three different compatibility concepts will be discussed to indicate how a memory board can be designed to accommodate different members of the dynamic compatible family, including both the 16-pin and the 18-pin packages. These will be considered as three possible printed circuit layouts as follows:

1. Board compatibility for the three supply members only. These include the MK4116 and the MK4332.
2. Board compatibility for the +5 volt only family members. These include the MK4516, MK4532, MK4164, and the MK4528.
3. Board compatibility for both the single supply (+5 volt) members, as well as the three supply devices, a board design that offers complete compatibility across Mostek's compatible dynamic RAM family.

Multilayer boards to support the different devices are relatively easy to design and will not be discussed. Although many of the recommendations apply to multilayer design, it should be noted that the use of multilayer boards does not preclude the need for careful board layout and circuit/logic design consistent with good engineering practices. Double sided PC boards that will accept numerous members of the compatible family are generally much more difficult to design. However, they are commonly used with dynamic RAMs and can demonstrate adequate margins when properly designed.

In order to design a memory board that is compatible across the complete family or within a subset of the compatible family, it is necessary to understand the fundamental differences between the members of the DRAM family. The five basic areas where the RAMs differ are given below (See Figure 1.):

1. Power supplies — The 16-pin MK4116 and the MK4332 require a three supply power system with +5V, +12, and -5V. The remainder of the RAMs (MK4516, MK4532, MK4164, and the MK4528) require a single +5 volt supply.

2. Addresses — The 16-pin MK4164 (Pin 9) and the 18-pin MK4528 (Pin 11) require an additional address pin to accommodate the increase in RAM density. A7 is used for this purpose. This pin is a N/C (No Connect, Not Bonded) on the MK4516/MK4532 and is used for V_{CC} (+5 volts) on the MK4116/MK4332.

3. \overline{RAS} and \overline{CAS} — The double density packages (MK4332, MK4532 and the MK4528) require an additional $\overline{RAS}/\overline{CAS}$ pair (Pins 9 and 10) of strobe signals to select the second chip on the package. These are connected to the extra two pins located at the lower end of the package.

4. Pin 1 Refresh — The new technology parts (MK4516, MK4532, MK4164 and the MK4528) have an on-chip circuit which simplifies the refreshing operation and reduces the battery-backup power requirements. Refreshing is accomplished by strobing pin 1 active low at the appropriate time. With this feature, the refresh address is provided on-chip, resulting in lower system support circuitry chip count and lower power requirements. If this function is not used, pin 1 may be allowed to float, but it is highly recommended that pull-up resistors to +5 volts be used to guarantee a solid high level (inactive state). The three supply DRAMs do not have the pin 1 refresh feature and this pin is used to provide the V_{BB} connection.

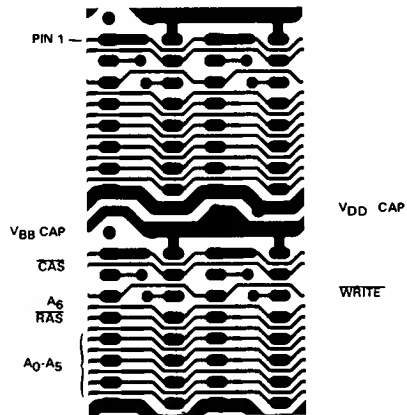
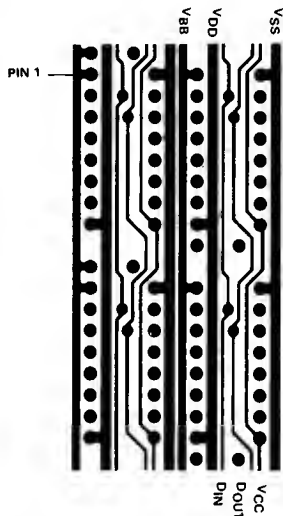
5. V_{CC} Location — The single +5 volt parts have V_{CC} connection on a different pin than the three supply parts. In actuality, the primary power pin (Drain Supply) has remained unchanged, but the supply requirement has changed from +12 volts to +5 volts.

MK4116/MK4332 Compatible Board Layout

The layout shown in Figure 2 has been used successfully with both the older 4096 bit RAM, the MK4096/MK4027 and the 16K RAM, the MK4116. If the user has experience with this layout and confidence in using it, it is possible to modify it to accept the double density MK4332 DRAM. Two additional pins must be added to the lower end of each device site to provide the additional \overline{RAS} and \overline{CAS} strobe signals required to select the second half of the double density package.

Note that the additional \overline{RAS} and \overline{CAS} strobe signals do not require an increase in the vertical spacing (300 Mils) between the rows of RAMs even though the bottom two pins are used for signal traces instead of power. The vertical spacing can remain at 300 Mils as previously shown with the 16-pin layout. However, the 18-pin layout does require .05 square inches more area per RAM than required with the 16-pin layout.

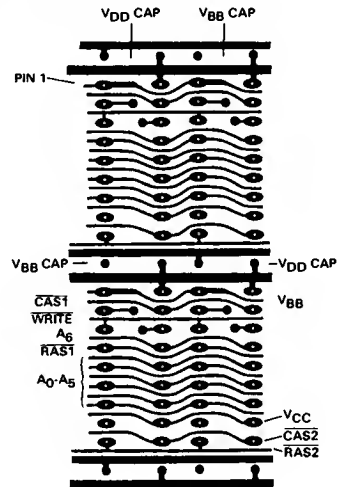
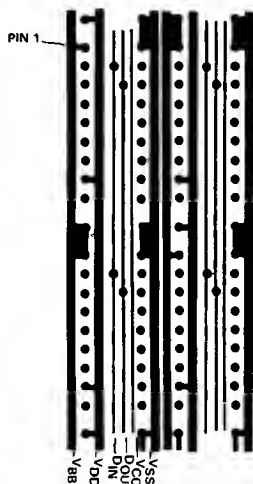
18 PIN MK4116/MK4332 COMPATIBLE LAYOUT (MODIFICATION OF LAYOUT SHOWN IN FIGURE 2)
Figure 2



Frequently used layout for 16 pin 3 supply address multiplexed Dynamic RAMs

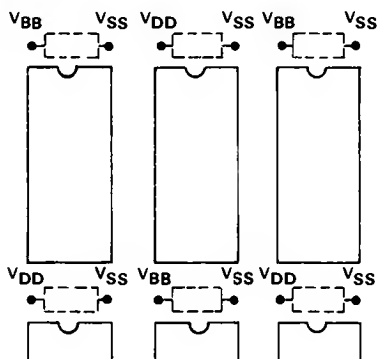
(SIMPLIFICATION OF 18 PIN LAYOUT)

Figure 3



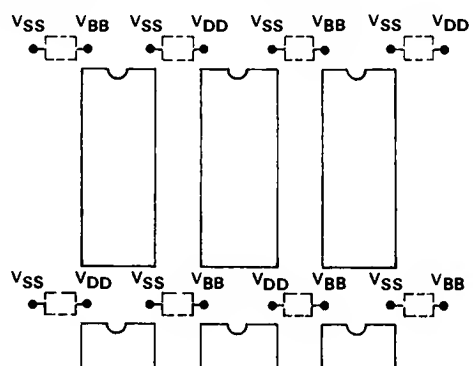
CAPS PLACED ON 300 MIL SPACING

Figure 4A



CAPS PLACED ON 200 MIL SPACING

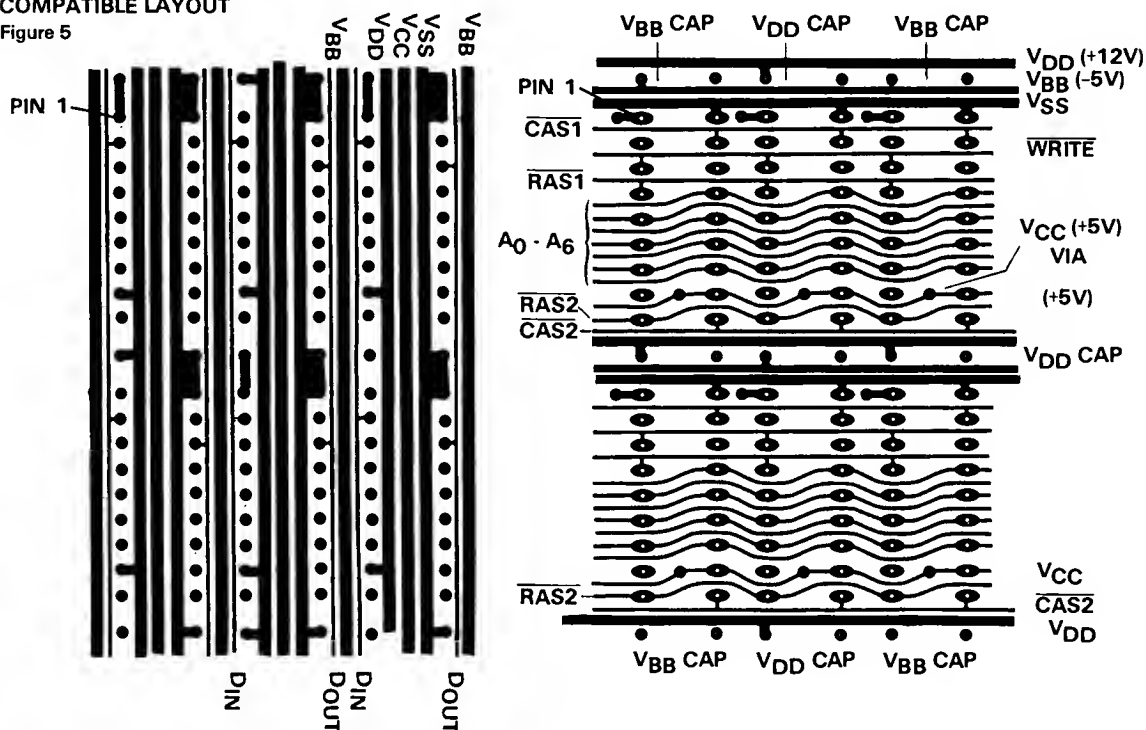
Figure 4B



**DYNAMIC
RAMS**

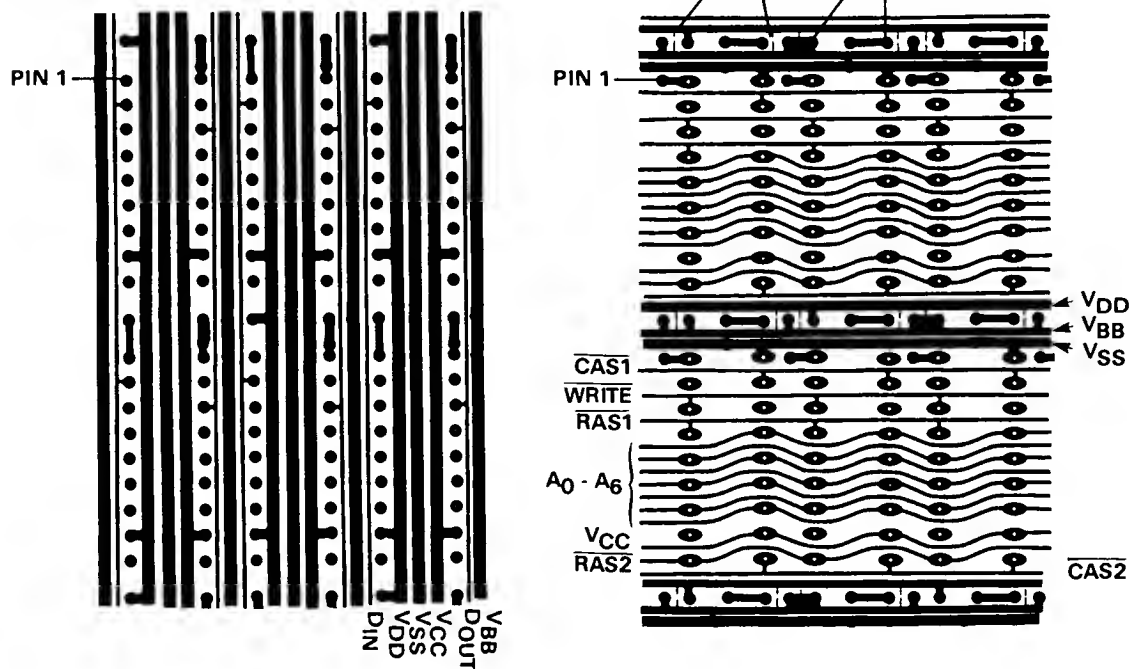
3 SUPPLY/SINGLE SUPPLY COMPATIBLE LAYOUT

Figure 5



MK4116/MK4332 COMPATIBLE PCB LAYOUT

Figure 6



The 18 pin version of basic layout shown in Figure 2 can be modified to eliminate the geometric complexity of the metal traces. The simplified layout is shown in Figure 3. The capacitors have been relocated to the center of the horizontal power bus channel and have been aligned directly above the memory devices. This arrangement allows the use of capacitors with either 300 Mil or 200 Mil lead spacing. For 300 Mil spacing, the caps are inserted directly above the IC locations (See Figure 4A) and for 200 Mil lead spacing, the caps are inserted above the spacing between the IC locations (See Figure 4B). The relocation of the capacitors simplifies the routing of the vertical signals and the power traces and permits auto-insertion of the capacitors within the memory array matrix.

Figures 5 and 6 show the suggested MK4116/MK4332 compatible PCB layouts. These layouts are slight modifications of the layout shown in Figure 3. The vertical power bussing has been routed down the 300 Mil spacing under the IC and the data-in and data-out lines have been routed down the 200 Mil spacing between the IC sites. This arrangement results in a straight line routing of data lines and the elimination of feed throughs on these lines. Also, heavy vertical power busses will reduce the trace inductance and provide a substantial effective ground plane for the horizontal signal traces within the memory array.

The layout in Figure 5 and all subsequent layouts provide considerable isolation between data-out and data-in traces by running a decoupled supply or ground trace between them. The data-out to data-in coupling is generally not a problem,

except during late write cycles where transitions on the data-out line can cause perturbations on the data-in line if sufficient coupling between the two lines exists. This condition may cause a violation of either data-in setup times or data-in hold times during the write cycle. In most cases, this problem can be avoided by using time discrimination.

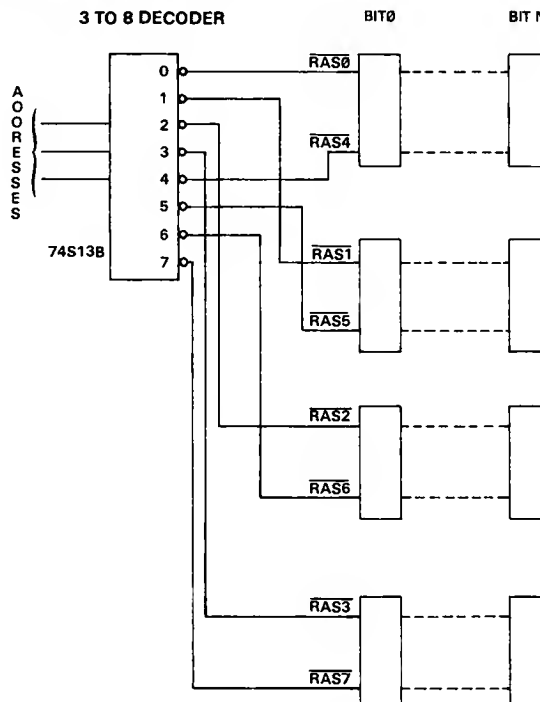
The layout shown in Figure 5 is preferred due to the direct connection of V_{DD} and V_{SS} to the RAM pins and the decoupling capacitors. Furthermore, the simplicity of the layout is very attractive. However, it does have the disadvantage of having a V_{CC} (+5 volt) VIA (Feed Through) under all RAM packages. The layout shown in Figures 2, 3 and 4 also have the VIAs under the RAMs. If feed throughs under ICs are prohibited in your design, Figure 6 shows a MK4116/MK4332 layout which eliminates them.

When using the layouts shown in Figures 3, 5 or 6 with the MK4116, the following considerations apply:

1. The 16-pin RAMs must be top justified in the 18-pin sites.
2. The address decoding logic must be designed to select on 16K boundaries and provide a \overline{RAS} signal to the RAM ($\overline{RAS1}$ on Pin 4). A $\overline{RAS2}$ signal will be ignored since nothing is connected to pin 9 of the 18-pin site when a MK4116 is used. It is recommended that \overline{RAS} decoding be used for the RAM selection.

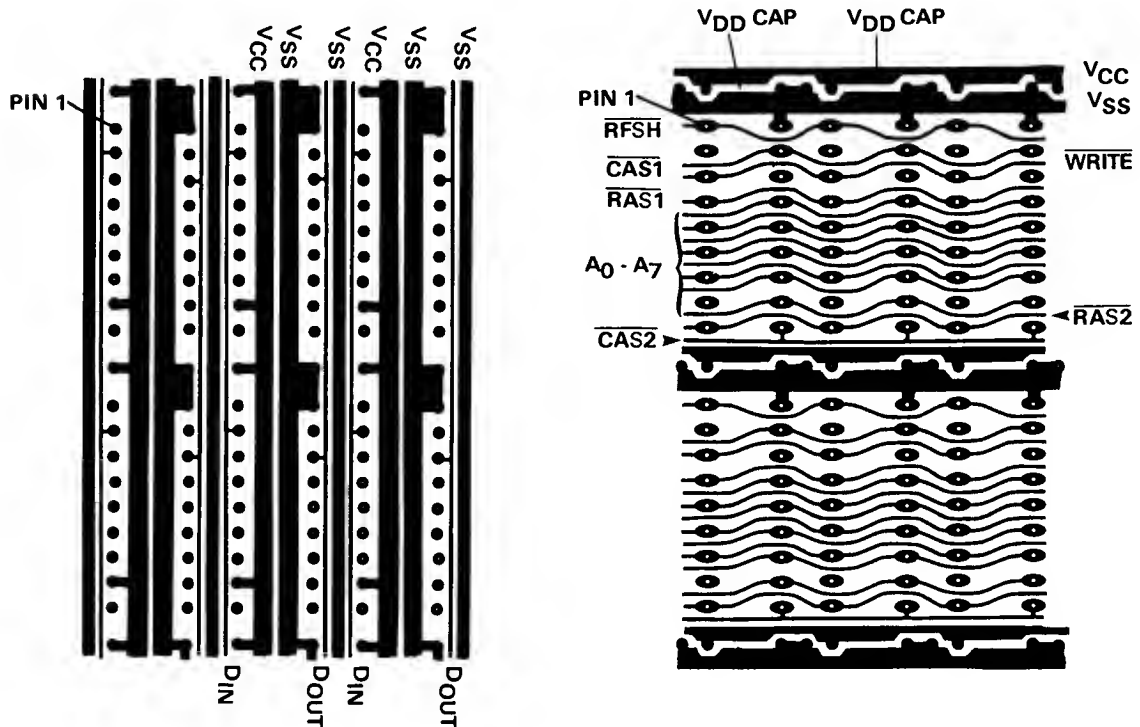
MK4516/MK4532/MK4164/MK4528 COMPATIBLE LAYOUT

Figure 7



MK4516/MK4532/MK4164/MK4528 COMPATIBLE LAYOUT

Figure 8



When using the layouts shown in Figures 3, 5 or 6 with the MK4332, these considerations apply:

1. The 18-pin devices are inserted directly into the 18-pin sites.
2. Since the 16K address boundary requirements for the MK4332 RAS decoding are identical to that for the MK4116, no major modifications are required for complete compatibility. The extra RAS and CAS inputs must be provided, based on 16K boundaries. This addition does not generally require jumper wires to handle the RAS clock. Figure 7 illustrates a method which can be used to avoid jumper wires in the RAS decoding logic. However, jumpers or switches are usually needed to adjust the board selection logic such that the memory subsystem acknowledges and responds to changes in memory density.
3. The power supply must provide the additional current needed to support the double density 32K devices.

MK4516/MK4532/MK4164/MK4528 Compatible PCB Layout

The use of the single +5 volt devices will require more demanding design efforts than those previously experienced

with the three supply devices, primarily because of considerations due to higher transient currents required by the +5 volt only devices.

Figure 8 shows the suggested PCB layout for compatibility across the single +5 volt high density compatible DRAM family. The power bussing has been made as heavy as possible to provide an effective ground plane and low inductance in the array power supply traces. The method used in Figure 8 to "beef up" the horizontal power traces may be used with the layouts shown previously (Figures 3, 5 and 6).

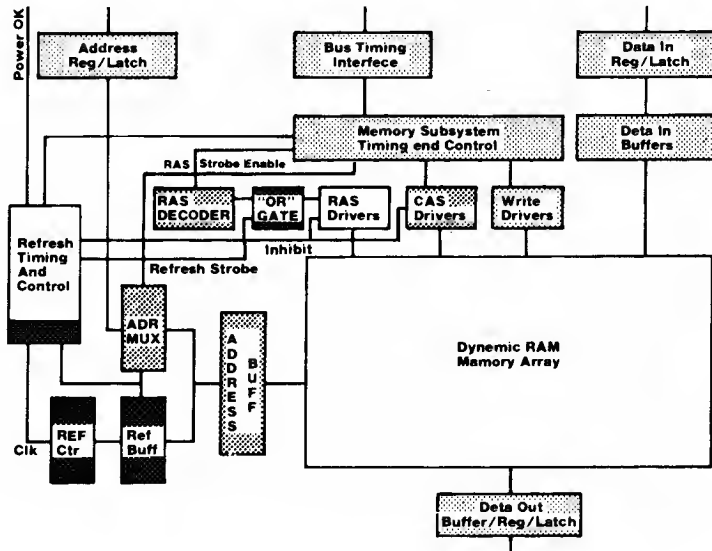
Since all of the single +5 volt high density compatible family members have the pin 1 refresh function, this layout will support the use of this feature without modification. (Pin 1 signal trace is included in Figure 8.) If the pin 1 refresh feature is not used, the signal trace should be pulled up to the inactive high state as previously discussed. The lower chip count and the reduced power requirements are illustrated in Figure 9 (Typical Memory Subsystem Block Diagram).

Complete Compatible Board Layout For The MK4116/MK4332/MK4516/MK4532/MK4164/MK4528

The previous examples have suggested how PCB layouts can

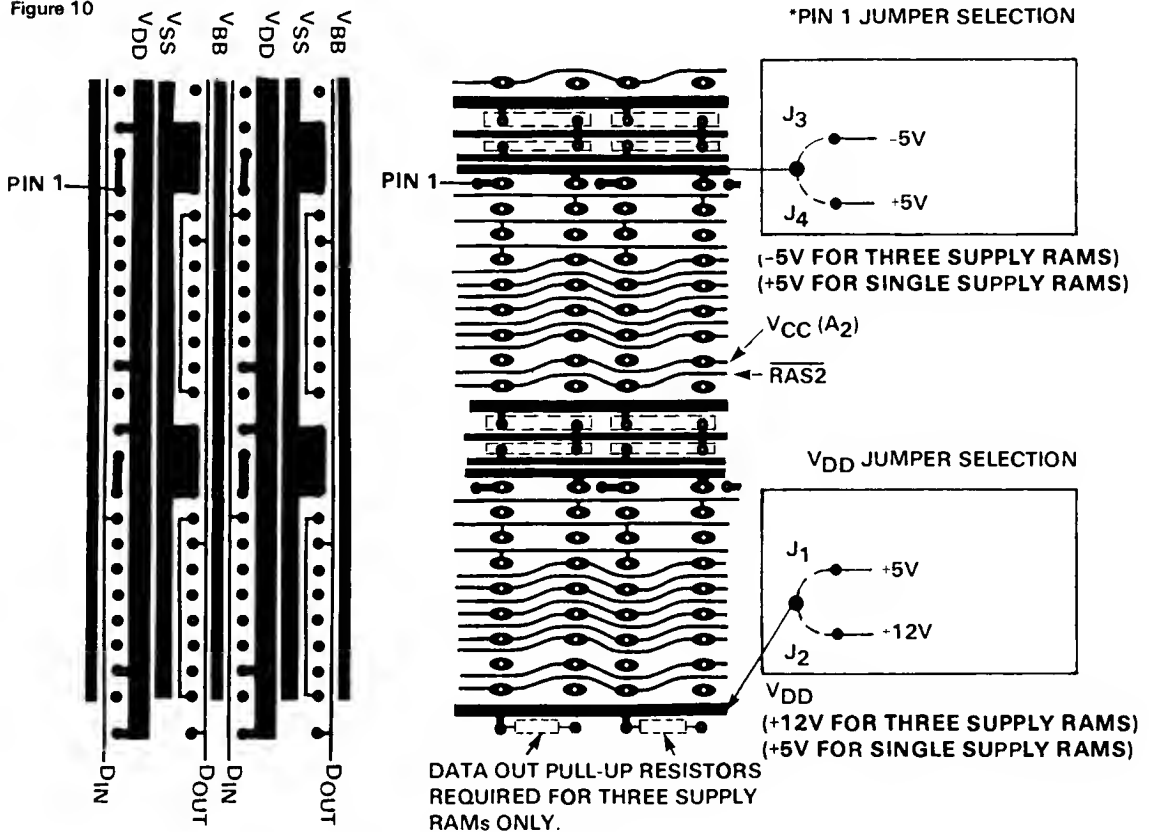
Figure 9

- ☐ Device powered down during RAS only RFSH
- ▨ Parts in addition to ☐ which can be powered down using Pin 1 RFSH
- Circuits not needed when using Pin 1 RFSH



DYNAMIC RAMS

Figure 10



accommodate either the three supply DRAMs (Figures 3, 5 or 6) or the single +5 volt devices (Figure B). That is, layouts to support one of the two basic subsets of the compatible DRAMs have been discussed, but a layout that will support all of the compatible devices on a common PCB layout has yet to be proposed. Figure 10 shows how the best features of the previous layouts can provide a layout for full compatibility across the entire family.

There are several notable features of this layout:

1. The V_{BB} , V_{DD} and V_{SS} power busses are very wide, to provide an effective ground plane and to reduce noise due to the transient currents. However, V_{CC} is provided by only a standard 15 Mil horizontal (signal) trace. Normally, the size of this trace could not provide the required V_{CC} level to the devices in the array. In normal operation, however, current is drawn from the V_{CC} supply only when data is being read from the RAM. Further, the current is required only when the data-out is a "1" (high level). In the multiple supply devices (MK4116/MK4332), the output can be treated as an open drain device by using pull-up resistors on the data-out port. The placement of these resistors is non-critical. The most convenient place is at the top or the bottom of the array. This method is feasible without sacrificing access time provided that interleaving is not done at the chip level within the array. The output data buffer circuitry is designed such that, at access time, the output will make a monotonic change from the high impedance state to a high for a "1" or from the high impedance state to a low for a "0". That is, glitches or spikes which would delay data access resulting from the RC time constant of the open drain configuration do not occur during a read operation. When using the MK4116 or the MK4528, the 15 Mil trace to pin 11 (used for V_{CC} with the three supply devices) becomes the A7 address line. If the MK4516 or MK4532 is used, this input does not function and may be allowed to "float". However, it is recommended that it be tied to a high or a low level to reduce noise within the array.

2. If the array layout has space limitations, the horizontal ground gridding at the bottom of the array may be excluded when interface circuits or critical ground current paths below the array do not exist. When eliminated, the power busses, including ground, should be extended under the bottom device to provide the ground plane effect for the signals to the bottom devices. (See Figure 10).

3. The second \overline{CAS} ($\overline{CAS2}$ on Pin 10) line for the double density devices is tied to the original \overline{CAS} line ($\overline{CAS1}$, Pin 17). This configuration is acceptable if \overline{RAS} decoding selection is done. Experience has shown that such short stubbing has

very little effect on the \overline{CAS} signal waveform. If \overline{CAS} decoding is used, then the additional $\overline{CAS2}$ line must be routed through the array as shown in the previous layouts.

4. "RAS-Only" refresh must be used with this layout, even with the single +5 volt devices, because pin 1 is tied to the V_{BB} gridding, which is required for the three supply RAMs. Therefore, for proper operation, pin 1 trace must be tied high (resistor to +5 volts or direct connection to +5 volts) when using the single supply devices.

5. When the single supply devices are used, all of the decoupling capacitors connected to the drain supply (V_{CC}) should be installed. One cap for every other device is an absolute minimum. The V_{BB} capacitors do not have to be installed when using the single supply devices.

The DRAM family compatible PCB layout shown in Figure 10 can be used with any of the Mostek 16-pin or 18-pin high density (N-bit by 1 organization) dynamic RAMs. Table 1 summarizes the array conditions required for each RAM type when using the compatible layout (Figure 10).

Conclusion

A PCB memory matrix layout suitable for use with any of the Mostek compatible family of high density RAM devices has been shown. Minor jumper type changes allow the versatility associated with this compatibility concept. Because the designer may wish to employ only one part of the DRAM family, layouts tailored for each of the family's two major subsets (three power supply devices versus one supply) were also described.

From a systems perspective, the compatibility concept can effectively control the rapidly growing costs of design. Casting a design which provides the option of using several different density devices in a single memory site produces long term savings by eliminating the need for redesign when upgrading density. Such a strategy will stretch the lifetime of a memory design with the minimum of effort required by the compatibility concept.

Besides trimming actual redesign costs, the compatibility concept can increase significantly the financial returns from a single system design. The increased effective system lifetime makes amortization over a longer than normal period of time possible. Exceeding the typical industry limit of a five year lifetime on a single board design not only frees up engineering time, but also slashes the manufacturing and field service related development costs which have become so significant. Viewed in this context, the compatibility concept offers promising short- and long-term benefits to both the memory system designer and his organization.

Table 1

RAM TYPE	(PIN 9) ARRAY V _{DD} BUS	(PIN 11) ARRAY V _{CC} /A ₇	(PIN 1) ARRAY V _{BB} BUS	DATA PULL-UP RESISTORS	RAS BOUNDARY RAS ₁ /RAS ₂
MK4116	J ₂ (+12V)	+5 Volts	J ₃ (-5V)	2.2K OHM	16K/NA
MK4332	J ₂ (+12V)	+5 Volts	J ₃ (-5V)	2.2K OHM	16K/16K
MK4516	J ₁ (+5V)	Don't Care	J ₄ (+5V)	Open	16K/NA
MK4532	J ₁ (+5V)	Don't Care	J ₄ (+5V)	Open	16K/16K
MK4164	J ₁ (+5)	A ₇	J ₄ (+5V)	Open	64K/NA
MK4528	J ₁ (+5)	A ₇	J ₄ (+5V)	Open	64K/64K

In some applications, the system power supplies can be changed to eliminate the need for jumpers.

**DYNAMIC
RAMS**

MOSTEK®

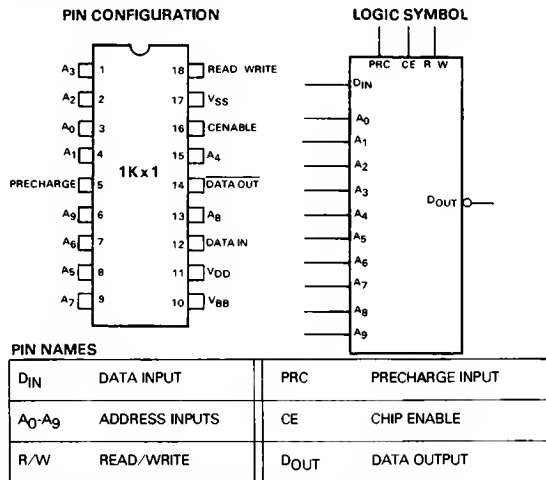
SEMICONDUCTOR MEMORY IN THE 80's

Technology Brief

In the computer memory hierarchy, main memory serves as the working memory where programs and frequently used information are stored. This memory evolved from the early days of vacuum tubes into magnetic core storage in the 50's and 60's. The 70's saw the advent of the semiconductor RAM. The 1103 (See Figure 1) 1K x 1 Dynamic RAM, was the beginning of the semiconductor memory revolution. The 1103, although not cost effective, did offer significant modularity advantages and a strong promise of things to come.

1st SIGNIFICANT DYNAMIC RAM PRODUCT

Figure 1



Semiconductor memory underwent rapid improvement in density, performance and cost. This evolution is shown in Figure 2. The 4096, introduced in 1973 by Mostek, was cost competitive with core and initiated the replacement cycle. The 4096 introduced several new concepts such as the one transistor cell which enhanced the circuit density and a revolutionary packaging scheme which nearly doubled systems density (See Figure 3). Both of these factors greatly enhanced the ability of semiconductor memory to compete with core. Still a relatively young technology, there was room for many improvements in density, cost and performance. The 4027 was introduced next in the evolutionary cycle in 1976 and improved on the circuit design capabilities available in the 4096 generation. The 4027 introduced a revolutionary sense amplifier which permitted an order of magnitude reduction in the amount of signal required, thereby permitting smaller and smaller cell sizes (See Figure 4). Process evolution also occurred and transformed an obsolete metal gate process into the currently used volume

Presented by Sam Young at ELECTRO 1980.

RANDOM ACCESS MEMORY EVOLUTION

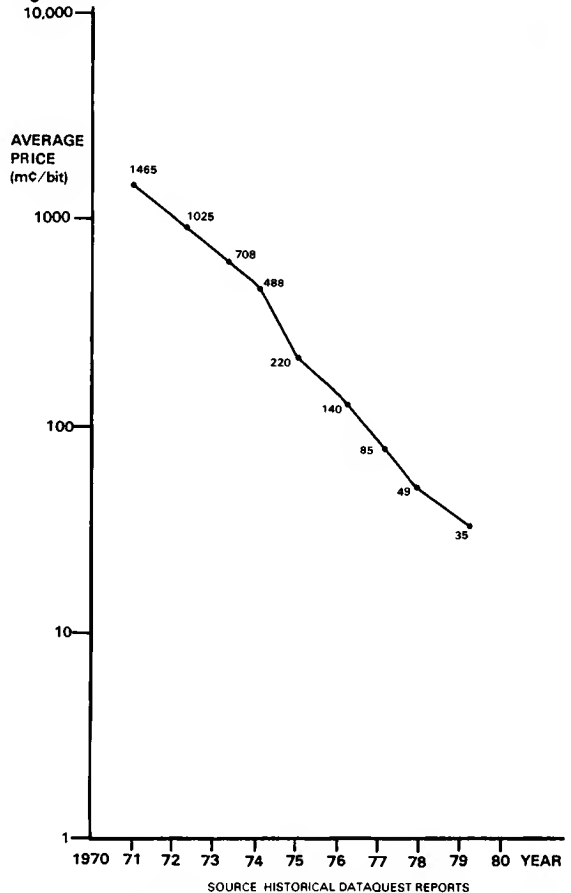
Figure 2A

YEAR	PART	CONFIGURATION	DIE AREA IN MIL ²	SIZE DIMENSION IN MILS	ACCESS
1970	1103	1K x 1 Dynamic	20K	—	350ns
1973	4096	4K x 1 Dynamic	28K	150 x 187	350ns
1974	4096	4K x 1 Dynamic	18.9K	127 x 147	250ns
1976	4027	4K x 1 Dynamic	20K	165 x 122	200ns
1976	4027	4K x 1 Dynamic	14.5K	104 x 140	150ns
1976	4116	16K x 1 Dynamic	27.7K	122 x 227	150ns
1977	4027	4K x 1 Dynamic	11.9K	96 x 124	120ns
1977	4116	16K x 1 Dynamic	22.3K	110 x 203	120ns

DYNAMIC
RAMS

DYNAMIC MOS RAM PRICE TREND

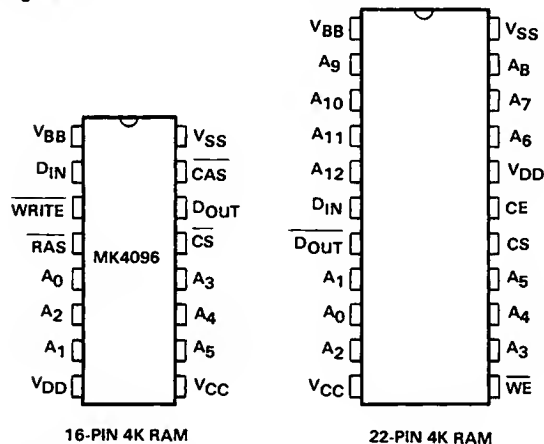
Figure 2B



production N-Channel silicon gate process technology. With the advent of the 4027, the argument of magnetic core still being competitive was all but dispelled. However, semiconductor memory in this generation was still sold at a price

NOVEL 16 PIN PACKAGE SAVES SPACE

Figure 3



EVOLUTION OF 1-T CELL SIZES

Figure 4

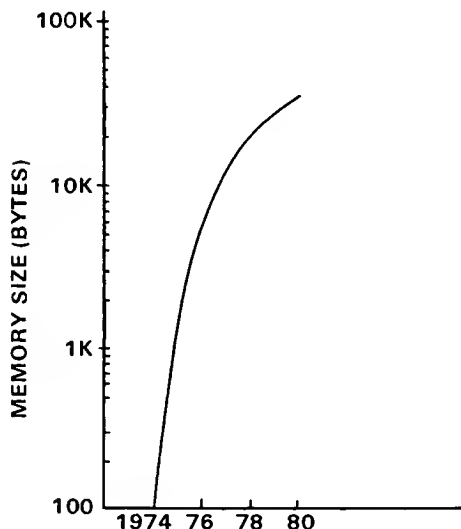
Device	Voltages	Size	Cell Area	Die Area
MK4096	+12, -5	4096 x 1	1.48 mil ²	18,923 mil ²
MK4027	+12, -5	4096 x 1	0.98 mil ²	11,844 mil ²
MK4116	+12, -5	16,384 x 1	0.55 mil ²	22,330 mil ²
MK4516	+5	16,384 x 1	0.39 mil ²	17,000 mil ²
MK4164	+5	65,536 x 1	0.30 mil ²	40,700 mil ²

premium. Therefore, users were still very conscious of the amount of memory incorporated into a system. In fact, great care was taken to optimize the software packing densities required by the host computer. In the mid-70's, a typical small machine used about 3 kilobytes of RAM at a cost of about \$100. Assembly language was typically used to minimize RAM size and required about 6 man-months to complete. Continuous breakthroughs in memory design technology quickly took semiconductor memory to the 16K bit generation. The key product of this era was the 4116 type RAM using a Poly II process. At the 16K level, computer manufacturers began to realize that memory cost was no longer an inhibiting factor. In fact, due to the people shortages of the late 70's, it became more advantageous to utilize more memory and expend less resources in trying to keep the programs efficient. Currently, a typical small system will use 40 - 50K bytes of memory (See Figure 5).

The 40K memory now costs only slightly more than the 3K of the mid 70's. Software costs, however, are huge with assembly language, and implementation today requires an order of magnitude more code than before. For this reason, many applications now use high order languages to reduce programming time at the expense of hardware. Today, this is a very practical tradeoff. So, we have seen a reversal for the first time in history of allocating more hardware rather than less to solve a problem.

TYPICAL COMPUTER MEMORY BECOMES LARGER OVER TIME

Figure 5



Due to the significantly decreasing cost per bit as well as actual density enhancement, main memory size has grown larger and larger. Multi-megabyte memory systems are quite common in some of the larger computers today. The fundamental minicomputer itself usually absorbs 64K to 256K bytes of memory. The new 16 bit MP chips have addressability well in excess of a megabyte of RAM.

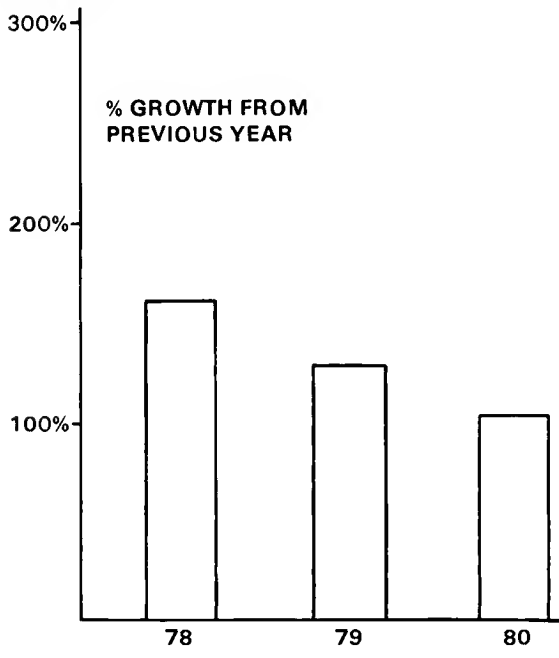
The previous discussion centers on several of the reasons for higher growth of the classical memory segment. A lower cost per bit also fuels demand bit expansion by opening up many new markets such as the home computer, small business computer, electronic games, intelligent terminals, telecom switches, etc. The constant cost reduction not only permits larger and larger main memories but is also beginning to permit penetration into mass memory. We currently see several manufacturers entering into the disk market using Solid State products. These end use products, commonly referred to as Solid State Disks, will enhance the performance of mass storage media, thereby bringing a performance/cost trade-off into the purchase decision.

One of the key questions in the semiconductor industry is how large the market growth for semiconductor memory will be. An assessment of the magnitude of this growth can be made by combining historic bit growth rates with industry projections of bit growth percentages. First, let us look from the historic perspective with reasonable visibility into 1980. This growth rate in bits is shown in Figure 6. Note the percentage is over 100% per year. Taking a slightly

conservative view, one can make a projection for the future. Figure 7 depicts the anticipated growth normalized in bits. Things affecting the bit growth rate are the firming of prices and the slow ramp of the next generation product, the 64K Dynamic RAM. Applying the bit growth rate assumption of Figure 7 to the known 1979 level, the projection of Figure 8 can be made. For convenience, since it is difficult to visualize billions of bits, the data is presented in equivalent 16K units. The numbers are fascinating in that in 1980, the industry will ship approximately as many MOS bits as it cumulatively shipped in all preceeding years. The 1984 number of 1,015,000,000 units, in bits is a mind boggling 16,629,760,000,000, which is trillions of bits.

HISTORIC D-RAM BIT GROWTH

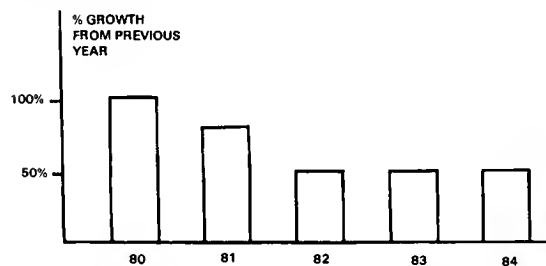
Figure 6



The last step of the projection question is to attempt to quantify the projected bits into device type, in this case 16K or 64K. The fundamental question is what percentage will be 64K RAM. The remaining bits will have to become 16Ks or not be built. This question is very subjective and one approach is to again use history. The 16K will be used as the reference vehicle for the bit mix projection. Several items should be considered when trying to rationalize the 64K ramp rate. The two key issues are the technology requirements and changes in supplier base. In the area of technology, in order to go from 4K to 16K, the industry merely had to change from a Poly I to a Poly II process. (See Figure 9). The 16K circuit design was pioneered by the MK4027 (4K device). The power supply voltage and the device geometries were the same. To achieve 64K density, the circuit design must undergo radical changes to accomodate single 5V supply requirements. Also, to achieve cost, performance and reliability goals, it is necessary to change device geometries from 5 micron rules to 3 micron

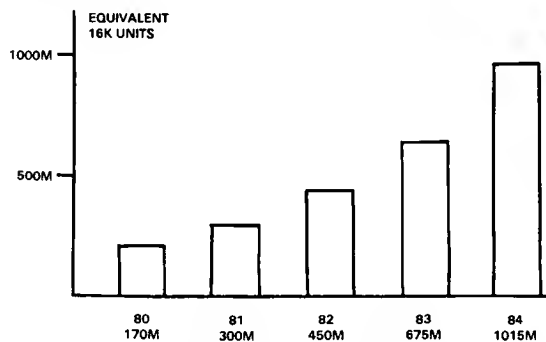
DYNAMIC RAM BIT GROWTH PROJECTION

Figure 7



FIVE YEAR DYNAMIC RAM TAM PROJECTION

Figure 8



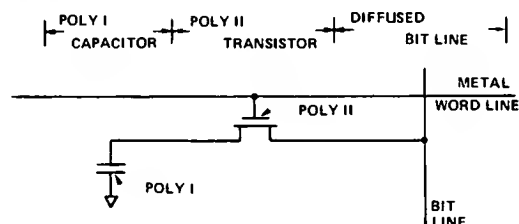
rules. This requires significant circuit design changes as well as use of new fabrication equipment. This makes the 64K a significantly tougher challenge in the evolutionary process. Even with the tighter geometries, the 64K will be a large die to manufacture: 35,000 to 40,000 mils depending upon the manufacturer vs 22,000 or 28,000 for 16K. This will significantly reduce units or bits shipped per wafer, thereby requiring large numbers of wafers to achieve a volume of product similar to that of the 16K generation. NOTE: Device yield decreases exponentially as die area increases:

$$Y = e^{-DA}$$

where Y = yield
D = defect constant
A = die area

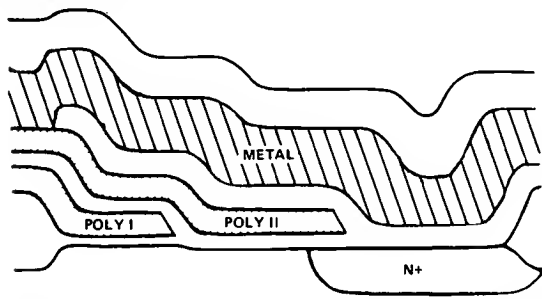
4K CELL

Figure 9A



MK4116 CELL AND CROSS SECTION

Figure 9B



This, incorporated with the limited production capacity currently available in the industry, will tend to limit the number of 64K's that will be available.

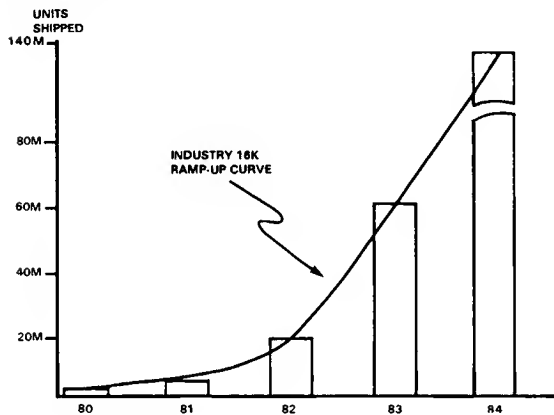
On the supply side, the Japanese are now a far greater contributor to the Dynamic RAM market than they were at the 16K introduction phase. Their participation will add capacity. However, many American manufacturers have de-emphasized the Dynamic RAM due to competitive pressures, offsetting some of the gain due to foreign participation.

If we assume for now that the 64K RAMP will match that of the 16K introduction phase, the projection of Figure 10 is realized. It should be understood clearly that the start time is key. The model will skew in time as the start period shifts. To fuel this capacity, the industry will need to invest huge amounts of capital much of which will come from current and future profits. Incorporating the information of Figure 10 into the TAM projection of Figure 8 yields the projected device mix, (See Figure 11), by year for the above assumptions. If this scenario happens, the industry will need to produce a huge quantity of 16K RAMs over the next five years. The ability of the bit growth demand projection to be realized in the face of firming prices without aid of the 64K is one of the many questions which still remain unanswered.

In the 70's, Dynamic RAM operated from several power supplies. These are +12V, commonly called V_{DD} , +5V commonly called V_{CC} , and a negative supply used to bias the

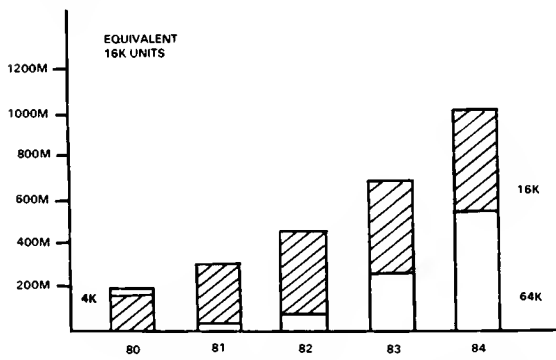
PROJECTED 64K RAMP-UP

Figure 10



FIVE YEAR DYNAMIC RAM TAM PROJECTION BY PRODUCT

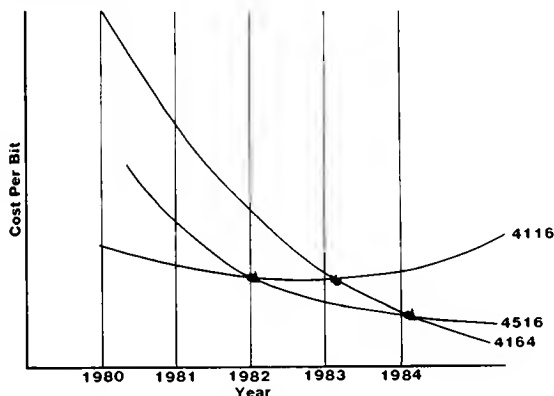
Figure 11



substrate at -5V commonly called V_{BB} . New generation devices which will become available in 1980 will offer a single supply alternative of 5V. These devices will all utilize a scaled process technology to further reduce the die size and power levels, thereby continuing the cost performance advantages of the MOS memory technology. Products of this type will be the MK4516, which is a 5V 16K x 1 Dynamic RAM with access time capability below 100 nsec, one half that of its predecessor the 4116. The 16K RAM has a large portion of its life cycle still ahead due to the huge bit demand and inability of the 64K to meet this requirement. The 16K device is currently a mature product with most of its cost reduction potential behind it. If the historical cost reduction of a Figure 2 is to continue, a second generation 16K device will be required. The 4K to 16K cost crossover was significantly delayed by the introduction of the second generation 4K (MK 4027, See Figure 2). Had this device not been built, the price per bit would have been significantly higher than the curve of Figure 2 shows. The 2nd generation 16K device (4516) will offer significant cost, performance and power dissipation advantages over the current production device. Unlike the 4K second generation, the second generation 16K will also be easier to use (one power supply and on-chip refresh) than its

AVERAGE SELLING PRICE PROJECTIONS PRICED IN EQUIVALENT 16K's

Figure 12

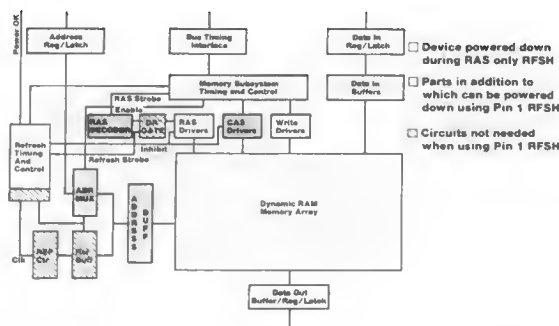


predecessor. The next major product in the 5V family is the 4164 or 64K Dynamic RAM. These two products are architected to be identical so that compatibility between generations can exist. The complex price relationships between the current 16K, future 16K (4516) and 64K (4164) are projected in Figure 12.

The new generation RAMs offer on chip techniques to ease the requirements of refreshing. The 5V RAMs include a refresh address register to eliminate the need to generate and supply a special address when refreshing the RAM. Also, a separate pin is assigned for refresh to enhance system performance as well as reduce parts count and power dissipation. This can be explained by referencing the memory system block drawing of Figure 13.

DYNAMIC RAM MEMORY ARRAY

Figure 13



The refresh function eliminates the need for those components associated with generating and timing the refresh address. Also eliminated is the "OR" gate shown in the block drawing which was needed to permit refreshing all devices simultaneously in the memory system. Eliminating components from the memory system has several obvious advantages and several not so obvious advantages.

The obvious advantages are:

- 1) Cost Reduction
- 2) Space Reduction

The not so obvious advantages are:

- 1) Power Reduction
- 2) Performance Enhancement

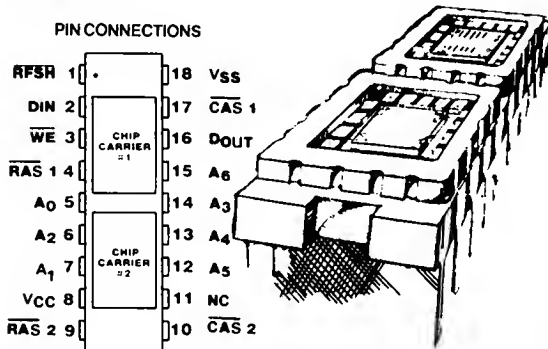
The power reduction is extremely significant when utilizing a system in battery back up. Power savings is achieved by eliminating the need for power consuming devices and by permitting additional devices to be unused during refresh. These devices are highlighted in Figure 13. The performance savings are made by eliminating a device, the "OR gate" in the system's speed critical path. This device has existed in all previous generation systems but can now be eliminated. This typically saves 10 nsec in performance. This is a significant number in systems using new generation devices. At 100 nsec or less this becomes extremely significant. This refresh feature is the beginning of an era of intelligent RAMs.

In the 80's, there will be many new concepts being introduced to the world due to the accelerated demand for memory. Memory size requirements have grown to the point where system area has become extremely valuable to the system designer. Also, in the 80's we will find a significant shortage of engineers. It is therefore essential that we maximize the utilization of our engineering resource by minimizing the time spent in product design.

The multiplexed pin out selected in 1973 for use with the 4096 device has proven to be extremely flexible. The pin out utilized only 16 pins to accomplish 20 pins worth of functions on the device. The parts accomplish this by multiplexing the address inputs to the device. Normally 12 pins would be needed for 4K of memory to address it uniquely. By utilizing the multiplex concept, only 6 pins were needed. In fact, at the 4K level, one additional pin was not needed for basic functionality and this pin was, therefore, allocated to a chip select function. The 4027 or next generation device utilized exactly the same pin out, as did the 4116 16K device and the 64K which is soon to be offered. Evolution of functionality has permitted this expansion to occur. In going to the 16K, the chip select function was easily eliminated thereby allowing the additional address needed to decode the additional 12K of memory existing on this device. Typically, 2 bits are needed to do the decoding; however, when multiplexing that reduced the number to only 1. The 64K needs, again, an additional pin for its addressing capabilities. Fortunately, the 64K requires only one power supply thereby permitting the address to be added without increasing the package size. For convenience, this function has been added to Pin 9 which was V_{CC} on the 3 power supply devices (See Figure 3). If one were to take the basic pin-out used on this multiplexed RAM and decide to double the density per chip, (See Figure 14), one could add two extra pins to the bottom of the fundamental pin out. An additional RAS function to gain selectability between desired elements of the dual density RAM could be added. For additional convenience, one could also add an extra CAS function to include an extra dimension of selectability

DUAL DENSITY MODULE DOUBLES DENSITY

Figure 14



although this approach would be somewhat superfluous. The dual density achieved using this technique offers several major advantages. The device can be made pin compatible with its predecessor generation even though it contains two additional pins. The new device relies on the technology of the current generation device, and therefore benefits from all the learning experience and yield enhancements of the current product. In the 80's, due to increasing memory requirements, people will find it advantageous to package as much memory as feasible in as small an area as possible. To achieve this end, a new concept for the 80's has been created to aid the user in maximizing his engineering resources as well as maximizing the available space for memory in the computer.

In the 80's, the compatibility concept will be introduced and mature. Figure 15 depicts the compatibility family of products. There are three levels of compatibility which may be considered when utilizing this concept in board design. The first of these would be to merely design the three power supply family into the board. This would permit interchangeability between the 4K 4027, 16K 4116, and the 4332 32K module. This permits quadrupling or doubling the density without redesign. In fact, the same assembly based on application need, can be utilized by merely swapping out the parts and putting in the appropriate jumpers to enable the proper memory decode. The second compatibility concept possible is to key into the 5V RAM new generation of products which consists of the 4516 16K 5V, the 4532 32K x 1 5V, the 4164 64K x 1 5V RAM, and the 4528 128K x 1 5V

Dynamic RAM. Both the 4532 and the 4528 utilize the 18 pin package. The third approach that can be taken involves designing a board capable of following the evolutionary path using all the products on the compatibility chart. These devices consist of the three power supply as well as single supply devices. It is possible to design a board to accommodate any configuration of these devices. However, this topic is not a subject of this paper; the technical aspects of the design will require a great deal of discussion. There is literature available from Mostek on how to implement this concept. It is extremely interesting to note that the upper 16 pins of the dual density package concept are identical to the 16 pin definition which has been in existence since 1973. This permits drop-in compatibility between all generations of products, thereby simplifying the task of the designer to perform a compatible design.

Utilizing a compatibility concept, it is possible to implement extremely dense memories with today's technology. This concept will aid the computer designer of the 80's in achieving main memory densities previously approached only in mass storage devices. Also eliminated will be the need to continuously redesign for each successive generation of products.

The trend for larger and larger memory systems with new application opening up will continue. The constant improvements in memory technology will permit the cost/performance objective of new applications to be met. The eighties will be the decade of the RAM.

MOSTEK'S COMPATIBILITY CONCEPT

Figure 15

4528 128K (5V)	4164 64K (5V)	4532 32K (5V)	4516 16K (5V)	4332 32K	4116 16K	4027 4K		4027 4K	4116 16K	4332 32K	4516 16K (5V)	4532 32K (5V)	4164 64K (5V)	4528 128K (5V)
RFSH	RFSH	RFSH	RFSH	V ₈₈	V ₈₈	V ₈₈	1 (1)	(18) 16	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}
D _{IN}	D _{IN}	D _{IN}	D _{IN}	D _{IN}	D _{IN}	D _{IN}	2 (2)	(17) 15	CAS	CAS	CAS1	CAS	CAS1	CAS1
WRITE	WRITE	WRITE	WRITE	WRITE	WRITE	WRITE	3 (3)	(16) 14	D _{DUT}	D _{DUT}	D _{DUT}	D _{DUT}	D _{DUT}	D _{DUT}
RAS1	RAS	RAS1	RAS	RAS1	RAS	RAS	4 (4)	(15) 13	CS	A ₆	A ₆	A ₆	A ₆	A ₆
A ₀	A ₀	A ₀	A ₀	A ₀	A ₀	A ₀	5 (5)	(14) 12	A ₃	A ₃	A ₃	A ₃	A ₃	A ₃
A ₂	A ₂	A ₂	A ₂	A ₂	A ₂	A ₂	6 (6)	(13) 11	A ₄	A ₄	A ₄	A ₄	A ₄	A ₄
A ₁	A ₁	A ₁	A ₁	A ₁	A ₁	A ₁	7 (7)	(12) 10	A ₅	A ₅	A ₅	A ₅	A ₅	A ₅
V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{DD}	V _{DD}	V _{DD}	8 (8)	(11) 9	V _{CC}	V _{CC}	V _{CC}	NC	NC	A ₇
RAS2		RAS2		RAS2			(9)	(10)			CAS2		CAS2	CAS2

Parentheses Indicate Pin Number of 18 Pin Packages. 16 Pin Devices are Upper Justified in 18 Pin Socket

1980 MEMORY DESIGNERS GUIDE

X	Dynamic Random Access Memory	DYNAMIC RAMS
XI	Static Random Access Memory	STATIC RAMS
XII	Read Only Memory	ROMS
XIII	Technology	TECHNOLOGY
XIV	Memory Systems	MEMORY SYSTEMS

POLYSILICON-LOAD RAMS PLUG INTO MAINFRAMES OR MICROPROCESSORS Technology

INTRODUCTION

The past decade has witnessed a truly phenomenal growth in the number of MOS random-access memory types, with corresponding improvements in speeds and densities. But most of the emphasis has been on designs for mainframe computer memory. The chips in that type of memory are best organized in a bit-wide fashion (as in a 4K x 1 bit device) and must be inexpensive on a per-bit basis. But microprocessors have different requirements, and there the 8-bit-, or byte-wide, chip organization has proved the most efficient. Today's generation of MOS microprocessors are high-performance, multifunctional, easy to use, and low-cost—and the memory designed for them has to have the same features.

At the same time, MOS performance has improved to a point where a MOS RAM can fill many of the high-speed applications for which bipolar memories alone were once suitable: buffer and cache memories and writable control stores are examples. The question now is, can one memory suit both the microprocessor and the fast mainframe applications?

Enter the MK4118 and MK4801, a pair of 1,024 x 8-bit static RAMs that run that gamut of applications from microprocessor to mainframe. The devices have the same functions and 24-pin packaging, but differ in processing and speed. The 4118 is built with Mostek's Poly R process and meets microprocessor speed requirements with its 120-to-250 nanosecond access times; the 4801, on the other hand, uses the new Scaled Poly 5 process to achieve 55-to-90ns accesses offering a lower-power, higher-density alternative to the current generation of bipolar RAMs, such as the 4K x 1-bit 93471 from Fairchild Camera and Instrument Corp.

The design of a flexible RAM had to take the needs of control, power-down, and timing into account. A technique first used by Mostek in its 1K x 4-bit MK4104 static RAM was a clocked, or dynamic, control periphery, similar to that used in dynamic RAMs. Although the technique reduced power consumption, the RAM required an external chip-enable pulse to initiate the internal timing sequences. A different approach is used by Intel Corp. in designing the fully static 1K x 4-bit 2148, which instead relies on its chip-select input to turn off some of the internal circuits, thereby power-gating the device.

POWER-DOWN APPROACHES

Both approaches, however, place certain restrictions on signal timing, such as minimum precharge or active time for the chip-enable or chip-select inputs. Indeed, the 4104 will not read or write at all unless its chip enable input (\overline{CE}) sees a signal with a falling edge. But the 4104 was unique in that it contained circuits to detect such an edge—called edge activation—and start the internal sequence of events. The advantage was clear: reduced power in both the active and standby modes, just as in a dynamic RAM.

The 4118 and 4801 take the edge-activated concept a step further by eliminating the need for an external clock. That is accomplished by a circuit that can sense a transition, whether high- or low-going. With such a circuit on each of the chips' 10 address lines, the 4118 and 4801 can each generate its own clock pulse to start the internal timing, based on a change on any of those address lines.

The sensing circuit in the address buffers that generates the pulse is called a sense-address-transition (or SAT) detector (Figure 1). The address buffer is, in effect, connected to the control periphery; the negative edge of the SAT pulse, which occurs at any address transition, starts the internal cycle.

The 4118 and 4801 thus have the advantage of clocked periphery—low power—without the restrictions of an external clock requirement. This feature is called Address-Activated operation, and it is totally transparent to the user.

In addition to the SAT detector circuit, the 4118 and 4801 have other circuits designed to cut power dissipation. Tree decoders and clocked sense amplifiers are other examples. The decoders draw only leakage current in any stable state of chip operation; power is drawn only during transitions.

AUTOMATIC POWER-DOWN

Another example of low-power design is the chips' automatic power-down feature. Unlike the 2148, which powers down only when its chip enable input (\overline{CE}) is brought high, the 4118 and 4801 automatically reduce power to a standby mode once data is latched, as an internal clock shuts off power to the decoders and to the

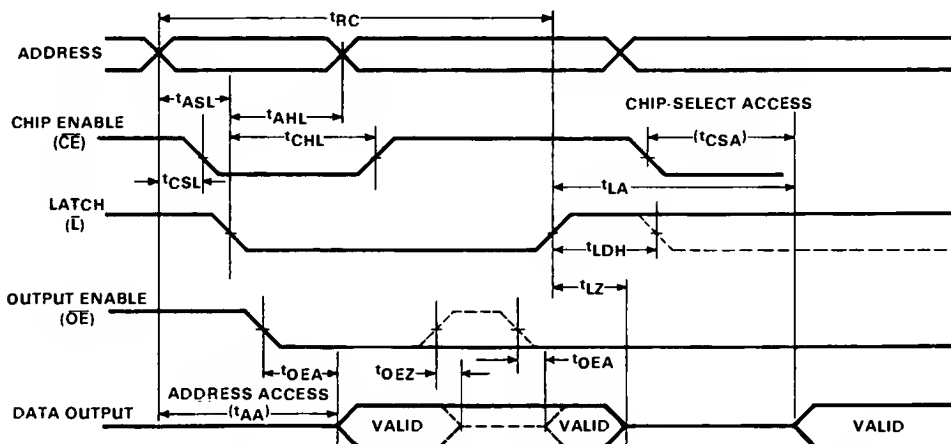
clocked sense amplifiers. The reduction in power dissipation is about 30%; although other power-down RAMs may offer a greater reduction, the 4118 and 4801 devices pay no timing penalties for their use of this feature.

Address data must be stabilized at the time either the latch or the write-enable lines are driven low. When writing data, the cycle will not be terminated until the clock signal has propagated through the polysilicon delay line; once through, the clock signal changes the state of the CEW flip-flop and thus reconnects the address line to the SAT detector. In a latched-read cycle, however, the address will not reconnect to the SAT detector until the latch input \overline{L} returns high.

Both the 4118 and 4801 rely on a substrate-bias generator (or charge pump) to supply the substrate with

Before a bit cell is read, the equilibrate signal's function is to hold the complementary DATA and DATA lines of the cell to +5V. When this signal is disabled, the complementary lines float at +5V. It is only when a particular cell is accessed that one of the two data lines is pulled to ground.

Figure 2



Latched read. The 4118 and 4801 have built in latches that are handy in multiplexed-bus systems. A latched-read cycle (write-enable, \overline{WE} , high) is performed by taking latch input (\overline{L}) low, which latches address and chip-select inputs and supplies data to the output drivers.

If a low signal is stored on the side of the cell not supplying power to the load resistors, the data line supplying power remains near 5V. But though it would appear detrimental that the line supplying power to the cell should be pulled to ground, the timing of the 4118 and 4801 is such that an adequate differential signal is generated between the DATA and $\overline{\text{DATA}}$ lines long before the low-going line can be pulled low enough to cause the voltage on that line to drop below the value required to maintain data in the column of cells to which it connects. That 200-to-300-millivolt difference between DATA and $\overline{\text{DATA}}$ is amplified by the differential amplifier that follows the cell, and once enough signal is generated, the polysilicon delay circuit enables the sense-amplifier clocks and disables the decoders. At that time, the equilibrate flip flop also turns on, pulling both DATA and $\overline{\text{DATA}}$ back to +5V. A short time after the clock pulse has enabled the sense amplifiers, the latched data is available at the outputs.

TIMING MATTERS

The timing diagram for a latched read cycle is shown in Figure 2. It is the same as the usual read cycle except that when the latch line is driven low, the address and chip enable information is automatically latched into the chip. \overline{L} also disconnects the address and chip-select pins from the input circuit. In this type of a read cycle the address and chip enable data must be valid prior to the latch signal transition and must be held valid for a specific time period, as the diagram shows.

Two other controls that can be utilized in the read cycle are the chip-select and output-enable inputs. If those inputs are not taken valid during the cycle, the output buffers will not be enabled. The chip, however, will go

ahead and access data from its cells for presenting to the output buffers. Because of that, both the 4118 and 4801 have a fast access time as measured from output enable or chip enable—50% that of the normal address access time.

The write cycle is slightly more complicated than the read cycle. The write-enable line $\overline{\text{going}}$ low has the same effect on addresses as $\overline{\text{L}}$ going low: both addresses and the chip enable are latched. Both of these therefore have a set-up and hold time with respect to the leading edge of the $\overline{\text{WE}}$ signal.

In the 4118 and 4801, the actual write operation does not occur until the rising edge of the WE signal. When that edge occurs, internal circuits pull either the DATA or DATA line in a cell to ground. But writing differs from reading in that the line must be pulled all the way to ground to set the flip-flop in the cell. Just as in the worst case of the read cycle—when the data line supplying power to the cell is pulled to ground—writing again pulls the data line low on a whole column of cells, which would seem disastrous.

However, the design is such that the RC time constant of the load resistors and the corresponding parasitic and cell capacitances is high enough for the voltage on the unselected cells do not drop significantly in the short period of time that the data line is held at ground. The only disadvantage of this type of approach is that neither the 4118 nor 4801 allows a fully static write operation; each write cycle must be initiated and terminated by a falling or a rising edge of the \overline{WE} signal, respectively. Also, since the actual write operation does not occur until the rising edge of the \overline{WE} signal, the input data will have a setup and hold time with respect to \overline{WE} .

COMPATIBILITY

Static RAMs have always suffered a lack of compatibility and an uncertain growth path. Of the standard devices, for example, the 1K RAM is in a 16-pin package and the 4K in an 18-pin package. The 24-pin, 600-mil-wide package is the next standard size, however, and it can fit up to 16K bits: not only is it suitable for the 4118 and 4801 devices, but will house the next-generation MK4802, a 2K x 8-bit static RAM. After that, higher-density devices will have to accommodate themselves to 28-pin packages.

The pinout of the 4801 allows easy upgrade to the 4802, since it substitutes the extra address bit (A_{11}) for the latch input. (Consequently, a system that is designed to eventually be upgraded should allow for that fact if it is using the latch input.)

As for densities higher than 16K, the 32K and 64K static RAMs must be put in 28-pin package, unless some data and address-multiplexing scheme is used. But the 28-pin package is the same width as the 24-pin one, and the pins on the 4118 and 4801 have been arranged such that it is possible to design a memory system to handle 1K and 2K x 8-bit RAMs in the lower 24 locations of a 28-pin socket and still accommodate 32K and 64K devices when those become available. In fact, a memory system comprising RAM, ROM, or EPROM can be designed today using 28-pin sockets that will guarantee

upgrade compatibility through three memory generations, or for the next four to six years.

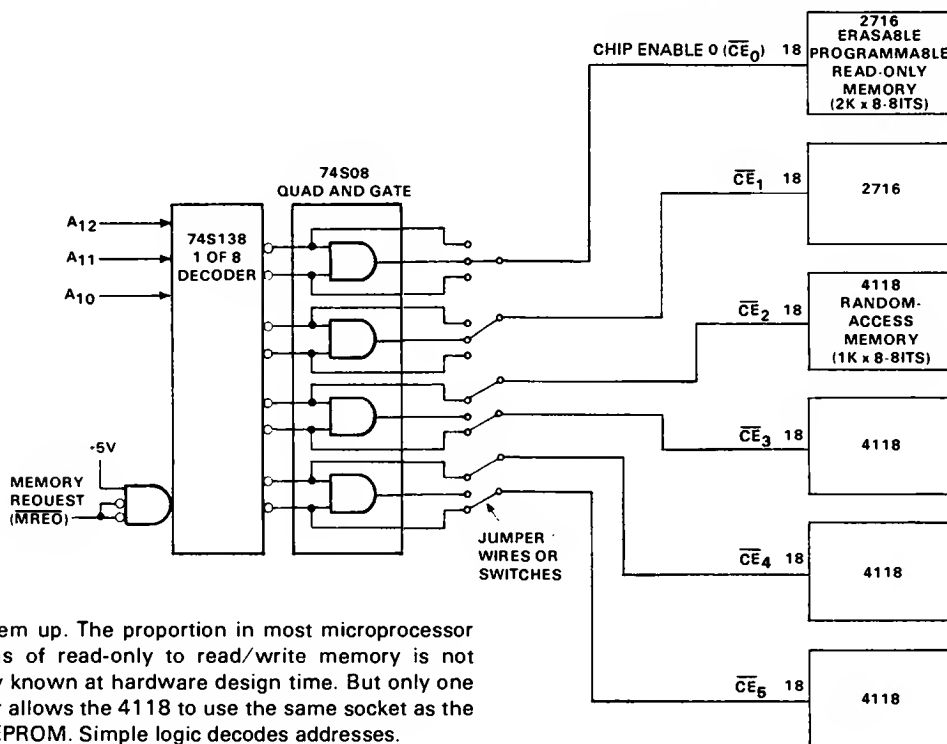
MIXING WITH RAM

The compatibility question comes into play especially when considering microprocessor systems that mix read-only memory with RAM. The exact mixture of RAM and ROM is rarely known at hardware-design time, and it frequently changes even during the course of the product life. The memory designer must allow for expansion with spare sockets in the memory matrix, and if RAM is not pin-compatible with ROM, two matrixes are needed. The result is an excess of unused circuit-board area, which could be avoided by designing around a RAM that is compatible with a ROM—and thus around a single memory matrix that can mix RAM and ROM at will.

Figure 3 shows a typical microprocessor system that mixes RAM and ROM. Six sockets provide 8 kilobytes of memory in any mixture of erasable programmable ROM (EPROM) and RAM). Address differences between the 16K 2716 EPROM and the 4118 are taken care of by a jumper wire on pin 19 of the 4118.

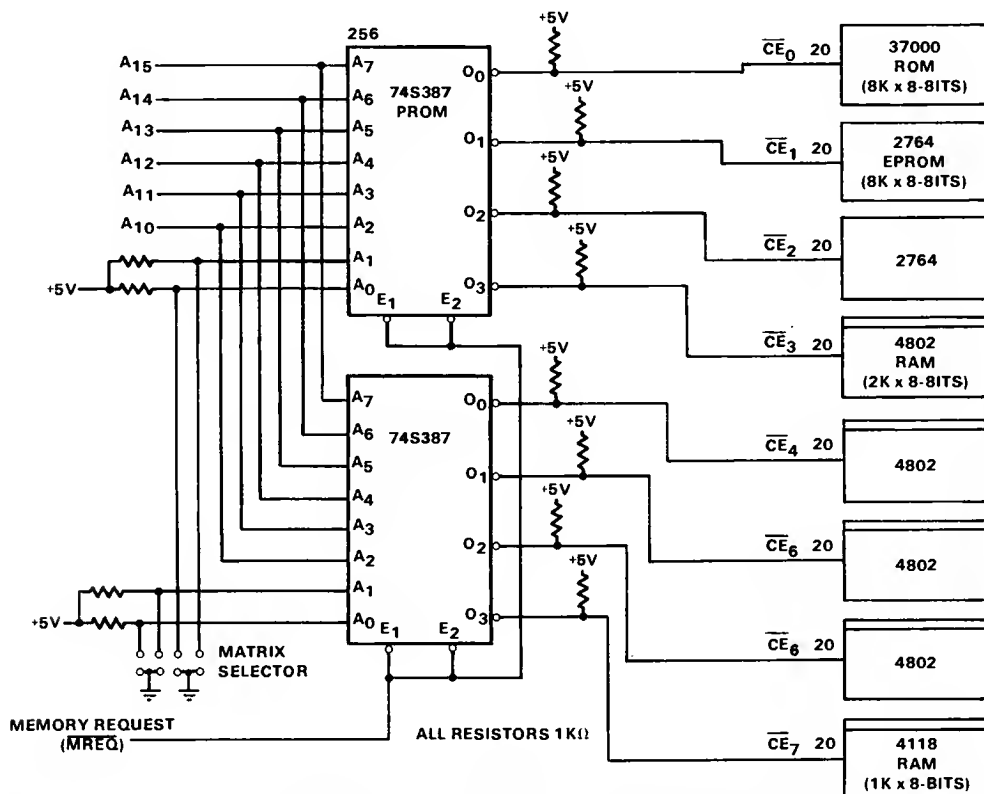
Figure 4 shows the upgrade compatibility of the system, which packs 33 kilobytes—8K of ROM, 16K of EPROM, and 9K of RAM—into eight sockets. The MK37000 is a 28-pin version of the MK36000 8K x 8-bit ROM, and the

Figure 3



Mix them up. The proportion in most microprocessor systems of read-only to read/write memory is not usually known at hardware design time. But only one jumper allows the 4118 to use the same socket as the 2716 EPROM. Simple logic decodes addresses.

Figure 4



Upgradeable. Up to 64K bytes of RAM, ROM, or EPROM will fit into eight 28-pin sockets. Forthcoming MK37000 ROM, MK2764 EPROM, and MK4802 RAM have pinouts compatible with the 4118, allowing upgradability of systems for the next four to six years.

MK2764 is an 8K x 8-bit EPROM. Both the devices are scheduled for introduction in the beginning of next year. Allowing 28-pin packages for the whole matrix increases the capacity of those eight sockets to 64 kilobytes.

The fuse-link PROMs provide a flexible scheme for decoding the socket address space, and switches in dual in-line packages fill the role of address jumpers. Further selection of the memory blocks can be handled by the extra addresses on the PROMs.

The pin compatibility carries further, since high-speed applications can be served by the 4801. It is pin- and performance-compatible with the 82S2708 bipolar PROM—both have 70ns access times—and the two can be paired well in a computer's control store, for example, where the PROM serves as read-only storage and the RAM as writable control store.

Last but not least is the question of compatibility with the 1K x 8-bit RAMs of other manufacturers. Currently, at least five manufacturers have announced intentions of producing devices compatible with the 4118 and

4801. Most of those products will be pin-for-pin-compatible except on pin 19; competitors will leave no connection on that pin, but it must be tied high if it is not used on the 4118 and 4801.

APPLICATIONS SPECTRUM

The 4118 fits into those applications requiring good performance at low cost. As Figure 5a illustrates, the part can easily interface with any microprocessor.

The 4118 is shown in a memory system for the Zilog Z80 microprocessor (Mostek's MK3880) in Figure 5a. The configuration uses 28-pin sockets and can mix RAM, ROM, and EPROM. The high-order microprocessor address bits are fed to a 74S387 256 x 4-bit bipolar PROM for address-space decoding. The PROM allows the space to be redefined at any time. All that is needed is an additional PROM address-decoder to expand the system to eight sockets, which would boost the memory capacity to 64 kilobytes.

A system connecting the 4118 to Motorola's 6809 microprocessor is shown in Figure 5b. The control

STATIC
RAMS

Figure 5a

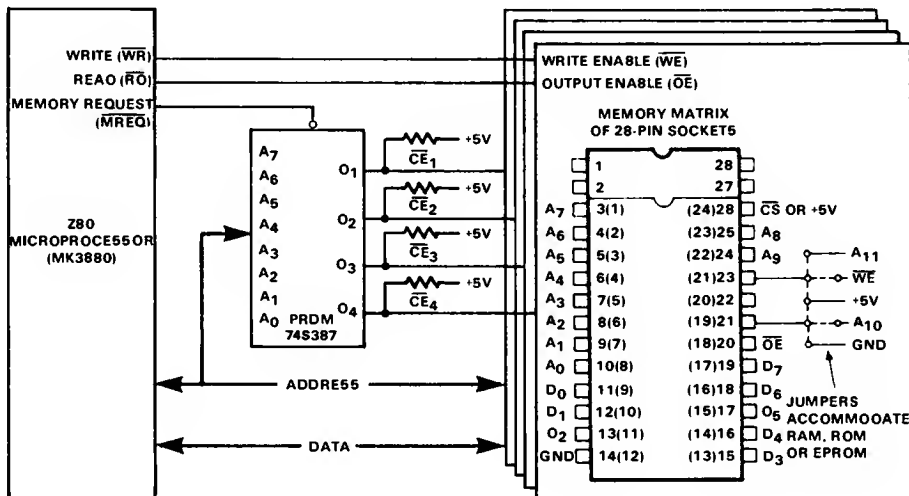
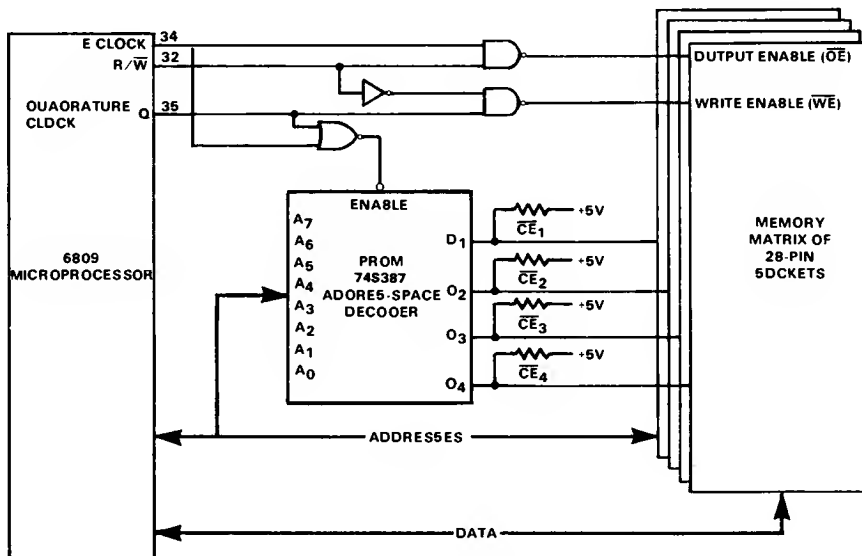


Figure 5b



Easy interfacing. The 4118 RAM hooks easily to most microprocessors. Connecting to the Z80 requires only a PROM for decoding (a). The 6809 requires additional logic (b), whereas the 8085 and 8088 need a latch (c) for demultiplexing. The 16-bit 8086 needs a memory parais (d), as well as a pair of PROMs for byte addressability.

signals in this case require some additional logic for two reasons. The first is that the 6809 puts the read/write control (R/\overline{W}) on a single pin, and logic is needed to separate the output-enable and write-enable signals. The second reason is a combination of several items of timing. To begin with, the 4118 requires that data inputs be held valid after the trailing edge of the \overline{WE} signal; in the 6809, however, data goes away at the same time as the R/\overline{W} signal. The extra logic combines clock output E on the 6809 with quadrature clock output Q to take the RAM's \overline{WE} high before R/\overline{W} . This ensures that \overline{WE} goes high approximately one quarter of a cycle before the disappearance of data.

Also, the E and Q outputs on the 6809 are used to enable the PROM decoder. Doing so provides an active period of three quarters of the microprocessor cycle and a chip-enable-precharge period of one quarter of the cycle as required by the edge-activated ROMs. All other connections to the 6809 are the same as in the Z80 connection.

ADD A LATCH

The 4118 fits easily into the Intel 8085 or 8088 microprocessor scheme, as Figure 5c shows. Read and

Figure 5c

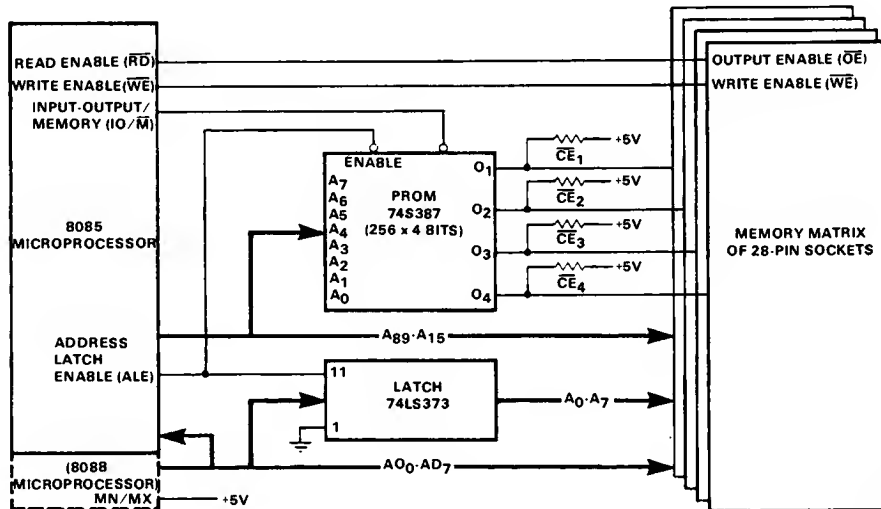
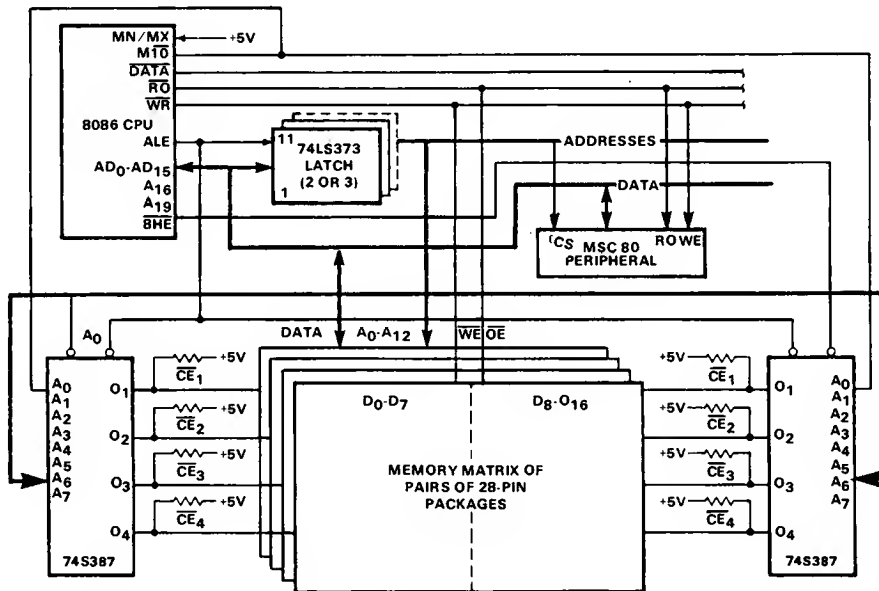


Figure 5d



write controls connect directly. The microprocessors' IO/M line, which determines whether the data path is to an input/output device or memory, connects to the enable input of the PROM decoder. The address-latch enable (ALE) connects to the PROM decoder and to the enable of a 74LS373 8-bit latch, which demultiplexes address and data on the 8085 and 8088 microprocessors.

Connecting to the 8086, Intel's 16-bit microprocessor, is nearly the same as to the 8085 except that pairs of 4118s are required to accommodate the 16-bit word (Figure 5d). Two PROM decoders are required to generate the chip-enable signals to meet the byte

addressability requirement—the 8086 can pick either 8- or 16-bit data at a time—otherwise a single decoder would suffice.

HIGH-SPEED APPLICATIONS

The 4801 serves the high-speed applications market, which currently relies on bipolar RAMs. The largest bipolar RAM is Fairchild's 93470, organized as 4K x 1-bit. The 4801 has twice the density, yet can dissipate as little as one fourth the power when used in a 4K x 8-bit array. (A similar array using 93415 1K RAMs would dissipate six times as much power as a 4801

implementation.) In addition, the 4801's BYTEWYDE organization fits well into a good number of bipolar applications.

BETTERING BIPOLAR

One application that has always used bipolar memories exclusively is caches and writable control stores in a computer. The 4801 can serve as a cache between a bit-slice processor and main memory, which would use dynamic RAMs, and at the same time can fill the various requirements of the processor's writable control store.

Another application that requires the 4801's high speed is multiported memory. Many distributed systems have several slow microprocessors that share a global memory.

If the memory is fast enough, which the 4801 is, the system can be configured such that all memory is shared without any significant slowing of either the overall system speed or the speed of any individual processor. In this application, the 4801 can greatly cut system costs by eliminating memory redundancy.

CONCEPTS FOR A DENSE NEW RAM

In 1976, Mostek introduced its Poly R process with the MK4104, a 4K x 1-bit static RAM. The part diverged from the usual static RAM designs in that it replaced the depletion-mode MOS transistor loads in its cell with ion-implanted polysilicon resistors (Figure a below). The design not only saved chip area but also greatly lowered power dissipation. Since the polysilicon resistors are actually laid over the four transistors, the cell of the 4104 shrank to 2.75 mil²—roughly half the size of conventional cells.

The power is reduced because the high resistivity of the polysilicon loads—typically, 5,000 megohms, accurately controlled by ion implantation—squeezes the current flow down to less than 1 nanoampere per bit. Another feature of the Poly R loads is their negative temperature coefficient, which automatically compensates for increased leakages that normally occur at elevated temperatures. Moreover, the polysilicon loads allow data retention in the cells even at greatly reduced supply voltages.

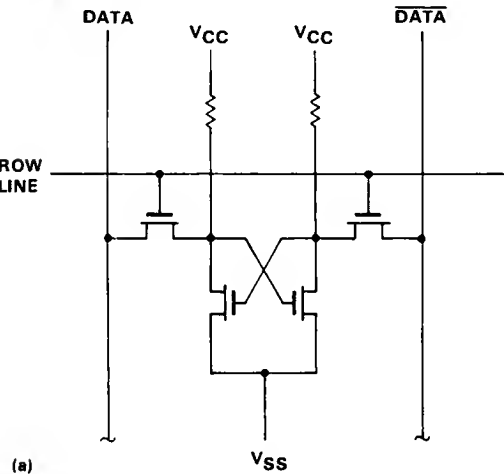
Both the 4118 and 4801 utilize the polysilicon-load concept, with one basic difference. Rather than connecting the load resistors to the positive supply (V_{CC}), as in the 4104, the 8K statics tie both resistors to one of the two data lines, depending on which side of the chip the cell lies, as shown in Figure b. Thus, power is fed to the cells via the column lines through the polysilicon load resistors. The key advantage of this arrangement is the elimination of the V_{CC} contact in the cell and the metal interconnection it required. Using that technique, the 2.75-mil² cell of the 4104 drops to 2.0 mil² in the 4118. Not only is the cell size reduced by tying the loads to the data line, but furthermore the low power and self-compensation advantages of the 4104 are carried through to the 4118, which packs 8K bits onto a 27,000 mil² chip.

NOW SCALING

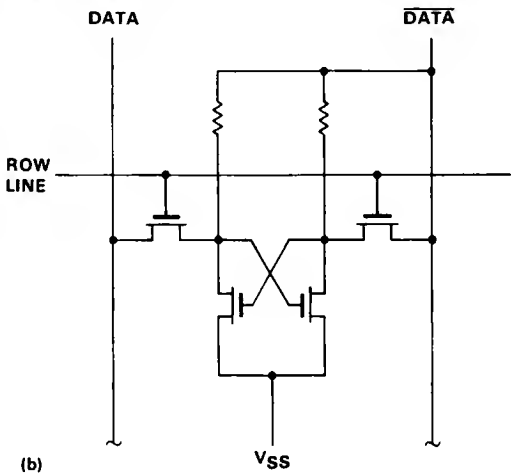
The 4801 is the first part to use Mostek's Scaled Poly 5 process, which further reduces the 2.0-mil² cell of the 4118 to 1.3 mil². The process is Mostek's answer to what will be required for the next generation of products.

Scaling down refers to reducing all physical dimensions both horizontally and vertically, as well as reducing the

MK4104 CELL

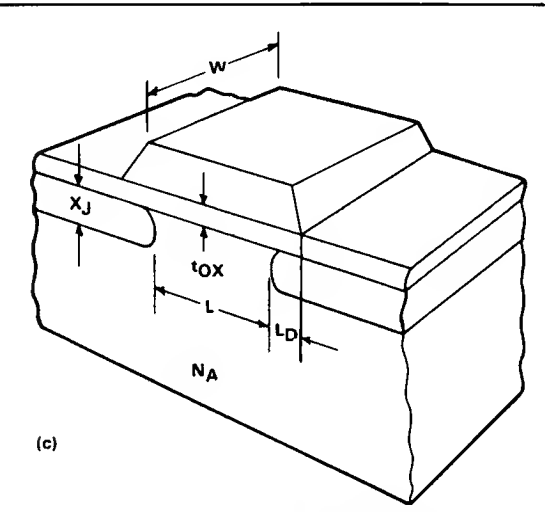


MK4118/4801 CELL



operating voltage. It is not to be confused with shrinking, which simply reduces the critical spacings and the number of elements, say, in a cell; the result is a squeezing together of the circuitry. Scaling down reduces actual design dimensions, plus certain operating characteristics, including voltage power, signal level, and so on.

Below are shown a cross section of a typical MOS transistor and some of the critical dimensions that determine the operating parameters. Thanks to new lithography techniques, the old 5-micrometer dimensions are no longer necessary. Also, since the new 5-volt-only parts reduce the operating voltage (from the 12V level), oxide thicknesses can also be reduced.



In theory, all parameters can be reduced by a constant—5/12 is a good starting point, since the operating voltage is scaled from 12 to 5V. This brute-force technique, however, is not necessarily the most efficient and must be modified somewhat. Table 1 shows both the brute-force and modified approaches.

The differences between the two approaches are there to enhance not only performance but manufacturability and reliability as well. Look, for example, at substrate resistivity. The brute-force technique would reduce it from 10 to 6 ohm-centimeters. The result of that, however, would be high junction capacitance and higher effective threshold voltage due to the body effect. Moreover, manufacturing tolerances also come into play.

Scaled Poly aims also at improving overall device reliability. Table 2 shows the changes in reliability when scaling down by a factor of K. The important one to note is power dissipation. It is a well-proven fact that the lower the power dissipation, the better the inherent device reliability. Current density increases, but there is no net effect on overall reliability because the previous design and process rules were overly conservative.

A final factor in scaling is the type of equipment required to manufacture a device. Scaled Poly 5 can be manufactured with existing equipment and technology—no new equipemnt is required for current products.

COMPARING METHODS OF DEVICE SCALING

Table 1

Device Parameter	Standard N-MOS	Brute Force	Sceled Poly 5
Channel length, L (μm)	5	2.1	2.5
Oxide thickness, t _{OX} (Å°)	850	354	500
Substrate resistivity (Ω-cm)	10	6	30
Power supply voltage (V)	12	5	5
Junction depth, X _J (μm)	1.2	0.45	0.4
Lateral diffusion, L _D (μm)	1.0	0.41	0.3

STATIC RAMS

MOS DEVICE PARAMETER CHANGES DUE TO SCALING

Table 2

Peremeter	Varietion
Field strength	1 ↔
Power per unit area	1 ↔
Current density	1/K ↑
Device power	K ² ↓
Device voltage	K ↓
Power-delay product	K ³ ↓

1980 MEMORY DESIGNERS GUIDE

X Dynamic
Random Access Memory

DYNAMIC
RAMS

XI Static
Random Access Memory

STATIC
RAMS

XII Read Only Memory

ROMS

XIII Technology

TECH-
NOLOGY

XIV Memory Systems

MEMORY
SYSTEMS

MINIMIZING THRESHOLD VOLTAGE TEMPERATURE DEGRADATION WITH A SUBSTRATE BIAS GENERATOR

Application Note

As with any MOS circuit, tight controls must be maintained on process parameters to insure that performance and reliability are maximized. This is important not only to a semiconductor manufacturer but to the user as well. The dependence of proper operation on processing is more critical in today's advanced N-channel circuits than in older generation P-channel circuits. This partially accounts for the limited manufacture of N-channel in the early history of MOS technology. Through research and experience, it has become possible to manufacture highly reliable and good performance N-channel circuits with a fair degree of consistency.

There are still, however, problems that are intrinsic to MOS circuitry that are difficult to compensate for by just controlling process parameters, in particular temperature variations. In Mostek's MK30000/MK-34000 and MK36000 (8K/16K and 64K ROMs respectively), a circuit has been incorporated with the standard design that has minimized process and temperature dependence. This circuit called a substrate bias generator, compensates for variations in the threshold voltage due to temperature excursions, aging and other conditions. While the substrate bias generator is and has been utilized on various circuits, the approach used by Mostek presents an innovative departure from the old idea.

Threshold Voltage

One of the most critical parameters in an N-channel MOS circuit is threshold voltage (V_T), or the minimum voltage potential required to be applied to the gate of an MOS device to turn the device on. Threshold voltage can be defined by the following set of equations:

$$\text{Eq. 1} \\ V_T = V_{FB} + 2\phi_B + \frac{\sqrt{2E_s q N_A (2\phi_B)}}{C_o}$$

$$\text{Where } V_{FB} = \phi_{ms} + \frac{Q_{fs}}{C_o}$$

$$\phi_B = \frac{kT \ln(N_A)}{q \left(\frac{n_i}{n_i} \right)}$$

ϕ_{ms} = metal/silicon work function

Q_{fs} = surface charge density/unit area

C_o = gate capacitance/unit area

The term Q_{fs} can also be divided into several components that will help to show how it is process dependent. It would include a term for the fixed surface charge on the Si/SiO₂ interface - Q_{ss} , a term for oxide ion contamination - Q_s , and also some secondary terms which have only minor effect. Table I summarizes how each term is affected by the process.

Table 1

PARAMETER	PROCESS
N_A	Impurity concentration in gate region.
ϕ_{ms}	Gate metal (poly silicon/aluminum)
Q_{fs}	Crystal orientation, oxide growth technology, mobile gate oxide contamination, oxide charge due to ionization.
C_o	Gate oxide thickness, density of dielectric.

Many different process techniques have been developed over the past few years to better control each of the above terms, so that any chosen optimum V_T can be as reproducible as possible. Mostek for example, pioneered the use of ion-implantation as a means of controlling the N_A term. Utilizing a 1-0-0 crystal orientation which has the lowest number of surface states on the Si/SiO₂ interface will minimize the Q_{fs} term. However, it is still very difficult to maintain a high percentage of the threshold distribution at the desired value. In a production environment a V_T distribution of $\pm 250\text{mV}$ is generally considered to be good.

This situation presents the MOS designer with a number of problems. He must take into account the fact that the V_T 's as well as other important parameters will vary considerably from their ideal values. The design must be done on a basis of worst case conditions. Therefore, the designer is forced into a trade-off position between an ideal speed-power product and circuit stability. Obviously a superior circuit design would be achievable if the designer was assured that the V_T 's would always be at their optimum values over the specified operating conditions in a system.

To the system designer, threshold voltage manifests itself in many ways in the actual operating characteristics of the circuit. Input high and low levels are directly dependent upon V_T . This in turn will determine noise margins of the circuit. Power supply tolerances and output drive capability also depend on thresholds. Due to the intrinsic dependence of V_T with temperature, the operating temperature range of a circuit and in turn the system is limited.

It is evident that if thresholds could be maintained at their optimum values regardless of process variations and temperature excursions, a superior I.C. is

possible. As a consequence the system designer is given the greatest latitude in his design tolerances.

Controlling Thresholds with V_{BB}

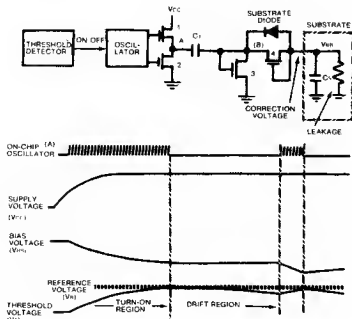
The effective threshold voltage of a MOS device can be shifted from the process controlled value defined in Eq. 1 in the following manner:

Eq. 2 $V_{T\text{eff}} = V_T + \Delta V_T$

The ΔV_T term is caused by the addition or subtraction of an electric field at the gate region, which is generally due to some negative potential applied to the substrate of the circuit. This potential is commonly known as back bias or V_{BB}. In dynamic RAMs for instance, a typical V_{BB} of -5 volts is used in order to shift thickfield thresholds to higher values and to reduce junction capacitances. However, until recently, the idea of making V_{BB} variable in order to precisely control thresholds has been overlooked. Mostek has utilized this idea in all of its new ROM designs by means of an on chip substrate bias generator. This bias generator, or "charge pump" as it is often called, is capable of supplying between -5V to -3.5V to the substrate in order to maintain thresholds at their most desirable levels. Since V_{BB} is generated internal to the device, many of the problems associated with an external V_{BB} supply are avoided. Generally an external supply has to be well regulated and may require a special sequencing with the other supplies used. If this external V_{BB} supply is lost, the circuit may become catastrophically damaged or the longterm reliability can be adversely affected.

CHARGE PUMP

Figure 1



The charge pump is actually a gated oscillator which is controlled by a threshold detector. (See Figure 1) The threshold detector compares the thresholds of the circuit with an on chip voltage reference (V_R). This reference is not threshold dependent; rather, it is a voltage which remains at a fixed percentage of the V_{CC} power supply.

The operation of the charge pump can be understood by a careful examination of the power-up sequence illustrated in the left portion of Figure 1. When the V_{CC} supply is first turned on the threshold detector compares the unbiased V_T's (threshold voltage at V_{BB}=0V) with the reference voltage V_R. The unbiased

V_T's are set by the process at about .5 volts below the optimum value. The threshold detector sees this difference and turns on the oscillator. The substrate voltage will go more negative each time the charge from C₁ is dumped into C_s (the substrate capacitance).

During the first part of the cycle, device 1 turns on pulling node (A) to V_{CC} while node (B) is held approximately at V_T. The second part of the cycle, node (A) is pulled to ground by device 2. This forces node (B) below the V_{BB} node. Device 4 conducts and puts more charge on the substrate capacitor C_s. As V_{BB} goes more negative, the effective thresholds begin to rise correspondingly. When V_{BB} reaches a magnitude sufficient to raise V_{T_{eff}} to its desired value, the threshold detector turns off the oscillator.

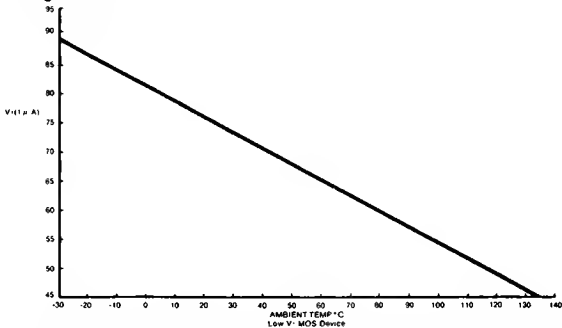
During normal operation, substrate leakage will tend to decrease V_{BB} and thus V_{T_{eff}}. The threshold detector however is sufficiently accurate that it can see these small changes and again activate the oscillator in order to bring V_{T_{eff}} back to its nominal level. This is shown in the right half of Figure 1.

Advantages of the Charge Pump

The advantages of a charge pump should be obvious. Because thresholds are no longer entirely dependent upon process parameters, much tighter V_T distributions are possible. Instead of V_T spreads of 400mV-500mV the circuit designer can expect to see distributions as tight as ±25mV. To the user this means much wider operating tolerances while maintaining optimum performance in the circuit.

THRESHOLD VOLTAGE VS. AMBIENT TEMPERATURE FOR A TYPICAL LOW V_T MOS DEVICE

Figure 2



The most important aspect of the charge pump is how it compensates V_{T_{eff}} over temperature. All MOS circuits exhibit degrading characteristics as the ambient temperature varies. This is primarily due to the intrinsic dependence of V_T upon temperature. Virtually every term in Eq. 1 has some linear or logarithmic temperature dependence. The overall effect of this is illustrated in Figure 2. It appears as a linear decrease of V_T with increasing temperature at an approximate 2.7mV/°C rate. The limit to the operating range of a circuit can occur when the device thresholds shift to such an extent that either a DC level problem occurs within some critical inverter stage or the device no longer meets the required input or output levels.

VT (1μA) VS. AMBIENT TEMPERATURE WITH CHARGE PUMP

Figure 3

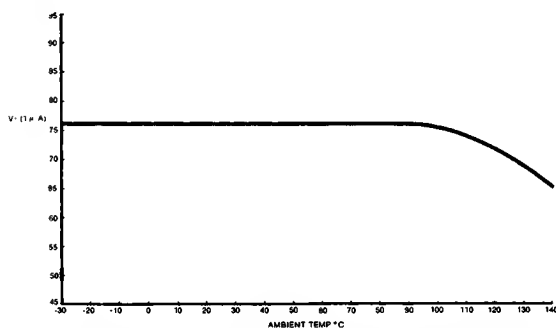
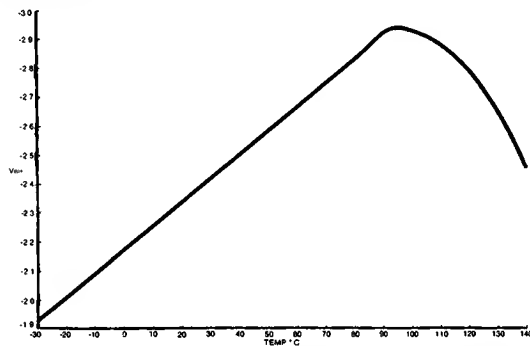


Figure 3 illustrates how the charge pump helps to overcome the problem. The data shown represents values typical of measurements taken from several manufacturing lots of the MK34000. Thresholds were found to be virtually constant from -35°C (the lower temperature limit of the experiment) up to about 95°C. Beyond 95°C, substrate leakage began exceeding the current capability of the charge pump. As a result V_T 's begin falling at a rate close to the 2.7mV/°C typical of any low threshold MOS device. Figure 4 illustrates how V_{BB} varied with temperature in order to maintain the V_T 's shown in Figure 3.

VBB VS. AMBIENT TEMPERATURE WITH CHARGE PUMP OPERATIONAL

Figure 4



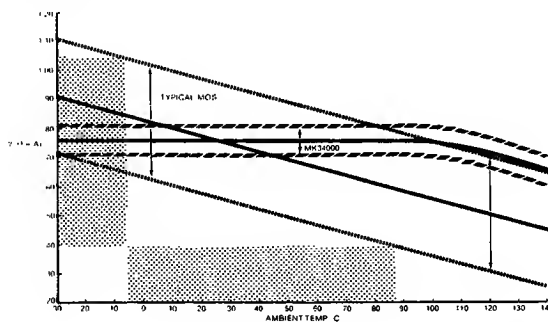
The real significance of the above is best seen when comparing Figures 2 and 3 on the same plot along with the limits of the distributions. This is graphically shown in Figure 5. A typical low V_T MOS device might be capable of operating over a range of thresholds from .40V to 1.05 volts. If an MOS circuit could be designed and processed repeatedly with ideal thresholds, the operating temperature range would be very wide. Since it cannot be done that accurately and consistently the operating temperature is more limited as shown by the typical MOS curve in Figure 5. For example, if it is assumed the device will not properly operate outside the .40V to 1.05V V_T range, then the

device will only operate from -6°C to +87°C. Outside of this range, the processing tolerances of the non-charge pump part do not allow proper operation.

As can be seen in Figure 5, with the charge pump working, V_T is much tighter around the nominal value.

COMPARISON OF THRESHOLD DISTRIBUTIONS FOR A TYPICAL MOS DEVICE WITH AND WITHOUT A CHARGE PUMP

Figure 5



Even with large variations in the no bias V_T , the pump sufficiently compensates to keep $V_{T\text{eff}}$ well within its operating tolerances over a wide range in temperature. This means the circuit can be expected to operate over a much wider temperature limit with no significant change in V_T .

The result is the charge pump has its greatest effect on the input levels of a circuit. It allows the designer to process the circuit to a V_T level that gives the best speed/power product commensurate with the TTL level inputs. In a normal production situation on an uncompensated device, the thresholds would have to be set artificially high to allow for process and temperature tolerances on V_T . The following shows how the charge pump effects this situation.

In an MOS device, the lower limit that can be tolerated on V_T is determined by the input low level. On a 5 volt only ROM such as the MK 34000, the lower limit on V_T is set at .5 volts. This number is the lowest V_T tolerable for proper operation of the part. The upper limit to V_T can be determined by the following equations.

$$\text{EQ 3 } V_{TNOM} = V_{T\text{ lower limit}} + \Delta V_{TT} + V_P$$

$$\text{EQ 4 } V_{Tupper} = V_{TNOM} + \Delta V_{TBE} + \Delta V_{TT}$$

where V_{TNOM} = Nominal V_T excluding tolerances

$$V_P = \text{Process tolerance of } V_T$$

$$\Delta V_{TBE} = \text{Change in } V_T \text{ due to body effect}$$

$$\Delta V_{TT} = \text{Change in } V_T \text{ due to temperature}$$

In Eq 3 the nominal V_T will be set by the lower limit of V_T plus whatever process and temperature tolerances have to be allowed for. Using the numbers mentioned before, where $V_P = \pm 250\text{mV}$ and $\Delta V_{TT} = -300\text{mV}$ (over

range of -55°C to $+125^{\circ}\text{C}$ centered at R.T.), it can be seen that V_T nominal is 1.05V. The upper limit to V_T would be 1.05V plus V_P (250mV) and $\Delta V_{T\tau}$ (200mV) or a total of 1.5V. The designer in this case would have to set the process V_T to 1.05 volts and design the circuit to operate over a range of .5 volts up to 1.5 volts.

This in itself may not be an unsolvable problem, however, the ΔV_{TBE} term has been neglected. At the upper level of V_T a problem occurs with the output high level. Equation 5 shows why.

$$\text{EQ 5 } V_{OH \text{ max}} = V_{CC} - V_{Tupper} - \Delta V_{TBE}$$

where $V_{CC} = 5 \text{ volts} \pm 10\%$

$$V_{Tupper} = 1.5\text{V}$$

If V_{CC} is taken to be at the lower tolerance (4.5V) and $V_{Tupper} = 1.5$ volts then ignoring the ΔV_{TBE} term puts the maximum output high level at 4.5 volts - 1.5V or 3.0 volts. By the time the body effect term is subtracted, the level may be below 2.0 volts which is unacceptable in a TTL compatible product.

By going thru the same analysis with the charge pump operational, and using the following numbers for V_P and $\Delta V_{T\tau}$, it can be shown that the process V_T can be set at a much lower level than before.

$$V_P = \pm 50\text{mV}$$

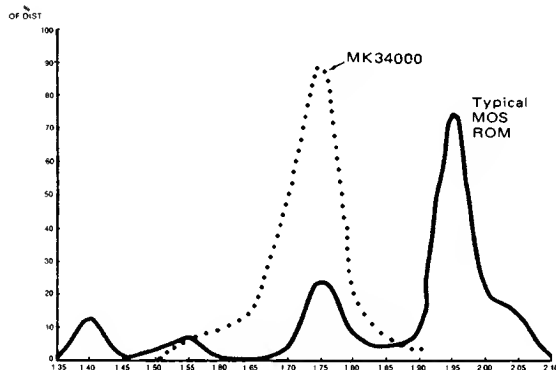
$$\Delta V_{T\tau} = \pm 100\text{mV}$$

This fact helps to optimize the speed power/product of the circuit while allowing true TTL compatibility on the inputs and high drive capability on the outputs.

Figures 6 and 7 show the distribution of input levels of uncompensated and compensated 16K ROMs. Although these are room temperature distributions, extending the temperature would tend to further widen the uncompensated distribution.

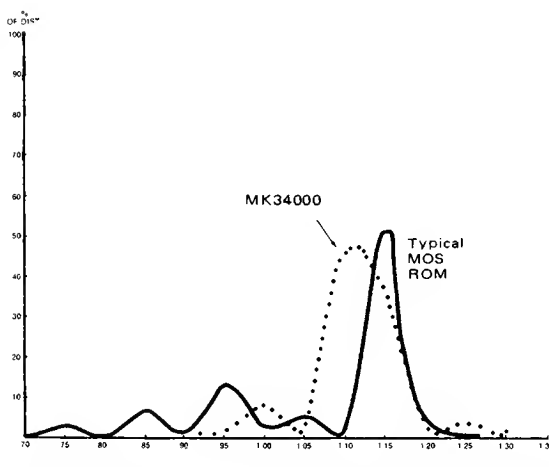
INPUT HIGH LEVELS

Figure 6



INPUT LOW LEVELS

Figure 7



As was eluded to above, output drive is at least partially enhanced by the operation of the charge pump in two ways. Since V_{TNOM} is lower, the overall output drive is made larger (see Eq 5). Over temperature (particularly from -55°C to $+125^{\circ}\text{C}$) the charge pump holds V_T constant, which in turn keeps output drive at a higher level.

Also with a compensated device, a power supply tolerance of $\pm 10\%$ is more easily accomplished. Again referring to Equation 5, if the upper limit of V_T is abnormally high, then the amount of tolerance on the power supply is reduced. On an uncompensated device, the V_T makes it extremely difficult to design an input stage with true TTL levels. Since the reference voltage V_R is kept at a fixed percentage of the V_{CC} supply, the output level will not decrease by the total change in V_{CC} , if V_{CC} should decrease. Rather output drive would only decrease by an amount determined by the fixed percentage that V_R is of V_{CC} .

User Benefits

The user benefits created by the charge pump are quite obvious. It is no longer necessary to utilize an external power supply (requiring regulation) to accomplish the tasks of shifting the operating thresholds and reducing junction capacitance. The substrate bias generator performs these functions with only a slight increase in circuit power dissipation (typically 5mW) and not a significant increase in overall chip size. This saves the cost of an extra supply with a non-significant increase in the I.C. price.

The charge pump allows the circuit designer and thus the system designer greater design tolerances, as witnessed by the MK30000 and 34000 performance specifications. It gives the system designer $\pm 10\%$ power supply tolerances while allowing greater output drive. This can be a significant advantage in a 5 volt only ROM. Input levels can be specified at true TTL levels providing the widest noise margins possible when used with high performance control circuitry such as standard TTL or Schottky TTL.

Power dissipation is kept to a minimum while access time is the fastest of any 5 volt only ROMs available. Due to the charge pump compensating for V_T changes with temperature the specified operating temperature range can be increased to -55°C to $+125^{\circ}\text{C}$ with only minimal loss in system performance (namely access time and power dissipation).

Another important factor is cost. The charge pump narrows the V_T distribution of the MK30000/34000 and MK36000 making them highly repeatable and manufacturable products. This not only reduces the device costs but increases yields, reducing the lead time for production quantities because of an increased number of available chips.

MOSTEK®

MOS READ-ONLY MEMORIES

ROM Programming Guide

ROM PROGRAMMING GUIDE

It has always been MOSTEK's policy to service its customers ROM needs in the most efficient way possible. In continuing with this effort, MOSTEK has revised its ROM Procedure to better facilitate the market we serve. This new ROM programming guide and information form will insure that all pertinent information is received with the purchase order. This will reduce the unnecessary delays which develop when sufficient information is not available.

DESCRIPTION OF ROM FORM

The first part of the ROM programming form is concerned with providing all necessary customer information to MOSTEK. This will simplify any correspondence which may be necessary to complete the order in question.

The ROM generic type simply indicates the ROM series the customer wishes to purchase. This includes the following MOSTEK series:

MK2300 Series
MK2400 Series
MK2500/2600 Series
MK28000 Series
MK30000 Series
MK31000 Series
MK34000 Series
MK36000 Series

PACKAGE TYPE

The package type must be included on both the ROM form and the purchase order to prevent parts being produced in the wrong package. Currently, all prototypes and any follow-on quantities built in Dallas will be ceramic. Remember: P = Ceramic, N = Plastic.

CUSTOMER NUMBERS

In the event the customer assigns a part number to the MOSTEK ROM selected, this number should be entered on the ROM form. This number will simplify any communication which may be necessary between the customer and MOSTEK.

SPECIAL BRANDING

Special branding of MOSTEK ROMs is possible if the instructions are indicated on the ROM programming form. But due to space and printing limitations, any special branding desired must be limited to 10 characters on one line.

CUSTOMER SPECIFICATIONS

If the customer desires different specifications for the ROM selected than appears on the appropriate MOSTEK data sheet; it is imperative that these specification changes be well documented and sent to MOSTEK as early as possible. This is important because any specification change must be reviewed and accepted by MOSTEK before the ROM order can be processed.

ROM DATA

MOSTEK will accept a number of media and formats for the inputting of programming data. This flexibility will make it easy for a customer to have his ROM order processed as quickly as possible. In all cases the actual ROM contents is preceded by four header cards or records which contain important programming information such as chip select codes, logic, and verification codes. Refer to the appropriate MOSTEK data sheet for the description of the header cards and the MOSTEK format for the actual ROM data. The following table shows the formats and media that can be most easily processed by MOSTEK. When filling out the ROM programming form, check the appropriate block under pattern media.

PATTERN MEDIA

Punched Cards: Use standard 80 column cards punched as per the applicable format. MOSTEK's four header cards must be included.

Paper Tape: Use 1", 7 or 8 bit ASCII coded paper or mylar tape. Tape records should be card images ending with a carriage return and line feed if a card format is being used.

ROMS/PROMS: On MOSTEK's ROMs of 4096 bit and larger density, PROMs of the 2708 and 2716

ROMS

type or pin compatible ROMs may be submitted for the ROM contents. They must, however, be accompanied by the header cards required for the MOSTEK ROM type or that information in written form. Each PROM or ROM submitted must also be clearly marked so that no question arises as to its starting memory location.

VERIFICATION MEDIA

For pattern verification, MOSTEK can supply either a printout, paper tape, card deck, or reprogrammed PROMs. Formats of cards and tapes are as shown in the table of acceptable formats.

To insure rapid turnaround of data verification information, acceptable media and formats should be used as outlined in the tables. If another method is desired, contact MOSTEK so that all arrangements can be made and an accurate schedule can be generated. Quick turnaround of verification information cannot be guaranteed in cases where new software has to be developed. Remember, when filling out the ROM programming form, check the appropriate block under verification media.

HOW THE PROGRAM WORKS

MOSTEK's ROM program is designed for maximum safety with two verification steps that limit the liability of both the customer and MOSTEK. However, if circumstances dictate, MOSTEK is flexible enough to vary its procedures to better serve its customers.

PATTERN VERIFICATION

Upon receipt of the ROM programming information form and the ROM input data, MOSTEK engineering will re-generate the pattern data for customer verification. At this point, no liability is incurred for either party. Following customer verification, MOSTEK begins prototype production. This verification step can be waived so that prototype production begins immediately upon receipt of the input data. The time savings is the time for MOSTEK engineering to generate verification plus the time necessary for the customer to receive and verify the data. This savings is usually less than two weeks. If data verification is waived, the customer is liable for the mask charge plus the prototype parts.

PROTOTYPE VERIFICATION

The second verification step in MOSTEK's ROM Program is that of prototype verification. The prototype quantity is usually 25 parts which are considered part of the order quantity for billing purposes. After the customer has verified the prototype, in writing, as being correct, MOSTEK will proceed with the production of the total remaining order.

The prototype verification step can also be waived and MOSTEK will immediately begin production instead of prototype. The time savings gained from waiving prototype verification is usually 5-6 weeks. If prototype verification is waived, the customer is liable for the mask charge plus all work-in-process material if a customer mistake occurs.

WAIVERS OF VERIFICATION

Arrangements must be worked out with MOSTEK prior to committing deliveries based on verification waivers. If an order is accepted by MOSTEK waiving pattern verification, the quoted cycle time begins upon receipt of the input data and only a small quantity of parts will be produced as prototypes. If MOSTEK accepts an order waiving prototype verification, the quoted cycle time will begin upon notification of pattern verification.

GENERAL INFORMATION

Production capacity cannot be reserved without a purchase order. Therefore any quotes for delivery will be subject to change until a purchase order is obtained.

Moderate quantities of parts are usually available from the MOSTEK Dallas Assembly facility shortly after prototype shipments. These units will always be ceramic packages and, if delivered in less than 8 weeks after prototypes, will require a \$2.00 per unit adder in addition to the ceramic package price.

The appropriate MOSTEK price sheet contains information on order minimums and price adders.

ACCEPTABLE MEDIA				
MK TYPE	CARDS	PAPER TAPE	ROM	PROM
MK2300P Series	X	X		
MK2400P Series	X	X		
MK2500/2600P Series	X	X	X	
MK28000P/N Series	X	X	X	X
MK30000P/N Series	X	X	X	X
MK31000P/N Series	X	X	X	X
MK34000P/N Series	X	X	X	X
MK36000P/N	X	X	X	X

READ ONLY MEMORIES

DEVICE	ORGANIZATION	LOGIC	NUMBER BITS	ACCESS (ns)	SUPPLY VOLTAGES					POWER DIS (MW) MAX	PACKAGE	
					V _{DD}	V _{GG}	V _{BB}	V _{CC}	V _{SS}		TYPE	PINS
MK2300	64x7x5	Static	2240	1000	0	-12			+5	750	Ceramic	24
MK2400	256x10	Static	2560	500	0	-12			+5	850	Ceramic	24
MK2500	512x8 or 1024x4	Static	4096	700	0	-12			+5	950	Cer/Plas	24
MK2600	512x8 or 1024 x 4	Static	4096	700	0	-12			+5	950	Cer/Plas	24
MK28000	2048x8 or 4096x4	Dynamic	16384	600		-12			+5	1000	Cer/Plas	24
MK30000	1024x8	Static	8192	450				+5	0	TBD	Cer/Plas	24
MK31000	2048x8	Static	16384	550				+5	0	300	Cer/Plas	24
MK34000	2048x8	Static	16384	350				+5	0	330	Cer/Plas	24
MK36000	8192x8	Dynamic	65536	250				+5	0	220	Cer/Plas	24

ROM CROSS REFERENCE

MOSTEK	AMD	INTEL	MOTOROLA	AMI	FCLD	SYNERTEK	NATIONAL	EA	G.I.
MK2500P				S5232			MM4232/5232		
MK2600P	AM9214			S3514	3514				
MK28000P/N								EA4800/4900	
MK30000P/N*	AM9208	2308/8308						EA2308A	
MK31000P/N		2316A/8316A		S6831A		SY2316A			RO-3-8316A/8
MK34000P/N		2316E/8316E	MCM68316E	S68318		SY2316B			RO-3-9316A/8
MK36000P/N									

* MOSTEK's MK30000 operates from +5 volts only

** User must consult the applicable MOSTEK Data Sheet for timing conformance.

ROMS

ACCEPTABLE FORMAT

MK TYPE	MOSTEK	NAT	FCLD	INTEL CARD	INTEL TAPE	EA	MOSTEK F-8	MOT 6800
MK 2300P Series	X							
MK 2400P Series	X							
MK 2500/2600P Series	X	X	X					
MK 28000P/N Series	X					X	X	X
MK 30000P/N Series	X			X	X	X	X	X
MK 31000P/N Series	X			X	X	X	X	X
MK 34000P/N Series	X			X	X	X	X	X
MK 36000P/N Series	X			X	X	X	X	X

ROM PROGRAMMING FORM

CUSTOMER NAME _____		
ADDRESS _____		
CITY _____	STATE _____	ZIP _____
PHONE (____) _____	EXTENSION _____	
CUSTOMER CONTACT _____	TITLE _____	
MOSTEK REP. OR DIST. _____		

ROM Generic Type _____

Package Type _____

Customer Part Number _____

Branding Requirement _____

Customer Specification:	Yes	Parts to be tested to standard Data Sheet
	No	

Date customer spec sent to MOSTEK _____

PATTERN MEDIA <input type="checkbox"/> PROM (2708/2716) <input type="checkbox"/> PIN COMPATIBLE ROMS <input type="checkbox"/> PAPER TAPES <input type="checkbox"/> CARD DECK <input type="checkbox"/> TAPE OF CARD DECK <input type="checkbox"/> OTHER - NOTE 1	VERIFICATION MEDIA <input type="checkbox"/> PROM (2708/2716) <input type="checkbox"/> PIN COMPATIBLE ROMS <input type="checkbox"/> PAPER TAPES <input type="checkbox"/> CARD DECK <input type="checkbox"/> TAPE OF CARD DECK <input type="checkbox"/> OTHER - NOTE 1
--	---

NOTES: (1) Other Media Require Factory Approval

Date Pattern Data Sent to MOSTEK _____

Does Customer Require Prototypes Yes____ No____

Pattern Verification Required by Customer

Yes		Waived	
Yes		Waived	

Prototype Verification Required by Customer

COMMENTS: (waiver explanation)

Customer Order Number	_____
Date of Customer Order	_____
Distributor Order Number to MOSTEK	_____
Order Quantity and Price	_____
Delivery Requested/Committed	Prototypes _____ Production _____
Date Form Completed	_____

A 64K ROM using standard N-channel silicon gate technology will be described. Cell layout affords a small die area for a given number of bits, while differential sensing and dynamic clocking has permitted the combination of high speed and low power. Operating from a single 5V supply, the chip has a typical access time of 80ns and typical power of 150mW. The cell area is 0.25mils² (158μm²) and the overall chip area is 183 x 190 mils; 4.65 x 4.83mm.

BLOCK DIAGRAM OF 64K ROM

Figure 1

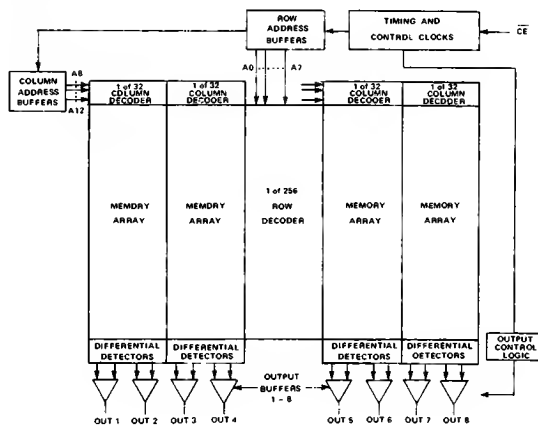


Figure 1 shows a block diagram of the circuit, and a photograph of the device is shown in Figure 2. The chip is organized as 8K words by 8 bits per word. The memory array is divided into four 16K quadrants, each containing the data for two outputs. The column decoders provide a 1 of 32 selection and the row decoders a 1 of 256 selection.

The schematic diagram of the basic cell and the interfacing differential sense amplifiers is shown in Figure 3; photograph of cell appears in Figure 4. The small cell area was achieved by sharing not only the outputs of each cell, but also by sharing the virtual ground line between cells, resulting in only 1/2 contact per memory cell. Programming of information in the array has been achieved by selecting which devices in the array receive a threshold modifying implant.

The negative going edge of \overline{CE} starts an internal timing chain of dynamic clocks. These internal timing edges latch in addresses, which provide dynamic X-Y decoding, and transfer data through a set of differential

amplifiers and latching flipflops to the output buffer. The chip then automatically goes back into precharge mode except for the static output buffers which trap data until the positive going edge of \overline{CE} open-circuits the outputs.

The memory cell and differential amplifier shown in Figure 3 operate as follows. During precharge (\overline{CE} high), all data buses, output buses, and column lines are clamped to the 5V supply, V_{CC} . This is done with depletion transistors to avoid a threshold voltage loss. The negative-going edge of \overline{CE} starts the internal timing clocks bringing the precharge clock, PC, to ground which leaves the data lines floating and equilibrated at V_{CC} . After decoding takes place, the selected poly row line is driven to V_{CC} , applying gate drive to both the reference cell transistor T11, and the memory cell transistors, T8, T9, and T10. For this example, assume that the cell transistors are programmed to a "0" or low threshold. Both the selected column, COL_N and the reference column are pulled to ground (V_{SS}) turning on the reference transistor T11 and a pair of cell transistors, T9 and T10. The reference data line, node 22, and the two data lines, nodes 11 and 13 begin to discharge. The widths of the cell and reference transistors are in a ratio such that the cell transistors, T9 and T10, discharge the data lines at about twice the rate as the reference transistor, T11, discharges the reference data line. At the same time COL_N is discharging to ground, the differential amplifiers are activated through devices T3 and T6. As a signal difference develops between the reference data line, node 22, and the data lines, nodes 11 and 13, the differential devices T1 and T2, and T1 and T5 produce true and complement data on the output bus lines, nodes 17 and 18, and nodes 19 and 21. When a few hundred millivolts of differential signal is available on the output buses, this information is latched by cross coupled flipflops in the appropriate output buffer. This information then steers the output clock enable signal to either the pull-up or pull-down drivers of the output buffer. If a "1" had been programmed into the cell, the cell transistors would have had a high threshold and the data lines in the array would remain high. This would produce complement data on the output buses.

For every column access, a pair of cells and differential amplifiers are activated. The memory array is split into four 16K blocks, each of which provides two outputs of the 8K words by 8 bits per word configuration. The diodes T3, T6, and T7 in the differential amplifiers serve to prevent adjacent amplifiers from becoming active when a particular column line is accessed. The depletion clamp, T17 serves to hold the adjacent column line at V_{CC} , further avoiding potential noise contributions from adjacent cells.

Figure 5 shows a photograph of typical access time for nominal supply and temperature conditions and Table 1 shows a summary of the device characteristics.

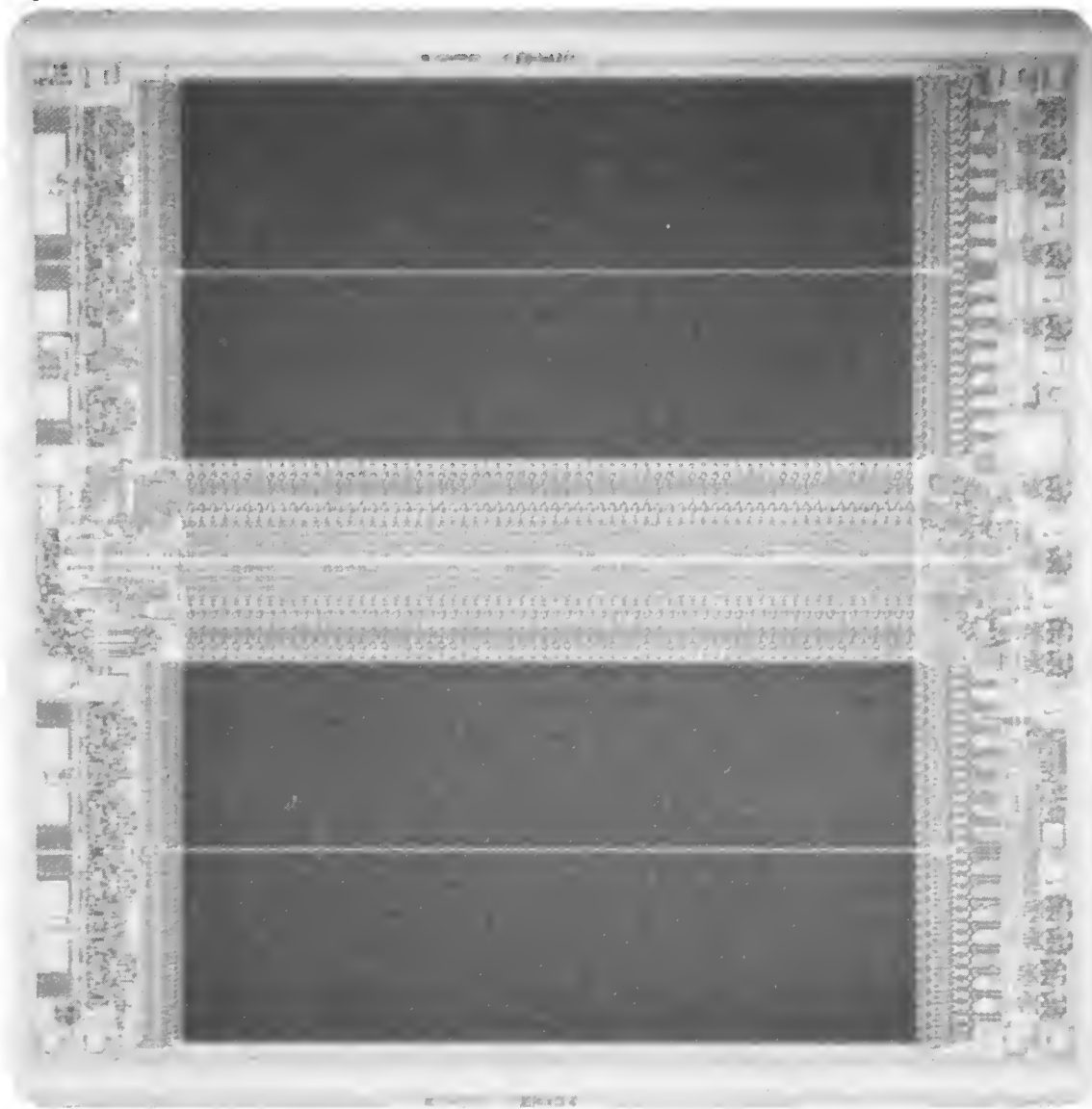
TYPICAL CHARACTERISTICS OF 64K ROM

Table 1

Technology	N Si Gate
Cell size	0.25 mil ²
Die size	183 x 190 mils (34.770) mil ²
Access time	80ns
Cycle time	150ns
Supply	5 (±10%)
Active current	30mA
Standby current	4mA
Input levels	2.0 0.8
Output levels	2.4 0.4

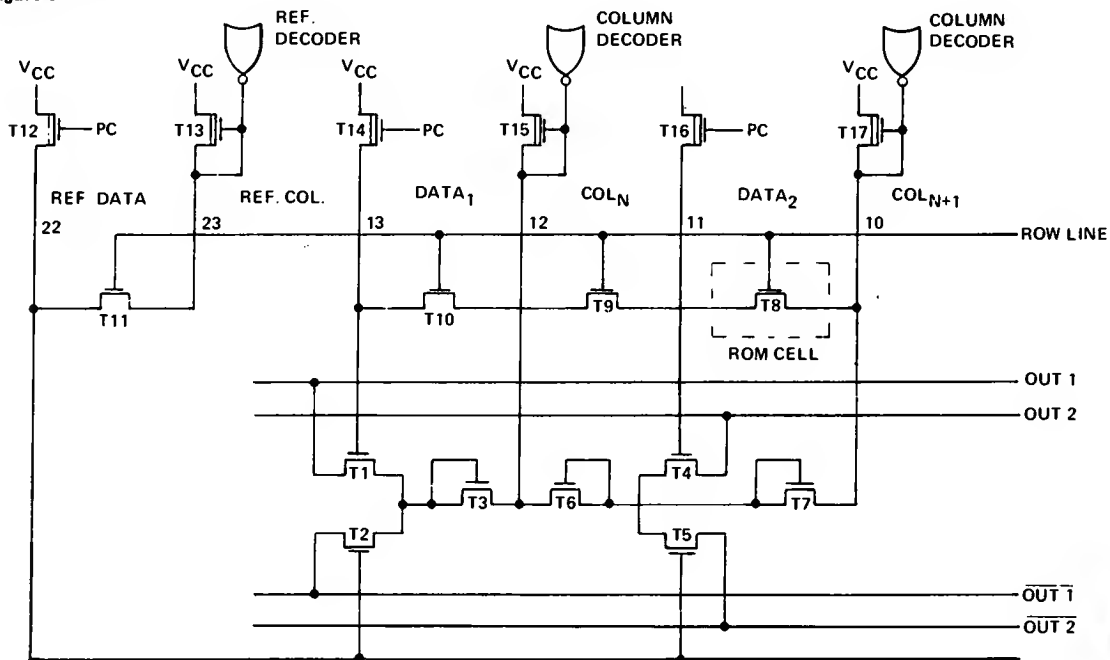
PHOTOGRAPH OF 64K ROM

Figure 2



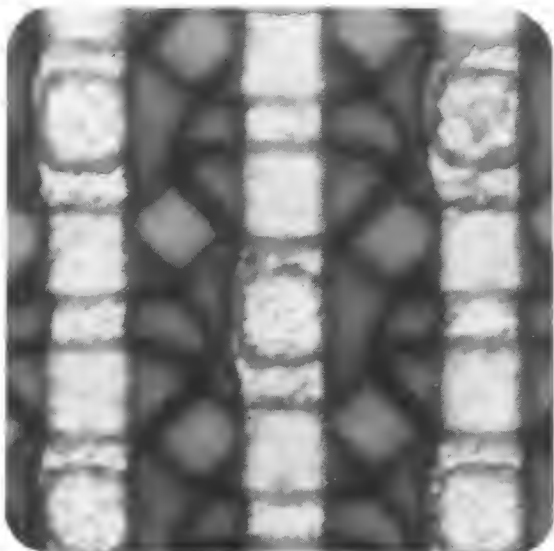
SCHEMATIC OF ROM CELL AND DIFFERENTIAL AMPLIFIERS

Figure 3



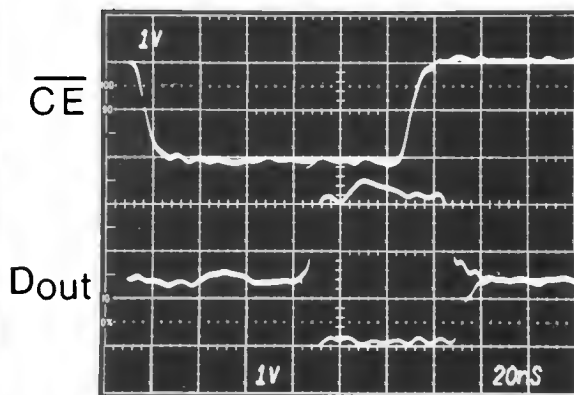
PHOTOGRAPH OF ROM CELL

Figure 4



OSCILLOGRAPH OF MEMORY ACCESS TIME

Figure 5



ROMS

1980 MEMORY DESIGNERS GUIDE

X	Dynamic Random Access Memory	DYNAMIC RAMS
XI	Static Random Access Memory	STATIC RAMS
XII	Read Only Memory	ROMS
XIII	Technology	TECH-NOLOGY
XIV	Memory Systems	MEMORY SYSTEMS

Application Note

INTRODUCTION

The proliferation of low cost microprocessors has created many new opportunities and challenges. With involvement of the microprocessor the need for specialized memory components has emerged. Mainframe memory designs of the past tended to be large in bit content with various word widths. Microprocessor memories, in contrast, are typically smaller in size with word widths fixed at X8 or X16 bits. This X8, or byte orientation, has given birth to wide word memories with new opportunities for standardization.

BYTEWYDE™ memories can adapt themselves to the microprocessor as building blocks because microprocessor architectures are byte oriented. By using these building blocks, memory design can inherit flexibility and compatibility that has not existed before. The design of custom memory arrays can be reduced to the mere insertion of components which directly match the microprocessor software requirements.

In memory design, various types of devices are more suited for a given application than others. The wide spread popularity of RAM, ROM, and EPROM validates the need for different types of memory devices. A truly non-volatile RAM could remove this complication. Since this device does not yet exist memory designers must decide, and usually very early in the design, how much and what type of memory components to use. Nevertheless a coherent memory packaging philosophy can resolve many problems associated with type, size, and expansion. The benefits of such an approach can be:

- (1) RAM, ROM, EPROM interchange
- (2) Upgradeability to higher density components
- (3) Single component incremental expansion

ROM and PROM interchangeability has existed for some time. This convenience has been used with non-volatile memory to reduce memory cost after system confidence has been established by substituting ROM for EPROM in high volume applications. The availability of RAM with pin compatibility has furthered the process of interchangeability. Memory design, as a result, is less restrictive in that exact amounts of ROM vs RAM may be decided virtually after the design has been complete.

Socket upgradeability presupposes that a higher density

part will exist and that the future part may be substituted for a former lower density part. Good memory designers will use the maximum density part available to reduce P.C. board space and cost; however, less clearly understood is that density of components doubles every 18 to 24 months. This seems to say with some certainty that a memory design which uses current state-of-the-art density will be out-dated in two years because of reduced cost effectiveness. However, many equipment manufacturers need 4 to 6 years of product life. Upgradeability allows not only the option for substituting new, higher density parts; but provides the solution to remaining price competitive. The wasteful practice of providing real estate consuming spare sockets for probable future development can be eliminated by allowing technology advances to provide expansion. Furthermore, a given matrix of memory can be populated to exact requirements with single component incremental expansion provided by BYTEWYDE organizations.

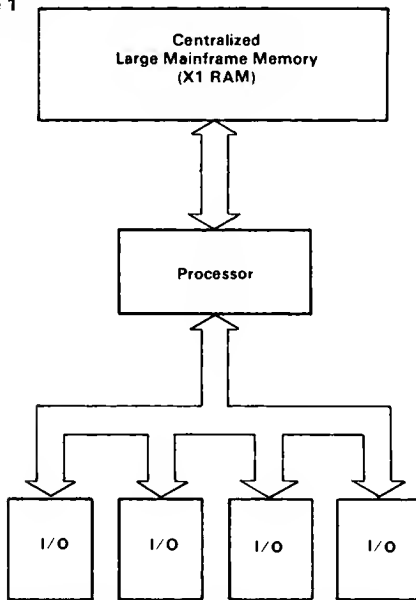
PACKAGE COMPATIBILITY

The 24 pin DIP has become the standard for presently available X8 memory devices. As the density of devices increases, more address pins will be needed to define higher density devices. This will create a need for future parts to occupy more than 24 pins. A logical choice is a 28 pin DIP package with the same pin spacing and package width differing only in the length occupied by the 4 additional pins. The key to future compatibility resides in the accepted 24 pin package pinout of today, and a 28 pin printed circuit board layout which is mutually inclusive of 24 and future 28 pin devices.

Mostek is dedicated to such an approach with its BYTEWYDE concept. This concept is particularly well suited for applications where the localized memory requirement can be implemented in 8 or less packages. Today, 80% of all 8 bit multi-chip microprocessor applications fall into this category. The future trend to distributed processor system architectures will emphasize smaller concentrations of memory localized in one area, although; the overall system requirement for memory will be substantial. Figure 1 shows the more traditional mainframe computer architecture of the 70's and Figure 2 shows the trend for the 80's using multiple microprocessors. Before proceeding to the packaging

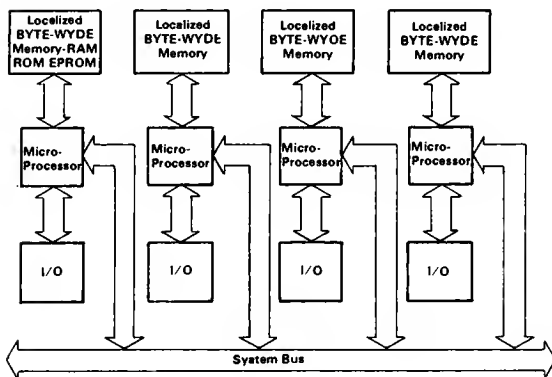
MAINFRAME COMPUTER ARCHITECTURE

Figure 1



MULTIPLE MICROPROCESSOR TREND OF THE 80's

Figure 2



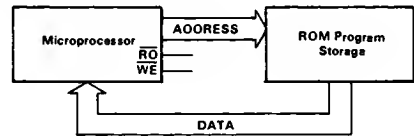
philosophy of BYTEWYDE memory control functions will be discussed.

MEMORY CONTROL FUNCTIONS

Memory control functions are provided to simplify interface and allow full utilization of performance. Historically, consistency in control functions has proved difficult. This is because control functions occupy pins which compete with address lines needed for future higher density parts. Three control functions have become very popular: chip enable, output enable, and write enable.

PROCESSOR/MEMORY INTERFACE - NO CONTROL FUNCTION

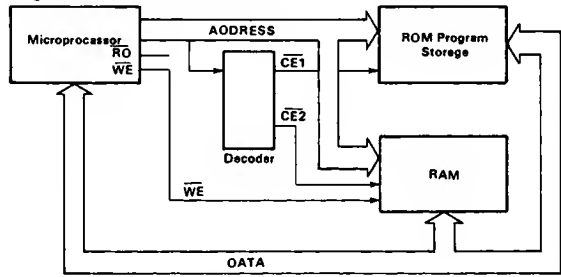
Figure 3



Insight into control functions can be gained by a few simple examples. The simplest case is a ROM processor interface in which addresses are supplied and data falls out at access time (Figure 3). No requirement for a control function is apparent. It is not until a second memory element is added that the need for the control function \overline{CE} becomes evident (Figure 4). Since the microprocessor must now decide between the ROM and the other memory for a given access, some method must be provided to control device selection. The highest level selection control is called chip enable (\overline{CE}) by convention.

PROCESSOR/MEMORY INTERFACE - \overline{CE} , WE CONTROL

Figure 4



To reduce costly interconnects most microprocessors have a common data in and data out, many have addresses time multiplexed on this same bus. To avoid bus contention, a condition where two or more devices attempt to drive the common bus at the same time, the use of the output enable (\overline{OE}) memory control is often desirable.

PROCESSOR MEMORY INTERFACE \overline{CE} , WE, \overline{OE} CONTROL (MULTIPLEXED A/D BUS)

Figure 5

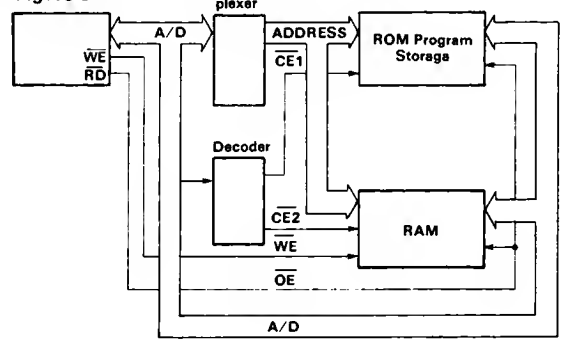


Figure 5 illustrates one of the many uses of an \overline{OE} memory control. In this diagram the bus is time multiplexed, first with address then with data out to accomplish a read cycle. As soon as addresses are valid, it is advantageous to start the read cycle; however, without an \overline{OE} control the possibility exists that the memory can go low impedance before addresses clear the bus. With an \overline{OE} control, data can be held off until the bus is clear of addresses and still not impair memory access time.

A third control function is required for RAM called write enable (\overline{WE}). It is used to differentiate between read and write cycles. To achieve RAM interchangeability with ROM and EPROM, provisions for a \overline{WE} must be incorporated into the system design and device pinout.

Having shown the usefulness of \overline{CE} and \overline{OE} , a more complete description will be given:

Chip Enable - A \overline{CE} (active low signal) is used to single out a device which is to go into cycle. \overline{CE} will typically be generated from a decoder which uses the high order address lines to uniquely select a memory device among the matrix of devices. The second aspect of the \overline{CE} control is to power up the selected device from a standby mode. In the case of dynamic logic \overline{CE} activates the internal clocks necessary to complete the cycle. Use of dynamic logic within the device makes substantial power saving possible and is widely accepted. This control is located in pin 18 of today's 24 pin DIPs.

Output Enable - An \overline{OE} (active low) controls the output buffer of the memory device. This control avoids bus contention since the memory device's output can be turned on and off directly by the controller (generally a microprocessor). Data can be gated out of the selected memory device (\overline{CE} low to the selected device) at the precise time required. This control is located on pin 20 of today's 24 pin DIPs.

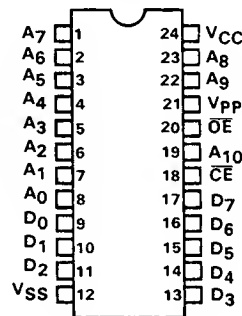
For many applications both \overline{CE} and \overline{OE} are needed to insure correct operation. The use of additional chip select signals (\overline{CS}) is viewed as redundant and serves little purpose, furthermore; it can cause compatibility problems with other memory device types. This also can have an adverse affect on upgradeability to next generation densities. If external decoding is needed, the sole advantage of additional chip selects is eliminated.

24 PIN PACKAGES

A good starting point for the discussion that will follow is the popular 2716 EPROM. The 2716 has found wide spread acceptance for microprocessor program storage. Figure 6 shows the 2716 pinout. Since this part is presently produced by no less than five manufacturers of memory devices, it may be safe to assume that this group has in itself agreed to standardization. Strengthening this assumption is the fact that many ROMs are available at the 2K level which are pinned to

2716 PINOUT - 2K x 8 EPROM

Figure 6

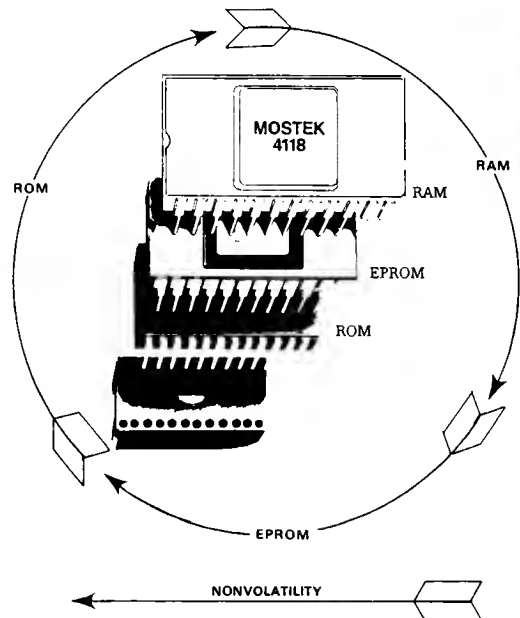


match the 2716.

The MK4118, 1K x 8 static RAM, packaged to the popular 2716 pinout, completes the compatibility circle (Figure 7). The 2716 is a 2K x 8 device requiring address line A10 as compared to the MK4118, which is a 1K device. The MK4118 (Figure 8) will interchange with the 2716 if allowance is made for the address line A10 and pin 19. A second consideration is the write enable line (\overline{WE}) required on pin 21 by the MK4118. The 2716, a ROM, does not require the write enable function. The availability of compatible 24 pin RAM, ROM and EPROM has completed the first phase of the 8YTEWYDE concept.

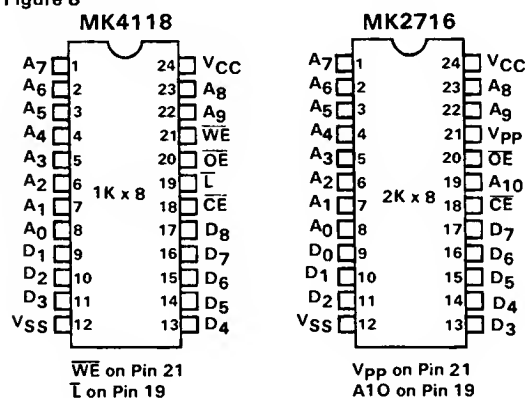
TYPES OF MEMORY

Figure 7



COMPARISON PINOUT

Figure 8



well thought out packaging philosophy. The first phase of BYTEWYDE memory standardization and its packaging philosophy has already been achieved with the 24 pin package; however, the higher density memories of the future will require a 28 pin package and the proper planning to go along with it.

These principles should be used to guide the 28 pin package assignment:

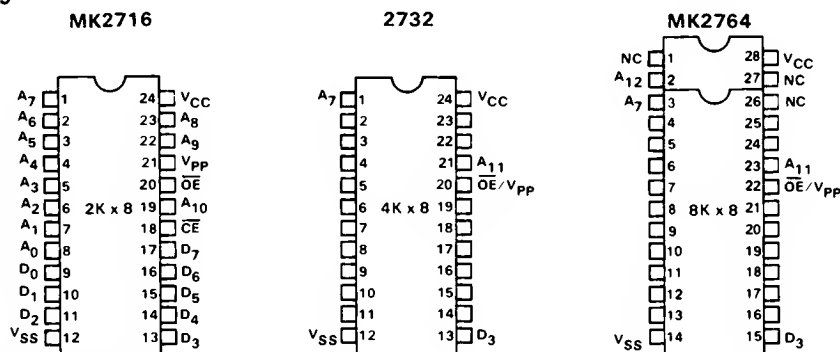
- (1) The popular 2716 pinout should be used to define address, data, \overline{CE} and \overline{OE} .
- (2) 24 pin devices should coexist with 28 pin devices by lower justification. 24 pin devices are lower justified in pin 3 thru 26 of 28 pin socket.
- (3) Consistent \overline{CE} and \overline{OE} control functions (same as 2716) should be used on all BYTEWYDE devices with provision for RAM (\overline{WE}).
- (4) Spare pins at a given density level should be no connect rather than redundant chip selects (\overline{CS}) to allow for the ultimate development and upgradability of 28 pin socket site.

FUTURE 28 PIN PACKAGING

Systems designers derive important benefits when component manufacturers discipline themselves to a

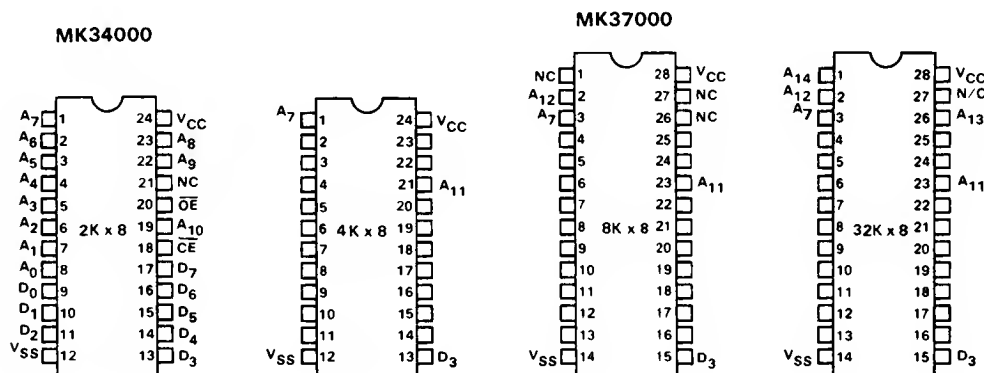
EPROM EVOLUTION

Figure 9

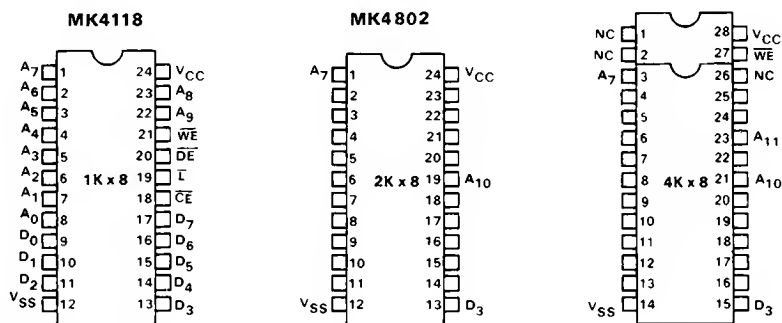


ROM EVOLUTION

Figure 10



STATIC RAM EVOLUTION
 Figure 11



BYTEWYDE FAMILY PINOUTS
 Figure 12

BYTEWYDE™ FAMILY PINOUTS																	
4118	4802	34000	2716	4816	37000	2764					2764	37000	4816	2716	34000	4802	4118
1K x 8 STATIC RAM	2K x 8 STATIC RAM	2K x 8 ROM	2K x 8 EPROM	2K x 8 PSEUDO- STATIC RAM	8K x 8 ROM	8K x 8 EPROM					8K x 8 EPRDM	8K x 8 ROM	2K x 8 PSEUDO- STATIC RAM	2K x 8 EPROM	2K x 8 ROM	2K x 8 STATIC RAM	1K x 8 STATIC RAM
				RFSH	NL	NL					V _{CC}	V _{CC}	V _{CC}				
				NC	A12	A12					NC	NC	WE				
A7	A7	A7	A7	A7	A7	A7	3(1)		28		V _{CC}	V _{CC}	V _{CC}				
A6	A6	A6	A6	A6	A6	A6	4(2)		27		NC	NC	CS	V _{CC}	V _{CC}	V _{CC}	V _{CC}
A5	A5	A5	A5	A5	A5	A5	5(3)				A8	A8	A8	A8	A8	A8	A8
A4	A4	A4	A4	A4	A4	A4	6(4)				A9	A9	A9	A9	A9	A9	A9
A3	A3	A3	A3	A3	A3	A3	7(5)				A11	A11	NC	V _{pp}	NC	WE	WE
A2	A2	A2	A2	A2	A2	A2	8(6)				OE/V _{pp}	OE	OE	OE	OE	OE	OE
A1	A1	A1	A1	A1	A1	A1	9(7)				A10	A10	A10	A10	A10	A10	L
A0	A0	A0	A0	A0	A0	A0	10(8)				CE	CE	CE	CE	CE	CE	CE
D0	D0	D0	D0	D0	D0	D0	11(9)				D7	D7	D7	D7	D7	D7	D7
D1	D1	D1	D1	D1	D1	D1	12(10)				D6	D6	D6	D6	D6	D6	D6
D2	D2	D2	D2	D2	D2	D2	13(11)				D5	D5	D5	D5	D5	D5	D5
V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	14(12)				D4	D4	D4	D4	D4	D4	D4
											D3	D3	D3	D3	D3	D3	D3

With these issues in mind, Figure 9 shows EPROM evolution from 2K to 4K to 8K bytes. Figure 10 shows ROM evolution from 2K to 4K to 8K to 32K bytes. Figure 11 shows static RAM evolution from 1K to 2K to 4K bytes. Figure 12 shows the BYTEWYDE memory presently offered by Mostek.

Presently available 2K x 8 pseudostatic RAMs also fit the compatibility scheme mentioned with the exception of requiring an additional control function to determine refresh time. Pin 1 is presently being used by pseudostatic RAMs as the refresh control. This conflicts with some 8K x 8 EPROM proposals that use Pin 1 for V_{pp}. When V_{pp} is multiplexed with OE, as in the case of the 2732, the problem is alleviated.

A new device on the horizon is called the E²PROM (Electrically Erasable Programmable Read Only Memory). This part, when it is introduced, should produce some exciting and yet perplexing possibilities. As the name suggests, ultra-violet erasure is replaced by electrical erasure. The benefit of such a device would be

in system programming and erasure. This intriguing idea could hold some hidden problems for BYTEWYDE memory standarization in that additional control functions and an in circuit high voltage pin would be required. It would be ideal if technology can solve this problem by the introduction time of these new devices so they could more closely emulate RAMs. Even if the pinout problem of E²PROM is solved, the interface to a microprocessor is likely to remain difficult because of slow write cycle and block erasure.

INTERFACE TO MICROPROCESSORS

The BYTEWYDE memories discussed can be interfaced easily to microprocessors. This fact will be reduced to practice demonstrated by a microprocessor/memory interface using eight socket memory matrix example.

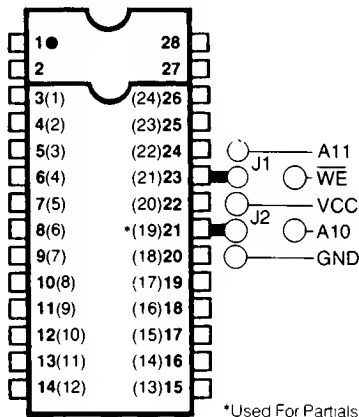
Memory design goals:

- (1) RAM, ROM, EPROM interchange
 - A. Program storage during software debug using RAM

- B. Program storage during prototype production using EPROM
- C. Program storage during production using ROM
- (2) Ratio of RAM/ROM flexible to allow for changing system requirements
- (3) Minimized package count (density and testing consideration)
- (4) Memory expansion capability for after market system enhancements
- (5) Minimum granularity for memory expansion in small increments
- (6) Memory design to stay cost effective for product life 4-6 years
- (7) System throughput not be limited by memory performance
- (8) Multiple sources for RAM, ROM, EPROM
- (9) Initial estimate of memory requirements 4K RAM 4K EPROM (non-volatile program storage)

JUMPER ARRANGEMENT FOR RAM/ROM INTERCHANGE

Figure 13 JUMPER LAYOUT



The first step is to design a memory matrix to accommodate RAM, ROM, and EPROM. Since pinout compatibility exists, eight identical 28 pin sockets will be used. The only special consideration which must be made is a jumper for pins 21 and 23, to allow for RAM/ROM compatibility (see Figure 13). The jumper connection on pin 21 will give the option of connecting pin 21 and A10, ground, or V_{CC} . Pin 21 connections will be jumped to the appropriate signal to defeat the latch function on the 1K RAM, or to allow use of partial 2K devices. The functional half of a partial memory is selected by connecting pin 21 to either V_{CC} or ground. Pin 23 connection will be jumped to the write enable signal (WE) for 1K and 2K RAMs, to A11 for ROMs, EPROMs or RAMs larger than 2K, or +5 for 2K EPROMs. All other control, address, and data lines are bussed together with the exception of the chip enable lines (CE). These connections must be individually routed to the decoder circuitry.

To define the address space of a particular socket site, a 256 x 4 PROM will be used for the CE decode of four sockets. The PROM decoder provides the flexibility of selecting from 1K to 32K bytes of memory at each socket location and can be also used to implement byte addressability for 16 bit microprocessors.

The microprocessor can now be connected directly to the memory matrix (see Figure 14). In this example, a 3880/Z80 microprocessor is used; however, many other microprocessors can be substituted. Figure 15 shows a p.c. layout which meets all the previously stated design goals.

COMPARING BYTEWYDE MEMORY WITH OTHER ALTERNATIVES

Implementing microprocessor memory designs with a coherent packaging strategy enhances density and has other advantages. Most microprocessor based systems require a portion of their memory to be non-volatile, namely ROM or EPROM. Therefore, a large portion of the packaging strategy involves the right combination of RAM, ROM and/or EPROM.

The exact mixture of ROM/EPROM and RAM is rarely known at design time and frequently changes during the course of the product life. As a result, commonly used approaches to building microprocessor memories are restrictive in that ROM/PROM and RAM do not share the same package.

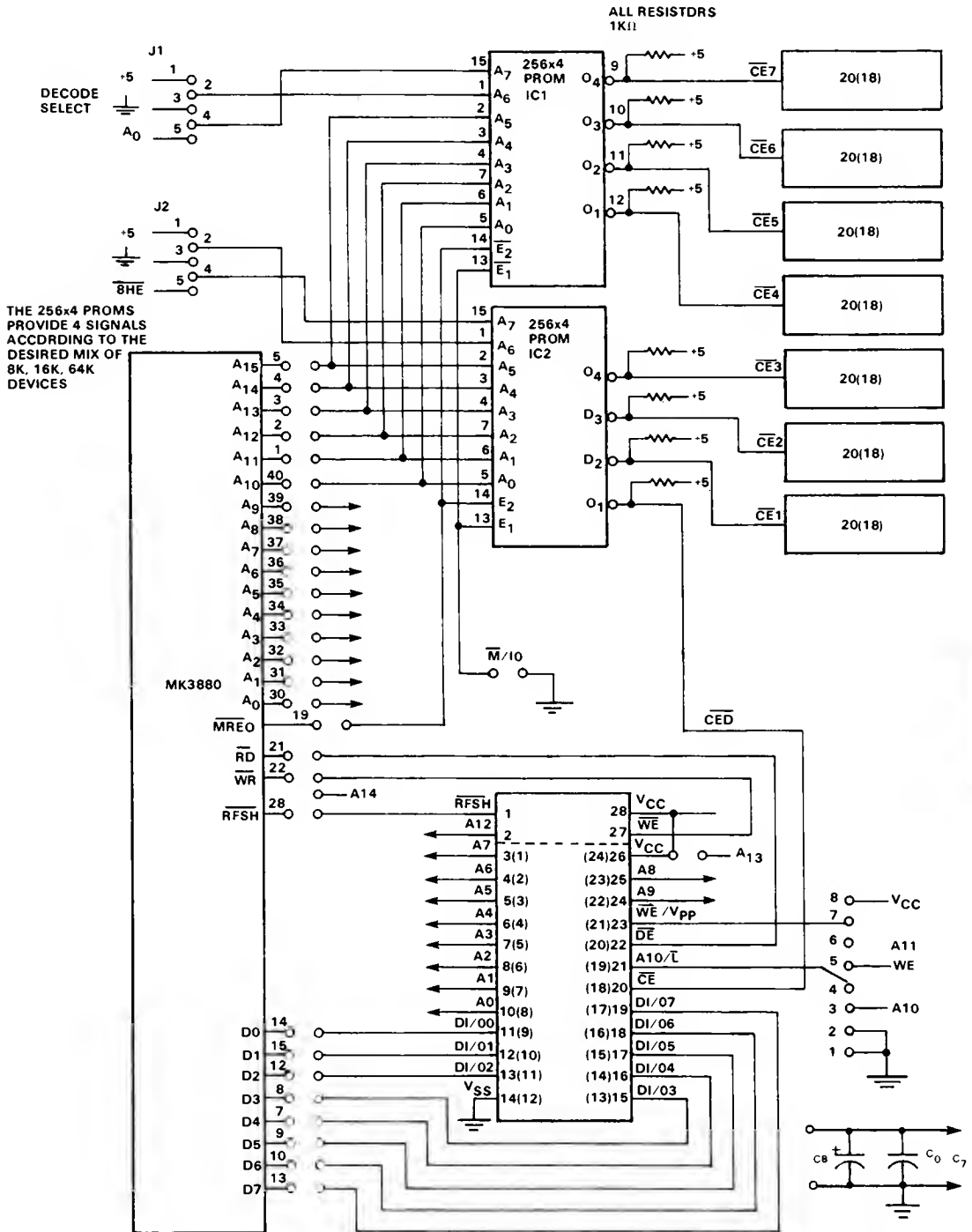
A substantial amount of printed circuit board space is conserved when a single matrix of 28 pin sockets is used, as opposed to the two matrices of ROM/PROM and RAM each having their own space requirements for expansion. BYTEWYDE pin compatible memory devices of RAM, ROM and EPROM make possible high density memory, yet allow for flexibility and future expansion by using a single matrix of 28 pin sockets.

With single matrix fewer constraints are placed on the memory configuration, since RAM and ROM/PROM are mixed at will. Expansion can be accomplished by using the next generation components which will be pin compatible with presently available BYTEWYDE memory.

A comparative analysis of current technology alternatives for implementing 4K x 8 RAM plus 8K x 8 EPROM memory has been performed (see Figure 16, Matrix A, B and C and Comparative Analysis Table, Figure 17). The printed circuit board density has been determined, using two sided printed circuit board with .05 inch layout rules. The advantages and disadvantages of each approach are summarized in a table.

INTERFACE TO AN MK3880

Figure 14



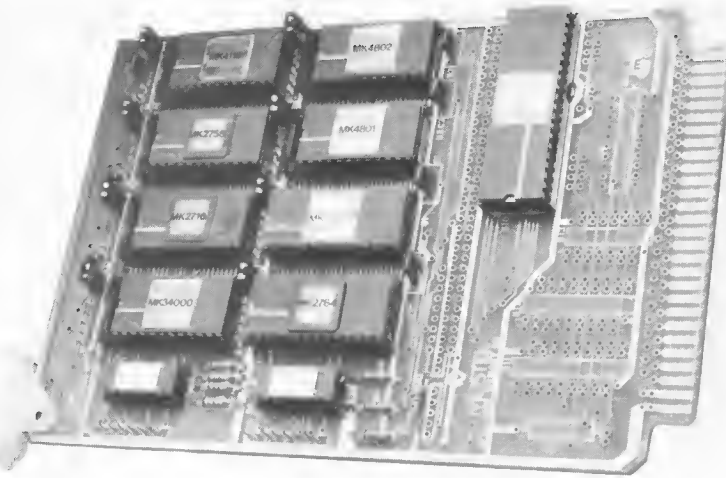
CONCLUSION

RAM, ROM, EPROM interchange, consistent control functions, a coherent packaging philosophy, future density upgradeability without redesign, and memory expansion by addition of a single device make BYTEWYDE memory a natural selection for new microprocessor memory design. The standardization of BYTEWYDE memory can eliminate many problems imposed by ever changing software and heretofore rigid memory configurations. BYTEWYDE is a concept for the future which makes sense today. Alternative approaches have shortcomings which cause them to be less cost effective. Dynamic RAMs with x1 organizations

are meaningful for large memory but inappropriate as a building block for smaller microprocessor memory. Static RAM like the 2114 1K x 4 require higher package count, offer no upgrade potential, and lack compatibility with ROM/EPROM. The printed circuit board density achievable using BYTEWYDE memory is equivalent to the alternative approaches today and will be superior in the future without redesign. Memory cost is minimized by the increased engineering return on investment and economics to scale associated with prolonged usage of the same design.

PHOTOGRAPH

Figure 15A



PRINTED BOARD LAYOUT (SOLDER SIDE)

Figure 15B

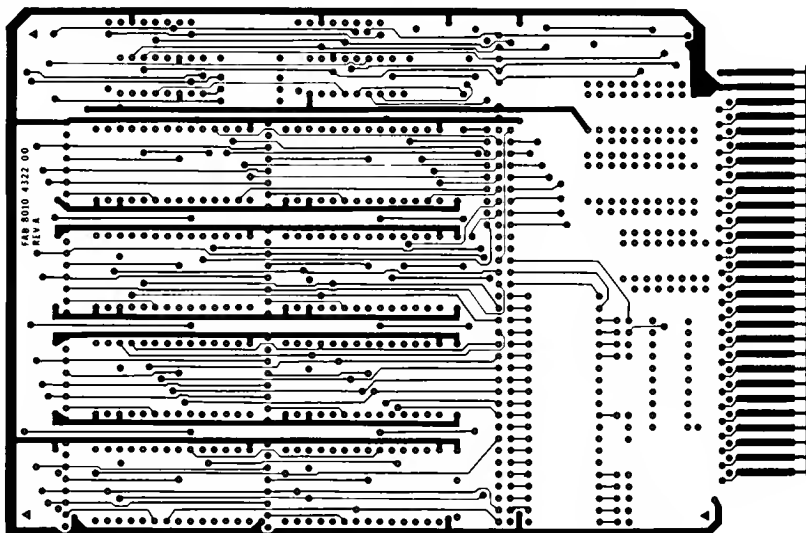
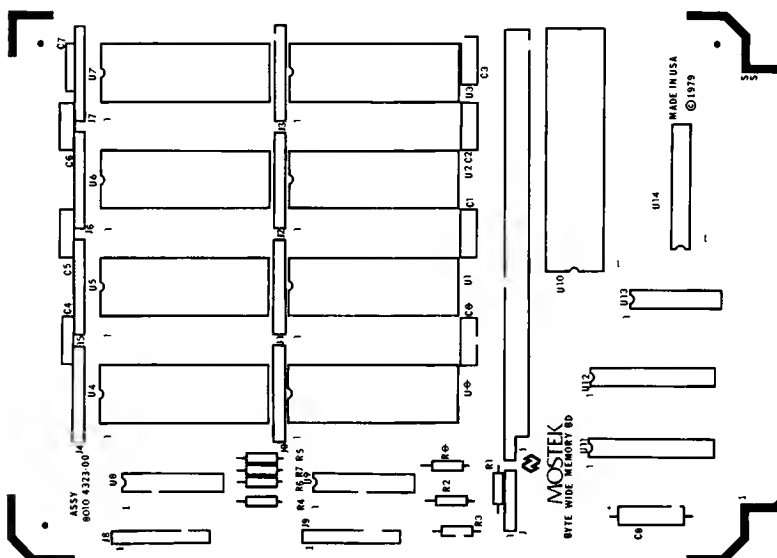
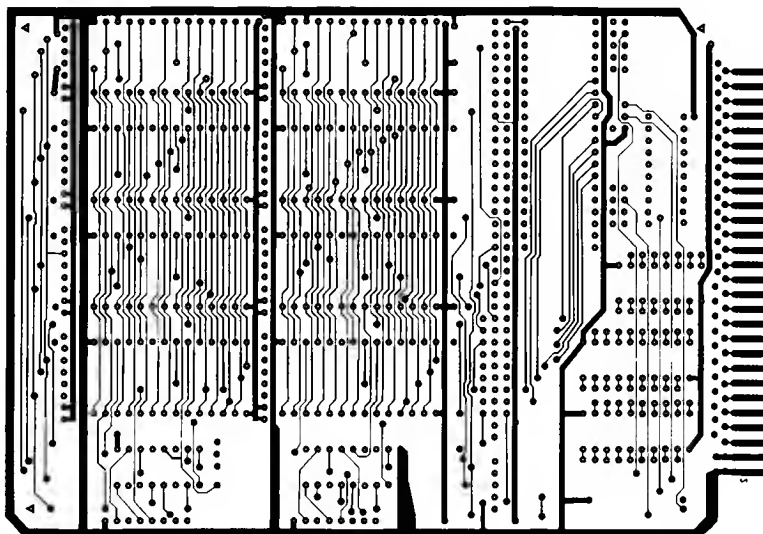


Figure 15C



DESIGN MEMORY BOARDS FOR RAM/ROM/EPROM INTERCHANGE

Application Note

Microcomputer-system designers can realize great benefits if their equipment has the flexibility of using mixtures of RAM, ROM and EPROM. For one thing, this capability allows them to take advantage of price differentials between memory-IC types; for another, it allows them to efficiently exploit these chips' different volatility characteristics.

This section details a method to achieve the desired flexibility: The technique it presents permits a single pc-board design to use multiple types of memory ICs. Furthermore, the method will work not only with today's devices, but with tomorrow's parts as well. Thus, you can use it to build systems that can readily be improved as technology advances.

AIM FOR SOCKET COMPATIBILITY

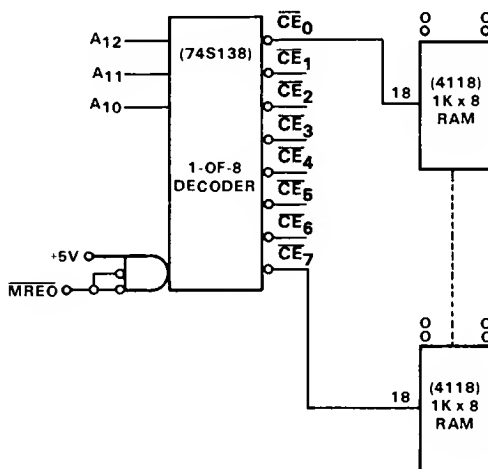
At any time, the density of available single-chip ROM is as much as four times that of EPROM, while EPROM is as much as twice as dense as RAM. Because this approximate density relationship is expected to continue, a particular μ -C system design, if it is to have a long product life, must accommodate blocks of memory in as much as a 16:1 ratio. This requirement in turn

dictates the need for a flexible address-space decoder: To accept devices that have an address space ranging from 1K to 8K, for example, a memory-IC socket must have a decoding mechanism that can accommodate such address-space differences.

A technique of programmable address-space management can meet this requirement. For memories of equal address space (same capacity), a simple 1-of-8 decoder such as the 74S138 works well (Figure 1). If you can limit memory usage to two different capacities, a 1-of-8 decoder, a quad AND gate and jumper wires (or a DIP switch) suffice (Figure 2). However, to support a wide range of memory capacities, a programmable bipolar ROM used as an address-space decoder provides the most flexible solution (Figure 3).

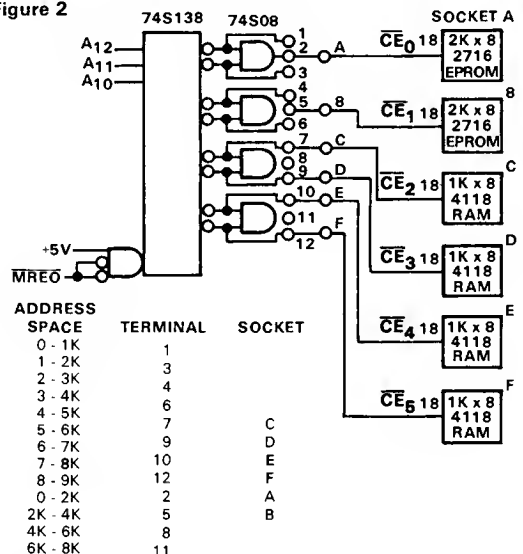
The most popular wide-word memory package today is the 24-pin DIP: It's used for the 4118 (1K x 8) RAM, the 2716 (2K x 8) EPROM, the 36000 (8K x 8) ROM, etc. But, although this 24-pin package serves today's devices, it can't support future higher capacity memory chips. The logical extension? A longer 28-pin package with the same center-to-center spacing and width. By using such a package and then carefully selecting their pinout

Figure 1



Address decoding for memories of identical capacity requires only a simple 1-of-8 decoder. A fixed 1K - word socket address space is shown.

Figure 2



A satisfactory address-decoding solution for memories with two different capacities employs a decoder, an AND gate and appropriate jumpers or switches. This technique handles 1K-or-2K-word devices equally well.

configurations, IC makers can obtain a high degree of compatibility between 24- and 28-pin memories—whether RAM, ROM or EPROM.

Fortunately for designers, such a trend is now very much in evidence. One example of such a 28-pin memory is Mostek's 4816 (2K x 8) RAM, soon to be joined by the 37000 (8K x 8) ROM and the 2764 (8K x 8) EPROM.

Note, however, that although the pinouts of various types of wide-word memories are similar, they are not exactly identical: Certain functions do not exist for all members of a manufacturer's family (WRITE ENABLE exists for the 4118 RAM, for example, but not for the 2716 EPROM). Additionally, multiple power supplies greatly complicate pinouts, so device compatibility is limited to parts that operate from +5V only.

Figure 4 takes all of these factors into account. It shows

a layout of a 28-pin socket that maximizes the degree of device interchangeability among present and contemplated parts. Memory ICs with 24 pins plug into pins 3 through 26.

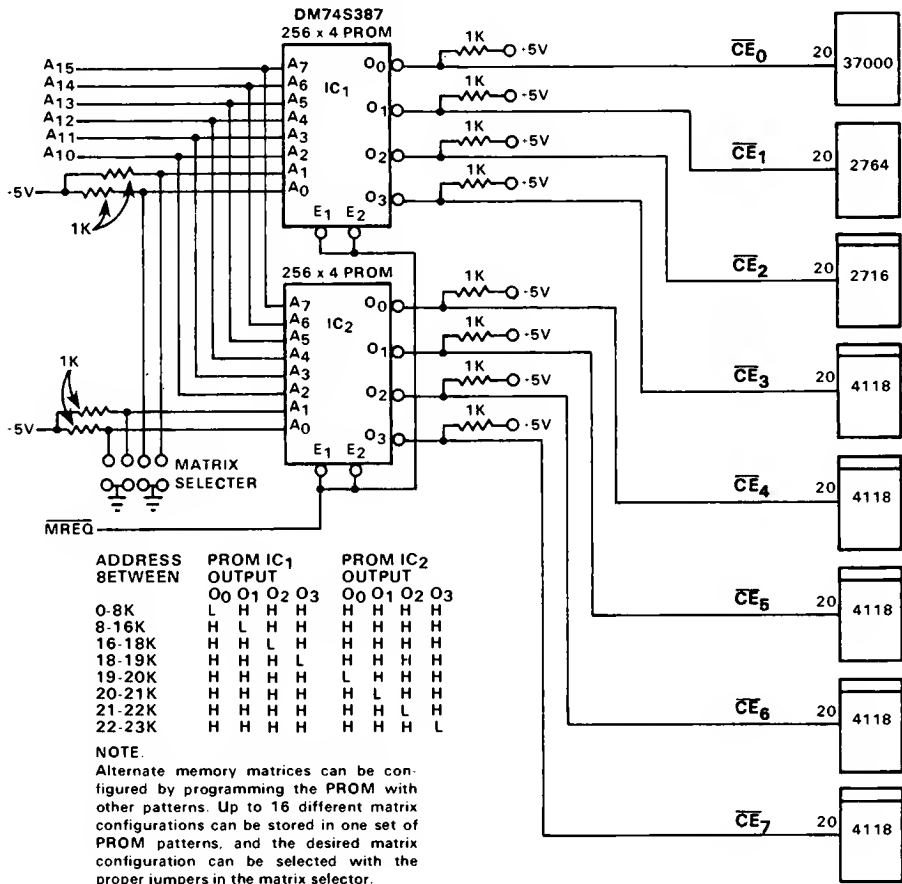
To put this pc-board design into perspective, consider Figure 5, which shows a 3880 μ P interfaced to eight 28-pin memory sockets. By placing the proper pattern in the system's address-space PROM and selecting the appropriate jumpers, you can fill the memory sockets with any combination of today's (or tomorrow's) compatible RAM, ROM and EPROM devices.

INTERCHANGEABILITY PRODUCES MULTIPLE BENEFITS

The cost of any IC reflects its manufacturability and the volume in which it's produced.

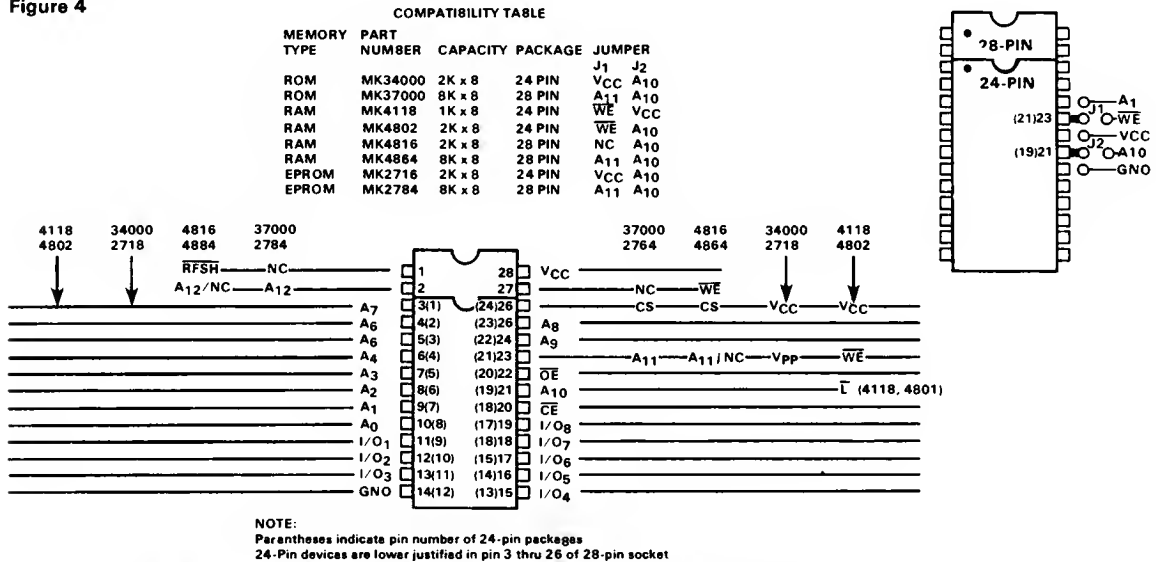
Taking the latter factor first, increasing the volume of a

Figure 3



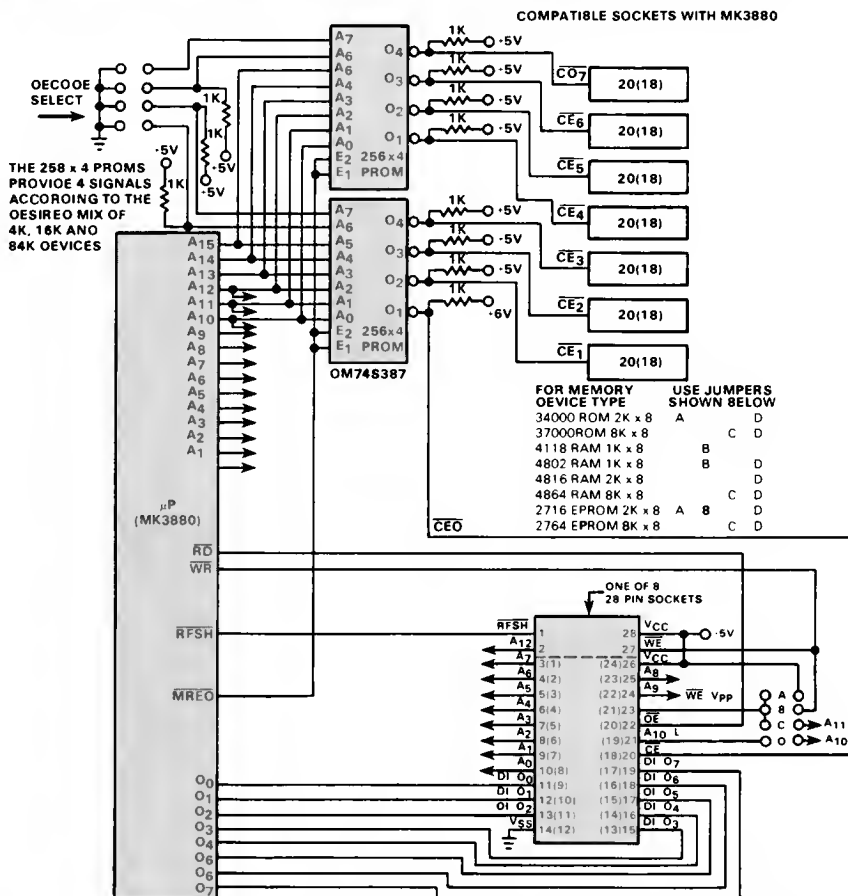
Programmable socket address space results from programming the PROM with a pattern corresponding to the desired socket address space. In this example, whenever an address between 0 and 8K is presented to IC₁, its O₀ output is LOW, and all others are HIGH.

Figure 4



Key to the interchangeability concept is the use of a 28-pin socket to handle both 24- and 28-pin memory devices.

Figure 5



This μP -based system accommodates a wide variety of RAM, ROM and EPROM combinations through variations in the address-space PROM pattern and the jumper connections.

part substantially reduces its manufacturing cost. Thus, standard devices with widespread usage generally offer long-term price advantages. And because socket compatibility enhances a memory device's chances of achieving high-volume sales, it should provide users with substantial cost savings, while also increasing the likelihood of viable second sources.

Manufacturability of an IC relates to its die size and the number of steps in its manufacturing process. For a given defect density, the yield of good parts is geometrically proportional to size; ie, the smaller the chip, the greater its yield and the lower its cost. And of course, the fewer mask steps used to make the device, the lower the chip cost.

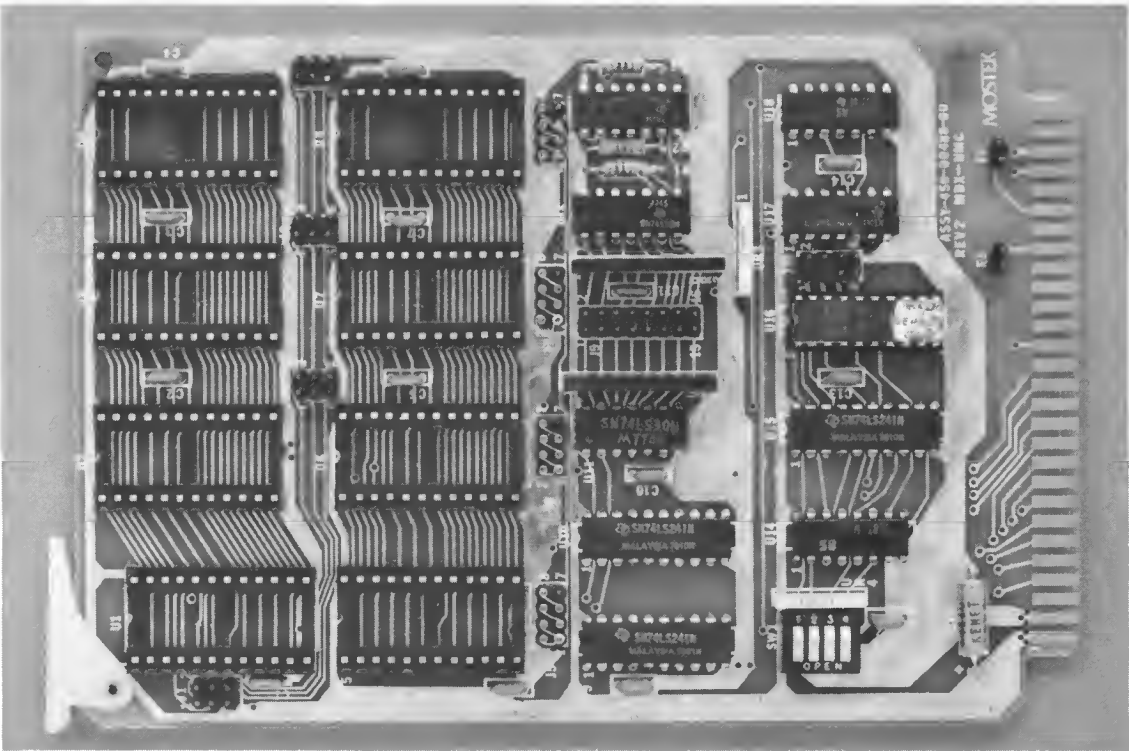
The accompanying table provides an understanding of the relative magnitudes of these factors.

	ROM (36000)	RAM (4118)	EPROM (2716)
Cell Size (mil ²)	0.25	2.02	0.65
Number of Masks	8	11	13
Capacity (bits)	8K x 8	1K x 8	2K x 8

ONE BOARD DOES IT ALL

The viability and benefits of pin-compatible memory components are demonstrated by Mostek's Model MDX-UMC, a pc board that can handle 4118 (1K x 8) or 4802 (2K x 8) static RAMs, 2758 (1K x 8) or 2716 (2K x 8) EPROMs and the 34000 (2K x 8) ROM. This capability permits a total of 16 different memory configurations using 4K boundary addressing. Thus, MDX-UMC-based memories could include 4K x 8, 8K x 8 or 16K x 8 static-RAM boards; 4K x 8 or 8K x 8 ROM boards; or 8K x 8 EPROM boards.

MDX-UMC BOARD



RESOLVING MICROPROCESSOR MEMORY BUS CONTENTION

Application Note

INTRODUCTION

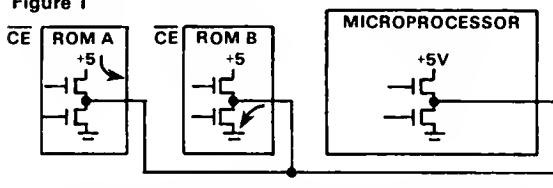
A microprocessor system will be plagued by reliability problems if attention is not given to timing parameters. One type of timing related problem often overlooked is memory bus contention. The symptoms range from catastrophic damage to soft errors which do not lend themselves to straight forward troubleshooting techniques. When bus contention occurs, large current transients are generated. The transients are 8 or 16 times the short circuit of single output due to the number of lines of the bus. This can disturb adjacent circuits or cause power supply fluctuations sufficient to destroy memory data integrity. The cause effect relationship of soft errors can be insidious and remain undetected until designs are into production.

RESOLVING MICROPROCESSOR MEMORY BUS CONTENTION

A good approach to microprocessor memory design is to provide two control functions so that memory system performance will not be compromised for lack of output buffer control. Memory busses are commonly constructed with three levels of complexity. In the simplest case the bus had unidirectional data flow. A more

OUTPUT BUFFER CONFIGURATIONS (SHARED DATA BUS)

Figure 1



complex bidirectional data bus allows data to flow into and out of the memory on the same lines but at different times thus conserving package pins, printed circuit board track, and connectors. To further conserve lines, addresses are sometimes multiplexed with a bidirectional data bus. In any of these cases the system designer must be able to guarantee that for any point in time the bus be defined for data in, data out, or address. In this way bus contention is eliminated.

Bus contention occurs when two or more output buffers on the same line are enabled. In Figure 1 ROM A and ROM B are said to be in bus contention because "A" is sourcing current (1) and "B" is sinking current (0) at the

same point in time. For proper system operation ROM A must go to a high impedance state prior to ROM B output turning on. This break before make characteristic is essential for all multi output bus schemes. Short periods of bus contention normally cause no catastrophic damage but do generate large amounts of system noise. This noise can cause an obscure system malfunction which does not lend to straight forward troubleshooting procedures. For reliable system operation bus contention must be avoided. The timing diagram (Figure 2) shows ROM A and ROM B implemented with output buffers controlled solely by \overline{CE} (chip enable). In this case the output buffer enable time must be longer than the disable time to insure a contention free bus. The second data bus wave form shows the contention problem when \overline{CE} enable "B" time is less than \overline{CE} disable "A" time.

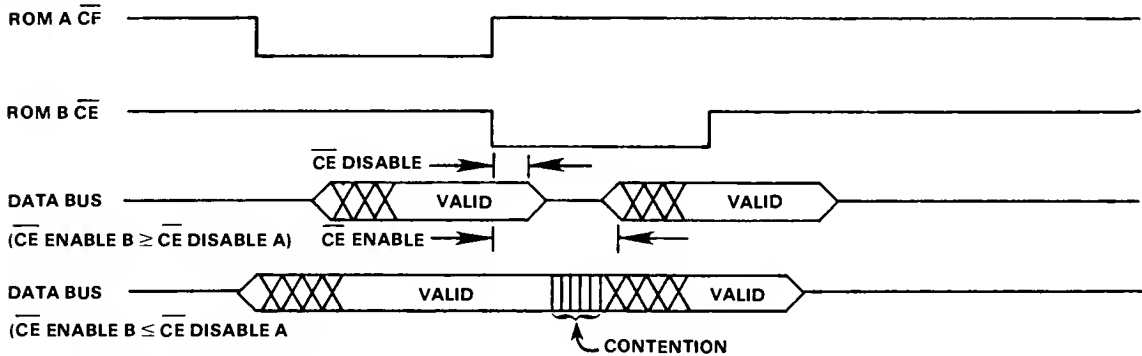
If a fast \overline{OE} (output enable) control is provided in addition to the \overline{CE} control no constraints are placed on \overline{CE} for bus contention. In this way \overline{CE} is reserved for device selection and \overline{OE} for buffer control. When a device is given a \overline{CE} , it is singled out in a matrix as the device to go into cycle. The selected device then powers up for the cycle. After the device is selected, at a time when bus contention is not a problem, \overline{OE} can be used to gate data on and off the bus. This freedom to control the bus with the \overline{OE} allows the next cycle to be initiated with \overline{CE} prior to the bus being released from the previous cycle thus enhancing performance or widening operating margin.

A bidirectional data bus configuration generates the possibility of another form of bus contention when a write cycle is followed by a read. Typically the data in for a write must be held valid until the completion of the write cycle. During this write time data is flowing into the memory and is being driven by the output of the microprocessor. A read cycle immediately following will force the data bus to switch from data in to data out. If the read device output is solely controlled by \overline{CE} the potential exists for the buffer to turn on before the data in (write data) from the microprocessor goes high impedance. The addition of an \overline{OE} control function would allow the selection and initialization of the read to occur without delay by using \overline{OE} to gate the read data on the bus after the write data is clear. Figure 3 shows what happens with and without the additional \overline{OE} control.

An even more restrictive condition exists when the data

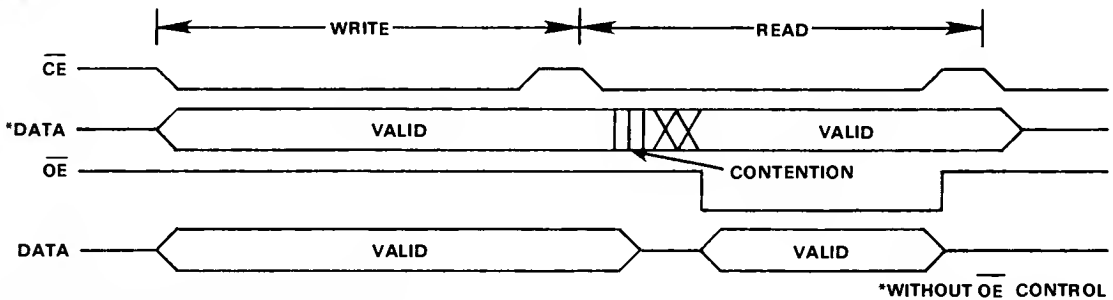
READ-READ BUS CONTENTION

Figure 2



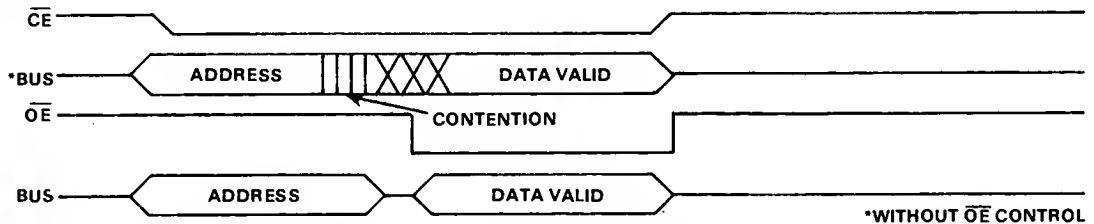
WRITE-READ BUS CONTENTION

Figure 3



ADDRESS-DATA BUS CONTENTION

Figure 4



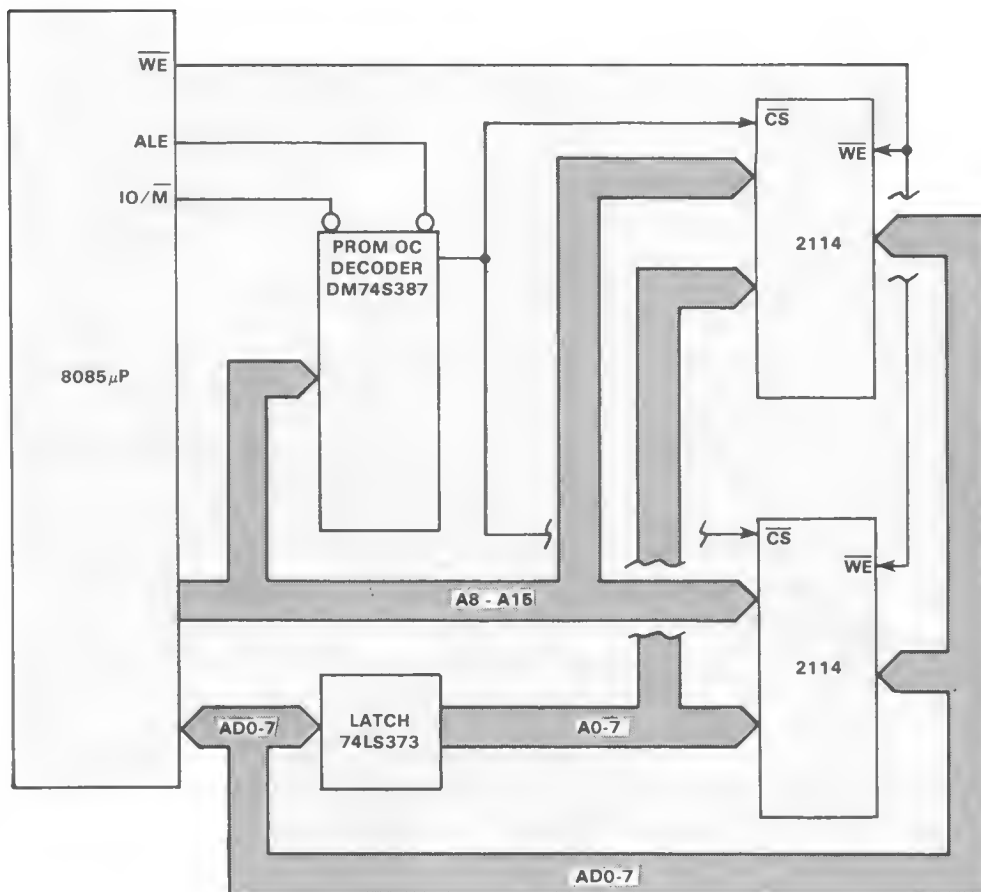
bus is bidirectional and address is multiplexed as in the 8085 or 8086 microprocessor. In this case the read cycle first has address on the bus followed by data. With a sole \overline{CE} control a fast memory could cause bus contention by sourcing or sinking output current before the bus achieved a high impedance condition from the address state. This contention problem can be resolved without performance degradation by the addition of an \overline{OE} as seen in Figure 4.

Address/data bus contention can be further illustrated in an example involving a popular microprocessor and memory configuration as in Figure 5. An 8085 microprocessor with time multiplexed address/data is shown using a PROM for memory device selection and a latch device for separating the lower 8 addresses from the data bus. The memory is comprised of a matrix of 2114-3 1K x 4 bit static RAMs which access in 300ns.

The PROM decoder is inhibited by the \overline{M}/IO and ALE signals until address decode is established and will generate a clean chip enable signal (\overline{CS}) for the selected memory device within 30ns from the trailing edge of ALE. The address will arrive at the 2114 memory delayed 15ns due to the propagation delay of the latch. (See timing diagram Figure 6) once \overline{CS} arrives at the appropriate memory device, \overline{CS} to data active time begins to occur and the output can become active in as little as 20ns. As a result, 50ns (30 + 20) after the trailing edge of ALE the output buffers will go active (low impedance) onto the address/data bus. However, the address hold time from the 8085 is 100ns minimum from ALE which puts the bus in contention for some 50ns.

This contention problem can be resolved with some added logic for delaying the \overline{CS} signal. However, for

Figure 5



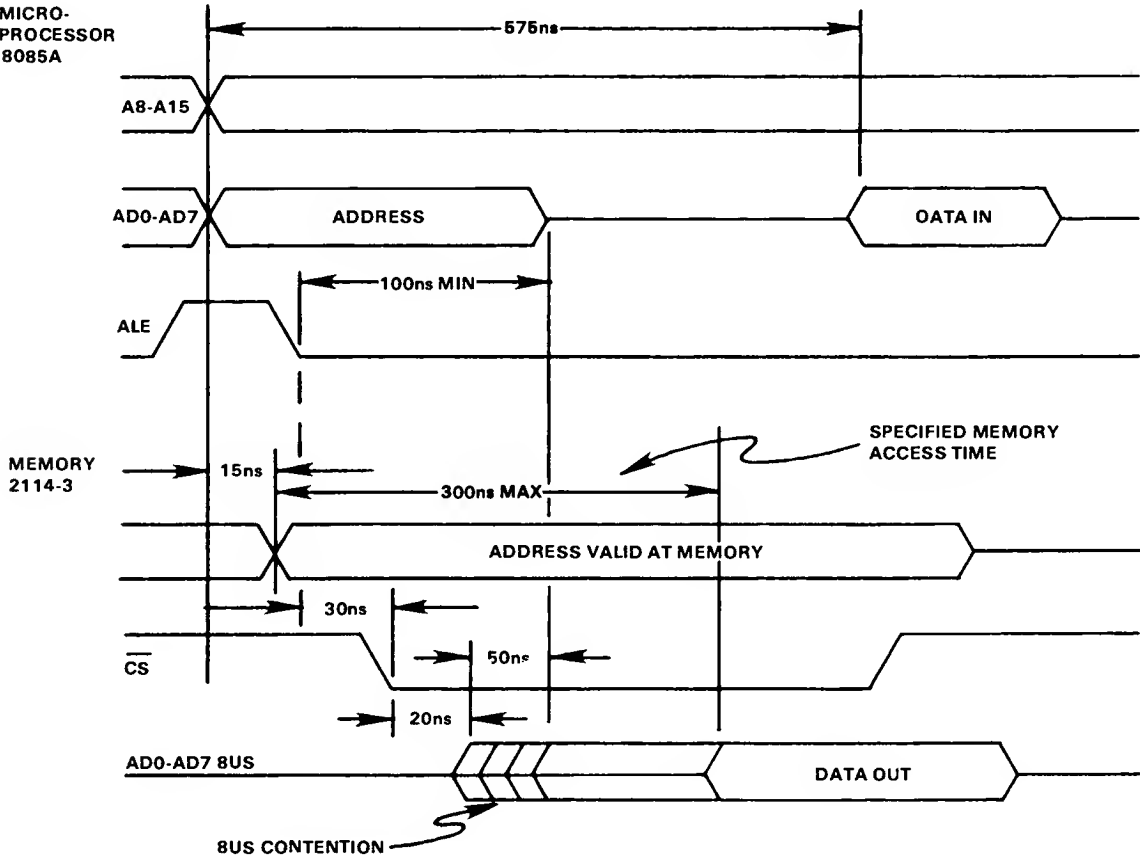
some applications this could degrade access which would require the selection of a higher performance device. The circuit board would also suffer the loss of potentially valuable real estate to the extra logic devices.

A better solution is to use a memory device which has an output enable function (\overline{OE}). Figure 7 shows the 8085 memory interface with the MK4118 substituted for the 2114's. The chip enable (\overline{CE}) and address signals are handled exactly as before. The difference is that read (\overline{RD}) signal is connected directly to memory for

control of the output buffers. The timing diagram (Figure 8) illustrates how the \overline{OE} control function holds the memory output inactive for 130ns minimum until being activated by the microprocessor. The \overline{OE} access time is fast enough so that no loss is suffered in performance.

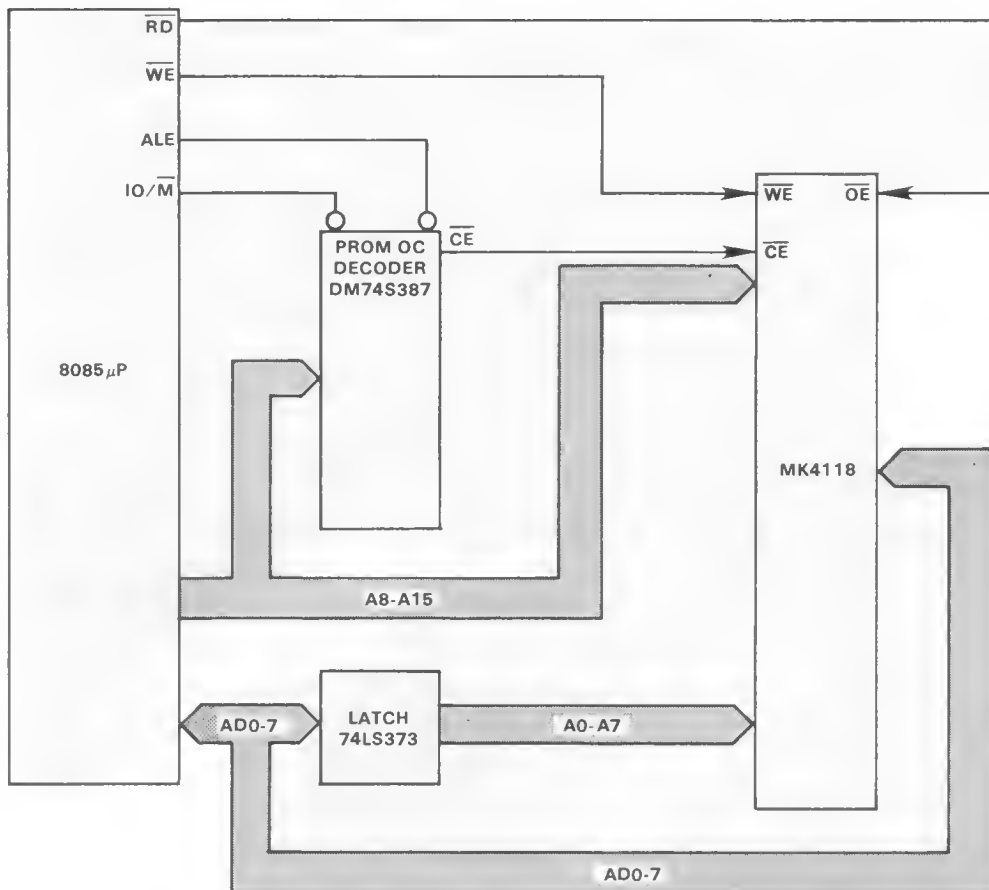
In short, the addition of the \overline{OE} control function on memories provides the designer with a powerful tool to resolve bus contention problems. Memories without two control function often result in more restrictive performance or external bus control elements.

Figure 6



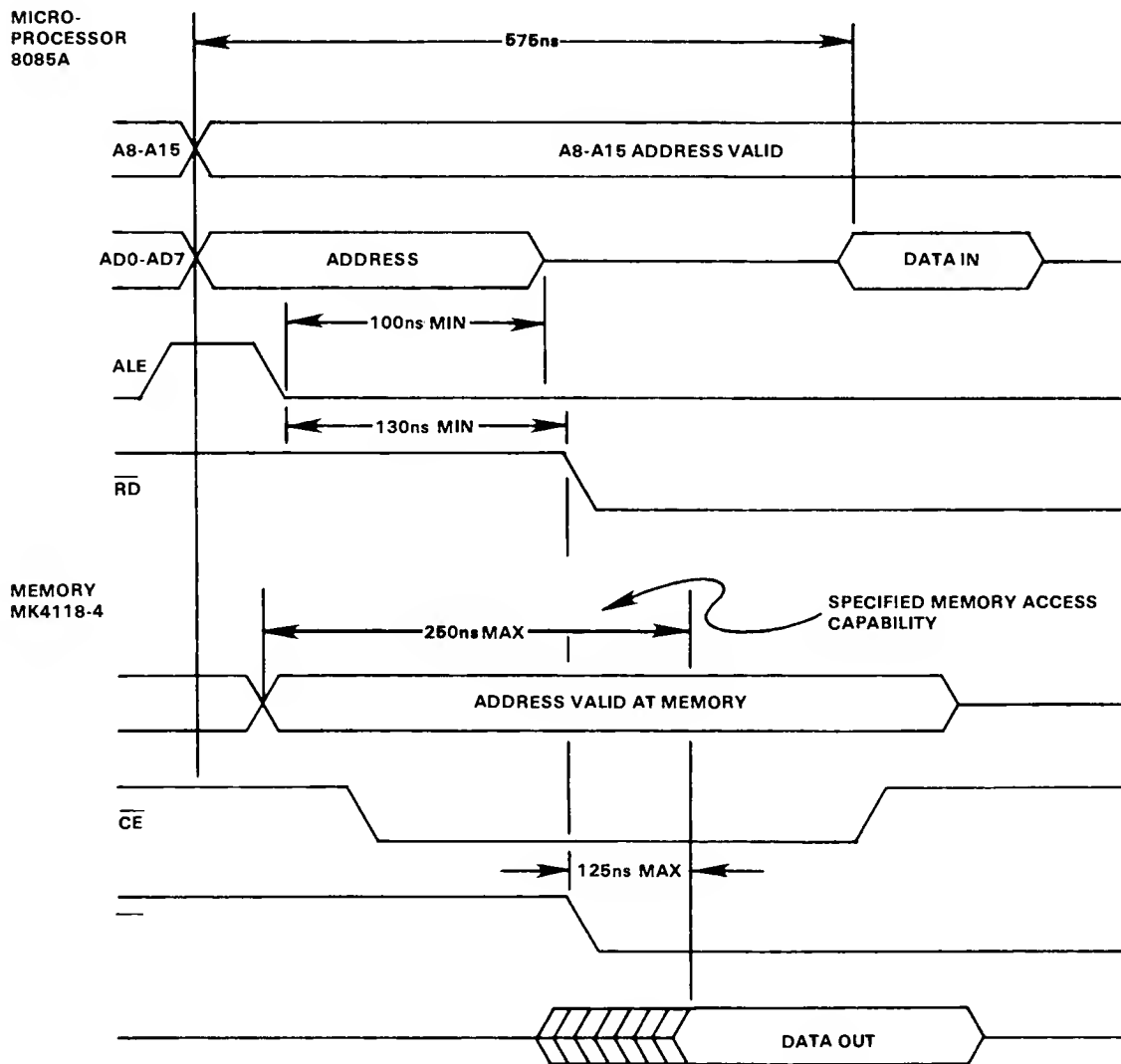
The memory's data out buffers can become active 20ns after \overline{CS} is low, the address can still be on the bus for 50ns after the memory output buffers are active.

Figure 7



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Figure 8



No bus contention exist because the output buffers are held inactive by \overline{RD} (\overline{OE}) control until well after the address has cleared the bus.

INTRODUCTION

The development of the solid state memory has proven to be one of the most important elements in the evolution of the computer. The fact that semiconductor memories can be manufactured at low cost and in high volume has made the cost of computing less expensive at all levels. Low cost memory has reduced the cost of mainframes and mini-computers and low cost memory devices have been the keystone in the development of microcomputers.

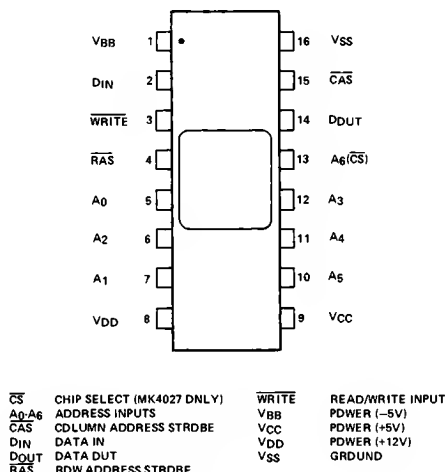
Although bipolar devices play an important role, most of the current development in semiconductor memories is concentrated on N-channel Metal Oxide Semiconductors (N-MOS). The flexibility of N-MOS has made possible several types of memory devices each with its own niche of applications. The three basic types of N-MOS memory are dynamic RAMs, static RAMs, and ROMs.

DYNAMIC RAMS

Dynamic Random Access Memories are considered the real workhorses of the memory industry. Because of their high density, low power consumption, and low cost, Dynamic RAMs have become the first choice for mainframe memory and for memory intensive minicomputers and microcomputers. Dynamic RAMs began to replace core and memory with the introduction of the 1Kx1 1103, however, the general acceptance of Dynamic RAMs really came about with the introduction of the 4Kx1 devices in 1973. Most of the early 4K Dynamic RAMs were 22 pin devices but 18 pin devices were also available. Then in 1974 MOSTEK introduced the 16 pin 4K Dynamic RAM with multiplexed addresses. The 16 pin device gained a great deal of acceptance and has become the industry standard because the board packing density with 16 pin devices was about twice that of the 22 pin devices. Another factor that accelerated the acceptance of the multiplexed Dynamic RAMs was that the 16 pin multiplexed configuration could be easily modified to accommodate a 16Kx1 Dynamic RAM. Presently MOSTEK and others offer a 4Kx1 (MK 4027) and a 16Kx1 (MK4116) that are functionally identical making it possible for a memory system designer to design a board that can accommodate either part. This allows an easy upgrade of 4K based systems to 16K based systems with no extra investment in design.

PIN CONNECTIONS MK4027 & MK4116

Figure 1

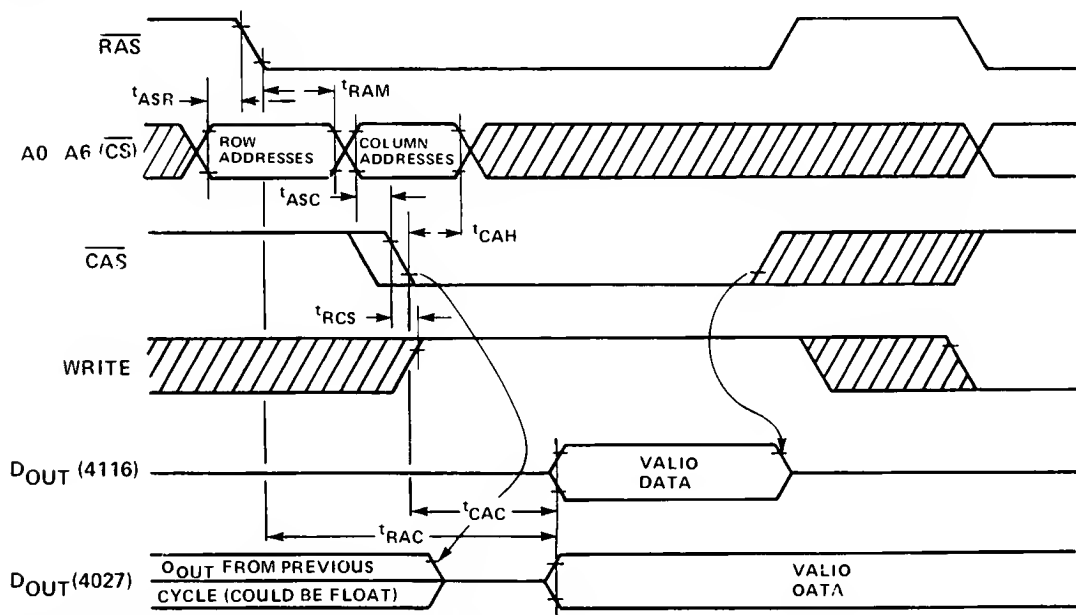


DEVICE DESCRIPTION

Before delving into some of the system aspects and applications of 4K and 16K multiplexed Dynamic RAMs, it is necessary to discuss the fundamental operation of the device. The MOSTEK MK4027 and MK4116 will serve as the models for the discussion. (Refer to the pin configuration in Fig. 1). As stated earlier, the basic operation of the MK4116 is very similar to that of the MK4027. The data storage within the memory is a matrix format with an equal number of rows and columns. The row address is applied to the address inputs and are strobed (latched) into the chip when RAS (Row Address Strobe) is applied. The Column Addresses are then applied and CAS (Column Address Strobe) is asserted causing them to also be latched. For the MK4027 there are 6 address lines to address, 64 rows and 64 columns giving $64 \times 64 = 4096$ bits. An additional pin (CS) is used for chip selection. For the MK4116 the CS input is replaced by a seventh address input giving 128 rows and 128 columns for $128 \times 128 = 16384$ bits. The Chip Select input that is present with the MK4027 is replaced with the additional address input required for the 16K RAM. With the MK4027 the output is controlled by the negative going transition of CAS. (See Figures 2 & 3). Once the output is set it cannot change until the part receives the next CAS. Without a Chip Select signal, the only

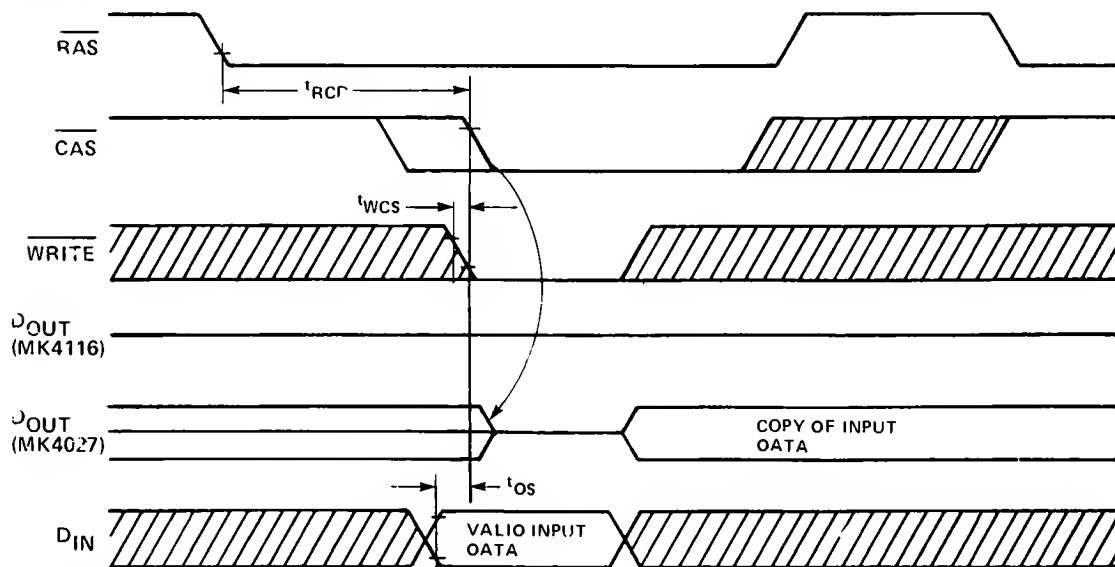
READ CYCLE TIMING FOR MK4116 & MK4027

Figure 2



WRITE CYCLE TIMING FOR MK4116 & MK4027

Figure 3



DEVICE DESCRIPTIONS (Cont'd)

possible method of chip selection on the 16K RAM would be decoding the Row Address Strobe. The Column Address Strobe ($\overline{\text{CAS}}$) must activate every memory cycle to turn off the latched outputs of unselected RAMs. In giving up the Chip Select a very important system feature also disappears - the option

(or function) of two dimensional decode within a memory matrix. Therefore, instead of the conventional latch output that is incorporated in the existing 4K RAMs, the MK4116 requires a slightly modified output stage to allow more system flexibility. The Data Out of the MK4116 becomes valid within the specified access time and will remain valid until the Column Address Strobe ($\overline{\text{CAS}}$) is taken to the inactive

DEVICE DESCRIPTIONS (Cont'd)

state. However, in early write cycles ($\overline{\text{WRITE}}$ active low before $\overline{\text{CAS}}$ goes low) the data output will remain in the high impedance (open circuit) state throughout the entire cycle. The purpose of the new approach of controlling the data output is to allow the 16K RAM to be the "universal memory" for all types of system requirements. The flexibility of this circuit will become apparent as we explore a wide spectrum of data processing applications.

THE DYNAMIC RAM IN MICROPROCESSOR SYSTEMS

The amount of read/write memory associated with microprocessor based system is ever increasing. Microcomputer applications range from computerized games to commercial transaction processing machines. Random Access Memory associated with these applications should be flexible in operation, tolerant of power supply noise, reliable, simple to interface, and offer the highest possible system bit density. The Dynamic RAMs definitely have a home with these types of products.

A block diagram for a typical 16 pin Dynamic RAM memory system is illustrated in Figure 4. The

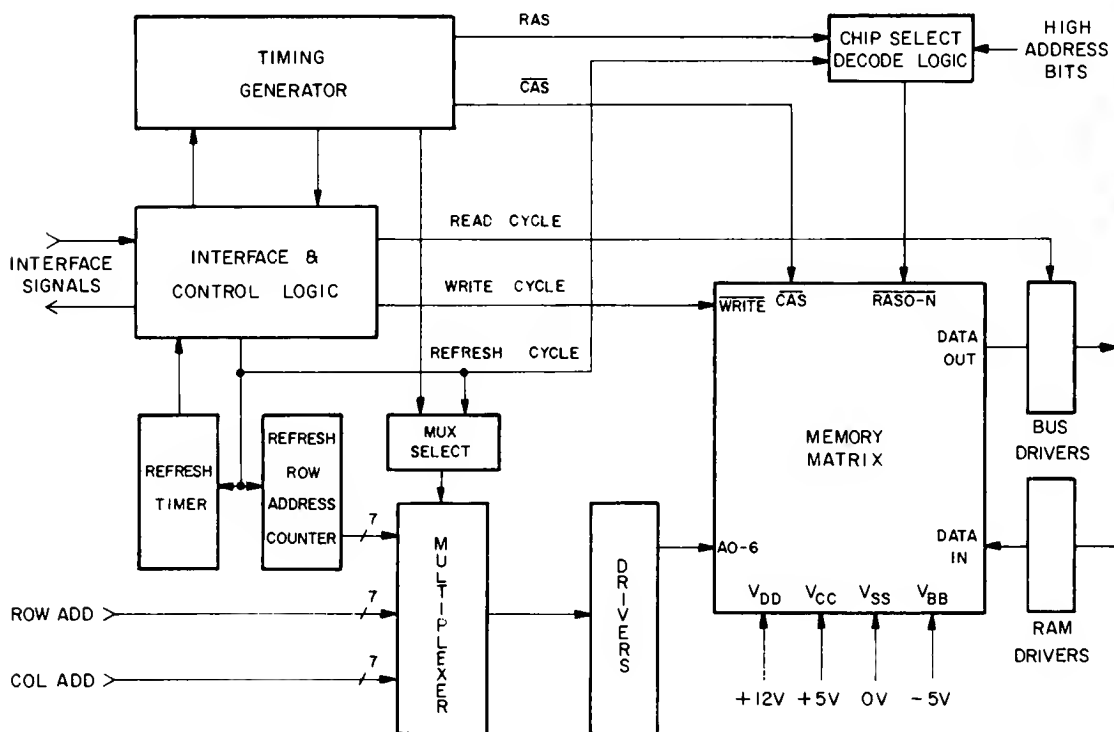
common elements of this system - which include interface logic, timing generator, decode logic, multiplex circuitry, refresh logic, and buffers - can be implemented using approximately 12-20 standard TTL devices. A full 64K by 8 bit system, which is the maximum amount of addressable memory for most common microprocessors, can be constructed on a single (Double-sided) Printed Circuit Board in an area less than 50 square inches.

The functions of most microprocessor based memory systems are reasonably simple and straight forward when compared to some mini-computers and large mainframes. Microprocessor memory modules are usually synchronous and initiate processor requested read or write cycles upon command. Refresh of Dynamic RAMs in a microprocessor based system is easily handled during the portion of an instruction cycle that does not require a memory access.

Since most microprocessor systems do not require specialized memory operations such as read-modify-write cycles, timing considerations for the Dynamic RAMs can be kept very simple. Therefore, interface convenience and device tolerance are more important than device operating modes. By not having an output latch on the 16K RAM, a very important microprocessor interface concept - the common I/O data

BLOCK DIAGRAM

Figure 4



THE DYNAMIC RAM IN MICROPROCESSOR SYSTEMS (Cont'd)

bus - can be realized. For interface convenience, the data input pin of the 16K RAM can be directly connected to the data output pin on the PC board. If common I/O operation is desired for the 16K RAM, then all write operations should be executed in the early write mode (WRITE active low before CAS goes low).

Two typical examples of the logic required for a microprocessor interface can be seen in Figure 5 and Figure 6. Figure 5 shows a minimum RAM system for the Z80 microprocessor. The RAM system consists of either 8 MK4027's giving 4K bytes of RAM or 8 MK4116's giving 16K bytes of RAM. This is the type of interface that would be found in small microprocessor systems where the RAM is located on the same board as the microprocessor. Figure 6 shows a larger memory organization where the memory is on a separate board.

In both examples it can be seen that Dynamic RAMs interface very easily to microprocessor busses mainly

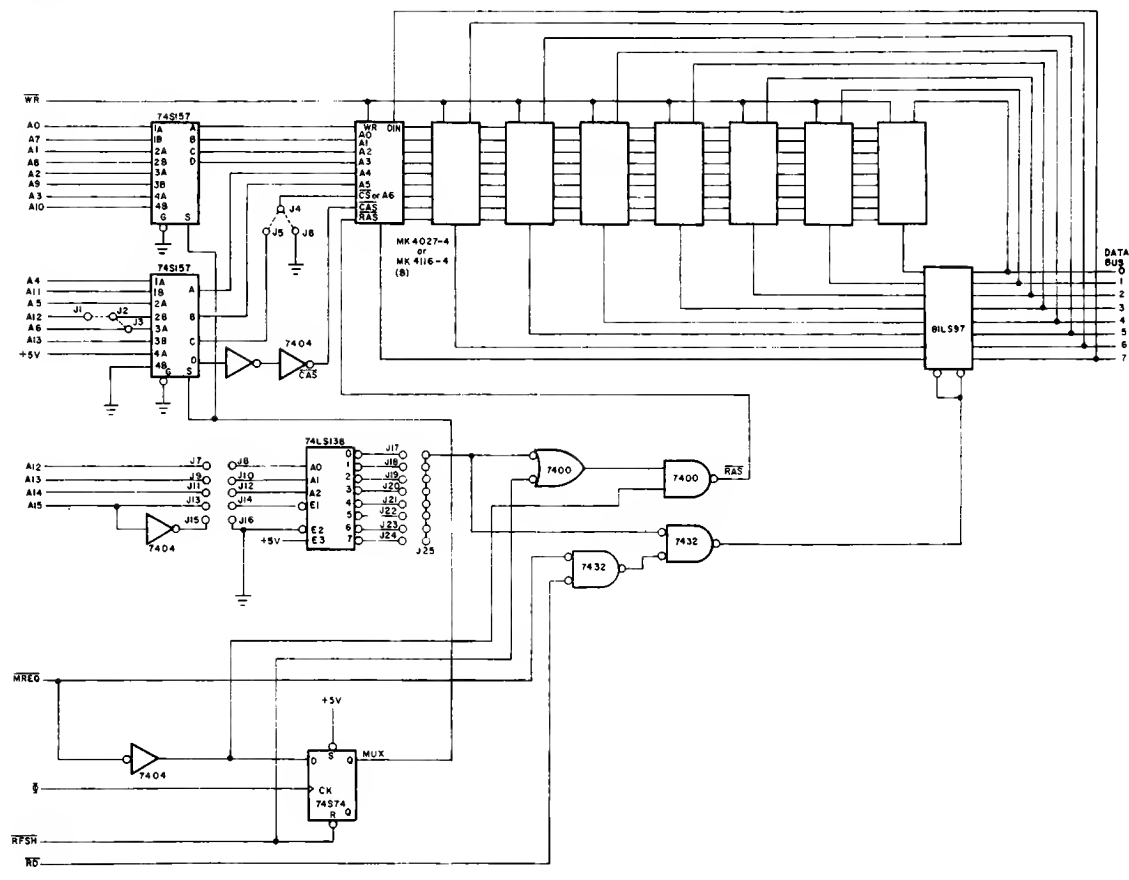
because of the synchronous nature of microprocessor systems. This makes it easy to accommodate the multiplex and refresh timing of the RAMs.

MINICOMPUTER/MAINFRAME APPLICATIONS

A logical progression beyond the simple microprocessor systems are the minicomputer applications and then mainframe computers. Here, concepts like multiway interleaved memory, Direct Memory Access (DMA), multiport memory and asynchronous bus techniques become a very important part of the system. Usually in these larger, more diverse data processing applications memory content integrity and reliability become absolutely necessary. Many times special error detection/correction schemes are employed to ensure maximum system reliability. In an error corrected system extra bits of memory are added to each memory word. When the word is written into the memory a hamming type code is generated and stored in the extra bits. When the data is read from the memory the extra bits are used to check the validity of the data. The check code is such that if a single bit of the read word is incorrect it

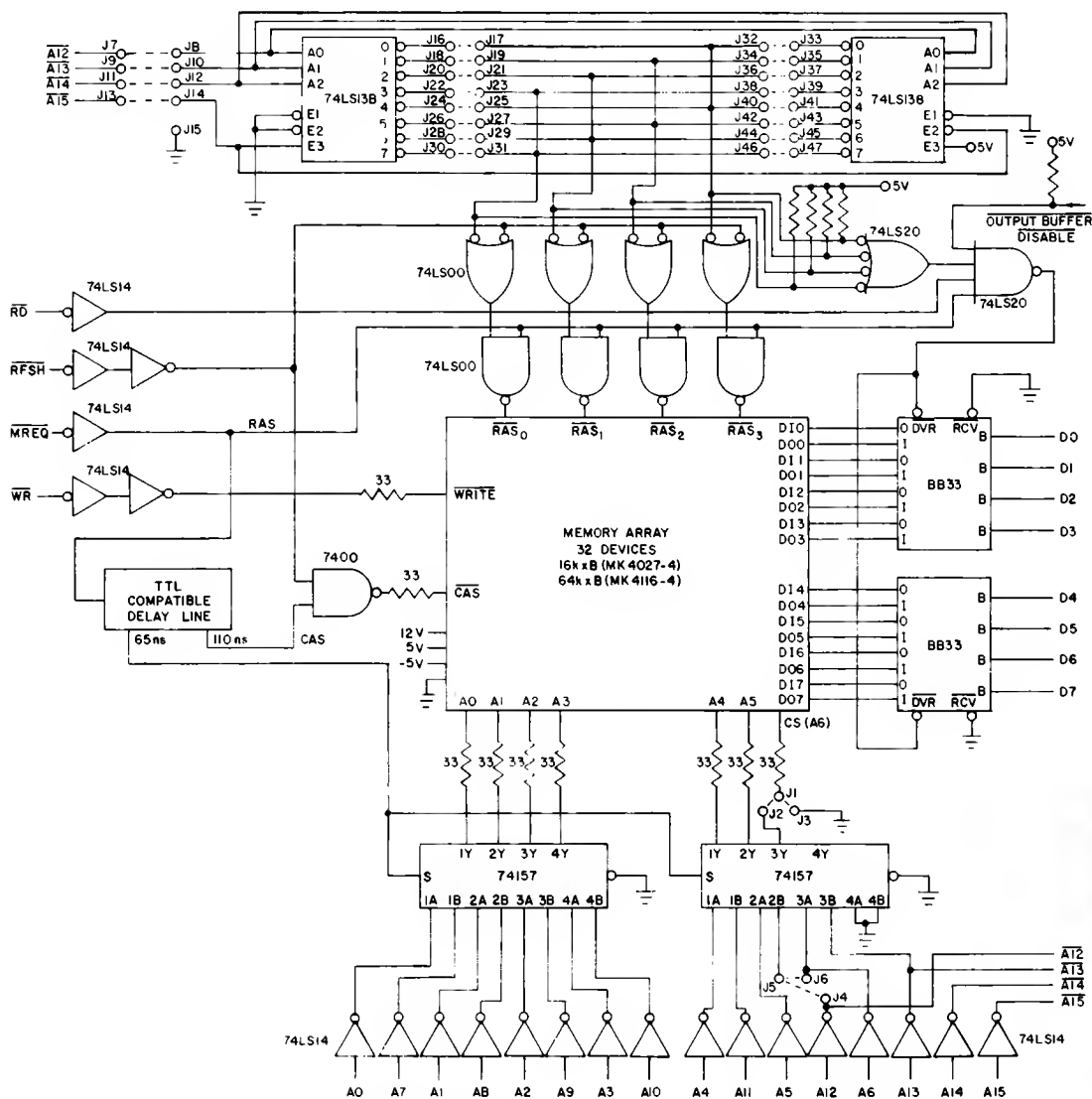
SMALL MEMORY Z80 INTERFACE

Figure 5



LARGE MEMORY Z80 INTERFACE

Figure 6



MINICOMPUTER/MAINFRAME APPLICATIONS (Cont'd)

can be corrected and if two memory bits are incorrect it is detected and flagged as an uncorrectable error. Thus, the error correction allows for a complete memory chip failure while maintaining data integrity. In these types of applications, the 4K and 16K multiplexed Dynamic RAMs begin to have a very significant impact over any previous memory product. In systems like these, read-modify-write cycles and new concepts like "page mode" operation and "read-while-write" memory begin to impact system design.

The "read-while-write" memory operation of the 16K RAM simply implies that both a read operation and write operation can occur at the same memory address almost simultaneously. This is done by strobing both the row and column address into the device and then waiting a sufficient amount of time after the Column Address Strobe is activated before the WRITE command is given. The MK4116 and MK4027 has been designed and characterized such that a read operation can begin at a particular address and, even before data is accessed from the memory, a write operation can begin at the same address and within the same memory cycle. The result of this op-

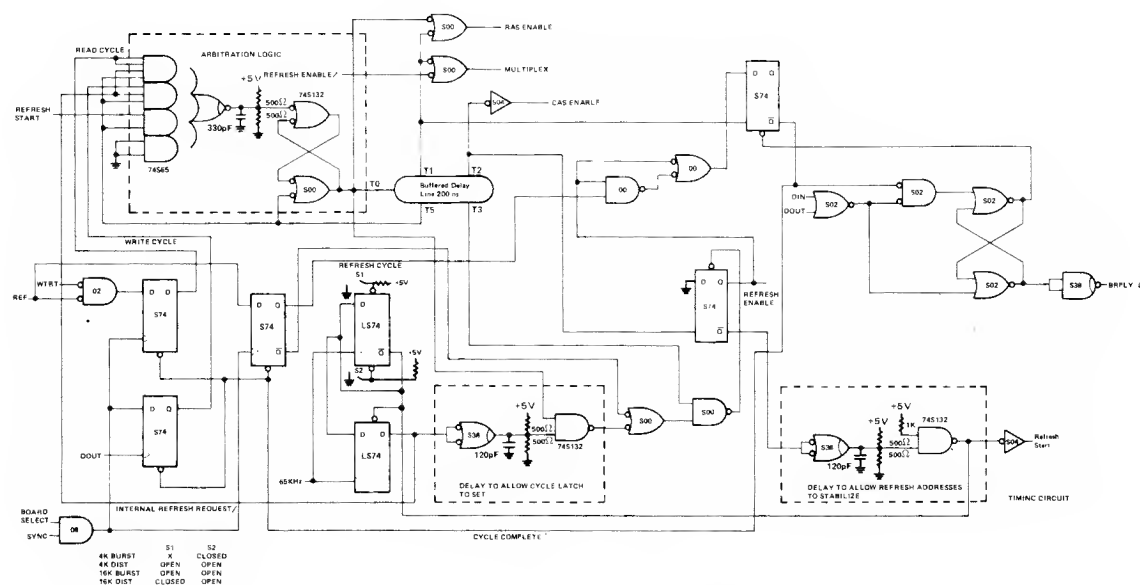
eration is that data stored at a particular cell location will appear at the output of the device within the specified access time and data at the input pin will be written into the same selected cell location. The read-while-write operation is different from a read-modify cycle in that read-modify-write cycle implies that data is read from the selected cell, then modified, and finally the modified data is written into the selected location.

The major design difference between microprocessor and minicomputer memory systems is that on the minicomputer system the memory transfers are very likely to be asynchronous. The main benefit of an asynchronous memory cycle is that it allows the system to operate as fast or as slow as necessary. Thus, when a system is pushed to its performance limits, it is fairly easy to increase the system throughput by upgrading the memory system. This can be accomplished in several ways but the most common approaches are by adding a cache memory (very fast content addressable memory) or by using faster memory devices as main storage. Making the memory system faster makes the asynchronous bus run faster and thus the system performance is improved. There is, however, one major problem with asynchronous busses when Dynamic RAMs are used. Since the asynchronous bus can request a memory cycle at any time there is no convenient time to do refresh. This

Figure 7

COST CONSIDERATIONS

Currently Dynamic RAMs offer about a 2 to 1 cost advantage over Static RAMs on a per bit basis. This



*LSI-11 is a trademark of Digital Equipment Corporation

COST CONSIDERATIONS (Cont'd)

does not mean, however, that Dynamic RAMs are the most cost effective solution for all applications. Factors such as interface complexity, board density, data retention (battery back-up), power supplies, and testing cost have a great deal of influence on the overall memory system cost. The additional cost for a Dynamic RAM interface over a static RAM interface is about \$15. This added cost includes the refresh control and multiplexing logic; and the insertion and testing costs of the added logic. Additional power supply cost can be as small as \$1 if +12 volt and -5 volt supplies are required in the system for other than the memory. It can be as much as \$20 if these supplies must be added just to support the memory. If we assume a \$3.00 component cost for a 4Kx1 Dynamic RAM, a \$15.00 component cost for a 16Kx1 Dynamic RAM and a \$6.00 component cost for a 4K Static RAM, it should be evident that in systems requiring 4K bytes or less of memory the Static RAM is the best choice. For systems requiring 16K bytes or more of memory Dynamic RAMs are the most cost effective mainly because it only takes 8 MK4116's to get 16K bytes vs. 32 4K statics. The resulting savings in board area and insertion costs outweigh the possible extra cost of the power supply and control logic.

A summary of estimated system cost for various memory sizes is given in Fig. 8. For this comparison it is assumed that insertion costs are negligible (they are not in reality) and that the +12V and -5V supplies must be added for the Dynamic RAM system with a cost of \$20 + \$1/watt. For the Static RAM it is assumed only that the +5 volt supply must be increased to support the memory at a cost of \$1/watt. Two types of static RAMs are shown one being a fully static 4Kx1 RAM that requires 500mW/device and the other is an Edge Activated in 4Kx1 RAM that has a frequency dependent power dissipation.

TYPICAL MEMORY SYSTEM COSTS (EXCLUDING PCB)

Figure 8

COMPONENT	MK4116	MK4027				TMS4044				MK4104			
COMPONENT COST EACH (\$)	15.00			3.00				6.00				6.00	
MEMORY SIZE (K BYTES)	16K	4K	8K	12K	16K	4K	8K	12K	16K	4K	8K	12K	16K
MEMORY COMPONENT COST (\$)	128.00	24.00	48.00	72.00	96.00	48.00	96.00	144.00	192.00	48.00	96.00	144.00	192.00
INSERTION COST (\$)	8.00	8.00	16.00	24.00	32.00	8.00	16.00	24.00	32.00	8.00	16.00	24.00	32.00
ADDED POWER SUPPLY COSTS (\$)	22.75	22.76	24.00	25.25	26.48	.79	1.08	1.39	1.69	6.00	12.00	18.00	24.00
INTERFACE COST (\$)	20.00	20.00	20.00	20.00	20.00	3.00	3.00	3.00	3.00	3.00	3.00	3.00	3.00
TOTAL (\$)	178.75	74.76	108.00	1412.00	174.78	59.79	116.09	172.39	228.69	65.00	127.00	189.00	251.00

FUTURE TRENDS IN N-MOS DYNAMIC RAMS

1978 will see the 16K RAM become the mainstay of the industry and attention will turn to the 64K bit Dynamic RAM. Some samples of the 64K RAM will be available by the end of the year but volume production will not be achieved until the middle or end of 1979. The 64K Dynamic RAM should operate on a single supply voltage with +5 volts being the most desirable. This single supply operation will make the 64K dynamic part very easy to design into a system. Not only is power sequencing not required but power distribution and decoupling is simplified. Another benefit is that since the substrate voltage is generated on the chip there is no damage of accidentally shorting the substrate to a positive supply voltage which can destroy the part.

Other strong possibilities for 1978 are Dynamic RAMs in an 8 bit configuration for use in microprocessor systems. These parts will allow for simple interface to microprocessors and present a strong challenge to Static RAMs in low end systems.

Packaging technology for Dynamic RAMs will allow higher densities than is presently possible with the standard DIP. Dynamic RAMs consume so little power that the current 16 pin package is not required for proper heat dissipation.

STATIC RAMS

Static RAM technology has advanced almost as rapidly as Dynamic RAM technology and even though Static RAMs do not match the densities of Dynamic RAMs they are cost effective in many applications. The ease of use of Static RAMs makes them popular devices for small memory systems and the semiconductor industry offers many different types of de-

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NOLOGY

STATIC RAMS (Cont'd)

vices to match the diversity of applications. Most of the current user attention is presently focused on the 4K bit Static RAMs that have become available within the last year. The two most popular configurations for the 4K Statics are the 4Kx1 part with the "Burr-Brown" pinout and the 1Kx4 part with the "Intel" 2114 pinout. The unfortunate thing about most of the new Static MOS RAMs is that besides density they offer very little new in the way of technology. The exceptions to this are the MOSTEK MK4104 and the Intel 2147.

The MK4104 from MOSTEK uses dynamic circuitry in all but the storage matrix. The majority of the power in fully static parts is consumed by the buffers and decode circuitry. By replacing this power consuming static circuitry with very low power dynamic circuitry, MOSTEK achieves a part with the benefits of both Static and Dynamic RAMs, i.e. a Static RAM with low power. The importance of low power in a memory device cannot be overstated. Analysis of a large memory system shows that the memory device remains in a quiescent state most of the time. Therefore, the steady state power of the memory devices determines the power consumed by the memory system. Take, for example, two 16K byte memory systems for a Z80 microprocessor organized as 4 rows of 8 chips (Figure 10) one of which consists of fully Static RAMs with 500mW dissipation for each device and one system employing Edge Activated TM memory system Static RAMs such as the MK4104. The memory system cycle time is 1.2 μ s worst case and then the average cycle time for single row of chips is 4 x 1.2ns or 4.8 μ s. At this cycle rate the system employing MK4104's consumes about 35.2 mw/chip or 1.125 watts for the memory while the fully Static RAM systems draws 500mW/chip or 16 Watts. This factor of 14 in power saving for the Edge Activated TM memory system translates to lower power supply costs, lower cooling costs, and higher reliability. Because the MK4104's only consume an average of 35.2mW the junction temperature inside the package will only be about 2.5°C above the temperature outside the package. The junction temperature of the fully Static RAM will be about 35°C above ambient or over 32°C hotter than the MK4104 in the same environment. MIL-STD-883 predicts that this 32°C difference in junction temperature would make the MK4104 system 14 times as reliable as the fully static memory system.

The 2147 is intended to be a major competitor to the bipolar RAMs that have dominated the sub 100ns memory market. Intel achieves this impressive performance with a process they call H-MOS. This in reality is little more than a slightly scaled process with arsenic diffusion of source and drain.

Because of its high speed and matching price the 2147 has little application in microprocessor systems

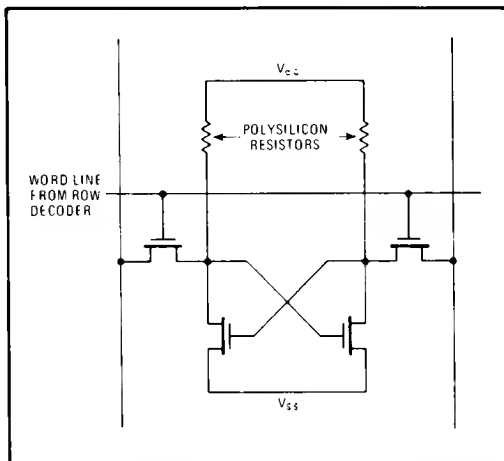
and only limited uses in minicomputers. In minicomputers the 2147 finds its best use in cache and writeable control store applications. Cache memory is a fairly small, high speed content addressable memory that is used to increase the apparent memory performance. When the computer presents an address to the memory system the cache memory is checked to see if the requested data is resident. If it is, the data can be accessed rapidly. If not, a normal memory cycle is initiated and the data is read into the CPU and into cache so that it will be available if required again. The power of cache memory can be seen from a simple example. DEC uses a 2K byte cache on the PDP-11/70 that is backed up by 2M bytes of main memory. 95% of all memory accesses find the required data in the cache ('hit'). If the cache access time is 290ns and the main memory access time is 500ns, the memory system performs as if it were 2M bytes of 310ns memory. Thus, the 2K bytes of cache improves the memory system performance by an impressive 38%. Even if the system uses the memory at only 50% of its capabilities this improves the system throughput by 19%.

Writeable control store allows a computer to have a variable instruction set. The control store of a computer directs the computer in the execution of the instructions. By having a writeable control store it is possible to change the execution of instructions to the point of introducing an entirely different instruction set. Writeable control store is a very powerful mechanism in that it allows the optimization of the instruction set to fit different program requirements and even allows one computer to emulate another. The only problem with the 2147 in cache and writeable control store applications is its 4Kx1 configuration. Because cache and writeable control store generally prefer a small number of wide words this would be better served by a wide word (x8) RAM.

For this reason MOSTEK has developed a 1Kx8 high speed static RAM called the MK4801. The MK4801 utilizes a static storage cell that is very similar to the MK4104 (reference cell dwg. in Fig. 9) with one exception. Rather than returning the load resistors to V_{cc} they are tied to the digit lines. The elimination of the V_{cc} line in the matrix allows the MK4801 to have a basic cell size of only 2.0mil² as compared to 2.7mil². This particular arrangement can be used because the duty cycle of the digit lines is very low meaning that they are almost always at V_{cc}. Keeping the digit lines at V_{cc} requires that the MK4801 operate somewhat differently from typical fully static parts. In the MK4801 an address transition detector is used on each address line. When any address changes, a set of clocks is triggered causing precharge of the output circuitry and other dynamic nodes. The row addresses are decoded in a no power tree decoder and a transition generated clock causes the addressed data to be latched into the output buffers. Once the data is latched the digit lines are again precharged to V_{cc}.

NEW STATIC CELL

Figure 9



A new static RAM cell design that uses resistors as loads saves space and reduces power consumption. Each 5000 megohm resistor is an ion-implanted polysilicon device that draws less than 1 nanoampere of current.

STATIC RAMS (Cont'd)

This marriage of static and dynamic circuit techniques allows the MK4801 to achieve very impressive performance characteristics. The access times are below 100ns with 60ns being typical. Even at 60ns, access time the MK4801 consumes less than 300mW^o (<350mW typical). To the user the MK4801 appears fully static with equal access and cycle times, and fully asynchronous operation.

The MK4801 is packaged in a PROM/ROM compatible 24 pin package and has four control lines that allow easy implementation of a wide range of functions. A Chip Select (\overline{CS}) is included for ease of memory expansion. The \overline{CS} access time is less than 50% of access time so that \overline{CS} decoding does not degrade system performance. The Data I/O lines are bi-directional and the output enable (\overline{OE}) control can be used to prevent possible driver conflicts. The access time from \overline{OE} is also less than 50% of address access.

Naturally one of the control lines is a write Enable (\overline{WE}). When \overline{WE} goes low the output is unconditionally open circuited so that new data can be placed on the data lines. When \overline{WE} goes high the new data is latched on chip and written into the addressed cell.

The fourth control line is on address and chip select latch control (\overline{LATCH}). This is one of the most powerful controls on the MK4801. When the address is latched the MK4801 is forced into a quiescent state and the power dissipation drops by 40%. In systems that must conserve power \overline{LATCH} can be decoded and the selected part unlatched and allowed to access.

Another configuration that can be achieved with the \overline{LATCH} function is a memory system with a multiplexed address and data bus. While the address is valid all chips are unlatched and accept new address and \overline{CS} information. Before the address lines are turned around to transmit data \overline{LATCH} would go low preserving the address and \overline{CS} information. Then when \overline{OE} or \overline{WE} is asserted the selected chip would either place data on the bus or accept new data.

The MK4801 should find wide application in cache, writeable control store and buffer memory applications. Because of the small cell size MOSTEK is able to produce an 8K bit static RAM that is only 27,900 mil² which is only slightly larger than the 2147 4K bit static RAM. This small die size will make the MK4801 a very cost effective part.

The list applications for Static RAMs is endless. The majority of systems using small amounts of RAM, 4K bytes or less, use Static RAMs and one rather large computer manufacturer (IBM) uses Static RAMs almost exclusively in their mainframe computers.

Because the power consumption is such an important factor in memory systems the probability is large that most future generation of Static RAMs will incorporate some sort of power saving circuitry. Even 2147, which is aimed at the bipolar market has a power gating circuit that reduces power to about 150mW when the part is not being accessed. New Static RAMs that are aimed at microprocessor applications will almost certainly contain dynamic circuits and high speed (sub 100ns) MOS RAMs will have either power gating circuits or some other dynamic circuit mechanism to reduce power consumption.

The movement toward Edge Activated TM static memory devices would not occur if users found them more difficult to use. This, fortunately, is not the case and many engineers have discovered that their microprocessor system actually generates what amounts to a clock for their fully Static RAM system. If we look again at the Z80 Static RAM interface board (Figure 10), we find that the output of the chip select decoder is clocked by MREQ. This signal is properly conditioned so that the Edge Activated TM Static RAM directly replaces the fully Static RAM with no change in interface.

One of the most significant indicators that future microprocessor oriented static memory components will need to be Edge Activated TM is the growing trend toward microprocessors with multiplexed address and data busses. Any RAM that interfaces to this kind of microprocessor will need to have on-chip address latches to capture the addresses while they are on the bus or else extra support circuitry would be required. These multiplexed microprocessors supply a signal to cause address capture and if Edge Activated TM memories are used this signal can be

Figure 10



0=Dpen
C=Closed

used almost directly to clock the memory and latch the addresses on the memory chip so that no external latches are required.

CONCLUSION

The developments in NMOS memory technology have been impressive by any standards. NMOS has proven itself repeatedly as the technology holds promise for continued improvement in terms of density, speed, and flexibility. This will undoubtedly lead to further improvements in microprocessor and minicomputer flexibility and processing power.

MOSTEK®

AN UPDATE ON MOS ROMS

Technical Brief

With today's faster, more powerful microcomputer chips emerging in abundance, and larger, more memory-intensive programs being written, semiconductor memory requirements for larger storage capacities, faster access times, and lower subsequent costs have become dominant system design factors. Basic semiconductor memory-chip technology involves variations of random-access memory (RAM) and read-only memory (ROM). RAM allows binary data to be written in, and to be read out. New and different programs and data can be loaded and stored in RAM as needed by the processor. Because information is stored electrically in RAM its contents are lost whenever power goes down or off. When fixed, or unchanging, programs and data are needed by the processor, they are loaded into some form of ROM. In ROM, information is physically (permanently) embedded; therefore, its contents are preserved whenever power is off or interrupted momentarily.

Semiconductor memory chips are normally manufactured using either bipolar or metal-oxide semiconductor (MOS) technologies. Bipolar and MOS memories implement bipolar transistor and MOS field-effect transistor (MOSFET) arrangements, respectively, to store addressable sequences of binary 1s and 0s. MOS memories are either static or dynamic. Static memory depends on a dc level for operation; it is easier to implement in many cases, but requires more power. Dynamic memory requires clock signals or level changes for operation; thus more external circuitry may be needed. However, chip size and thus cost is reduced as is power dissipation.

Typically, ROM has been the limiting component in computer system design, operation, and manufacturability. Problems like slow access time, high power dissipation, long prototype and production cycles, and lack of second sources have concerned computer system and equipment designers. This article summarizes the present MOS ROM state-of-the-art and describes the progress made by the semiconductor industry in manufacturing improved ROMs.

ROM TYPES AND PRINCIPLES

Major types of read-only memory (ROM) are: basic mask programmed ROM; electrically programmable, ultraviolet erasable (EPROM); electrically alterable (EAROM); electrically erasable (EEROM); and field

programmable (p/ROM). EPROM is electrically programmable, then erasable by ultraviolet (UV) light, and programmable again. Erasability is based on the floating silicon gate structure of an n- or p-channel MOSFET. This gate, situated within the silicon dioxide layer, effectively controls the flow of current between the source and drain of the storage device. During programming, a high positive voltage (negative if p-channel) is applied to the source and gate of a selected MOSFET, causing the injection of electrons into the floating silicon gate. After voltage removal, the silicon gate retains its negative charge because it is electrically isolated (within the silicon dioxide layer) with no ground or discharge path. This gate then creates either the presence or absence of a conductive layer in the channel between the source and the drain directly under the gate region. In the case of an n-channel circuit, programming with a high positive voltage depletes the channel region of the cell; thus a higher turn-on voltage is required than on an unprogrammed device. The presence or absence of this conductive layer determines whether the binary 1-bit or the 0-bit is stored. The stored bit is erased by illuminating the chip's surface with UV light. The UV light sets up a photocurrent in the silicon dioxide layer which causes the charge on the floating gate to discharge into the substrate. A transparent window over the chip allows the user to perform erasing, after the chip has been packaged and programmed, in the field. EAROMS use electrical pulses to clear all bits simultaneously.

The p/ROM has a memory matrix in which each storage cell contains a transistor or diode with a fusible link in series with one of the electrodes. After the programmer specifies which storage cell positions should have a 1-bit or a 0-bit, the p/ROM is placed in a programming tool which addresses the locations designated for a 1-bit. A high current is passed through the associated transistor or diode to destroy (open) the fusible link. A closed fusible link may represent a 0-bit, while an open link may represent a 1-bit (depending on the number of data inversions done in the circuit). A disadvantage of the fusible-link p/ROM is that its programming is permanent; that is, once the links are opened, the produced bit pattern cannot be changed.

Two other types of p/ROM that are not as prevalent in the industry, but deserve mention are EEROM and

EAROM. The first, EEROM or electrically erasable ROM, works similarly to the "floating gate" EPROM but can be erased (all bits) by electrically pulsing the device. The EAROM or electrically alterable ROM utilizes special processing techniques that allow bit locations to be reprogrammed at any time. However, unlike a RAM, the write cycle is very long preventing its use as a non-volatile RAM where both read and write cycles are to be used. Both EEROM and EAROM are used mostly in specialized applications where nonvolatility and electrical erasability are requirements.

In mask-programmed ROM, the memory bit pattern is produced during fabrication of the chip by the manufacturer using a masking operation. The memory matrix is defined by row (X) and column (Y) bit-selection lines that locate individual memory cell positions.

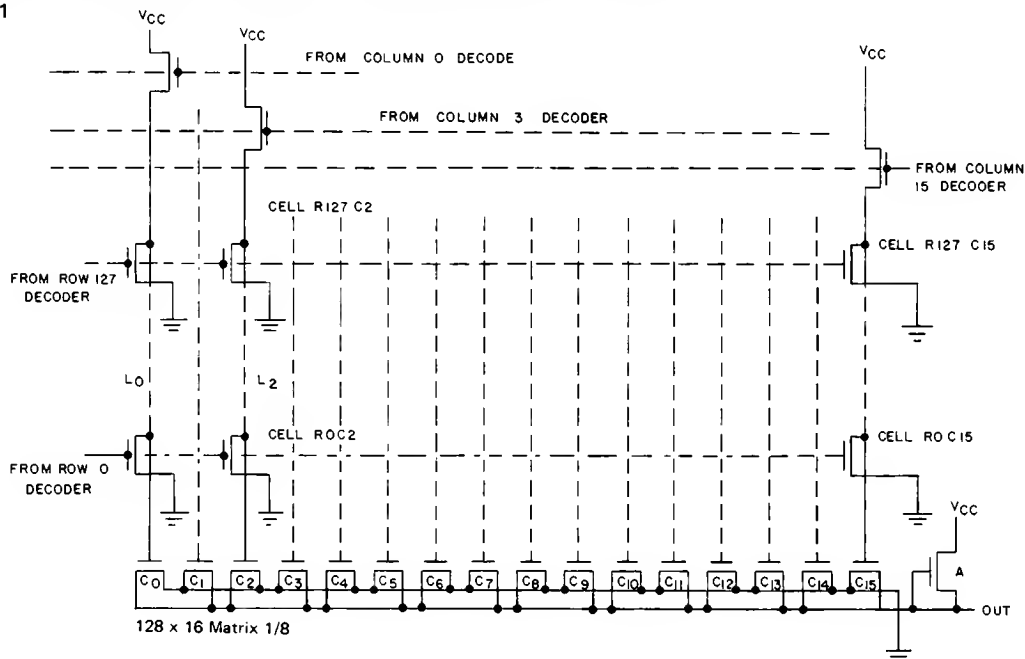
For example, in Fig 1 refer to column C_2 and row 127 as the storage cell location of interest. When the proper binary inputs on the address lines are decoded, the cell at R_{127}, C_2 will be selected. If the drain contact of this cell is connected to bit line L_2 , then L_2 will be pulled below threshold, turning off device C_2 ; note that devices C_0, C_1 , and C_3 through C_{15} will also be off since they are not addressed. Therefore, device A pulls the OUT line to V_{CC} for a logic 1 output when cell R_{127}, C_2 is selected.

Alternatively, consider when cell R_{127}, C_2 is masked it does not have a drain contact to bit line L_2 . Then when this cell is addressed, device C_2 is now connected to V_{CC} and will be turned on. Thus, the OUT line will be pulled to ground through device C_2 and will appear as a logic 0 output. To program a 1 or a 0 into a ROM storage cell, the drain contact will or will not be connected, respectively, to the particular bit line. Note that this type of programming is permanent. An alternative method of performing the same operation would be to eliminate the gate of the storage cell.

Typical ROM applications include code converters, look-up tables, character generators, and nonvolatile storage memories. In addition, ROMs are now playing an increasing role in microprocessor-based systems where a minimum parts configuration is the main design objective. The average amount of ROM in present microprocessor systems is in the 10K- to 20K-byte range, while some applications utilize as much as 30K or 40K bytes. Fig 2 shows a block diagram of a typical microprocessor system in which ROM is the predominant program storage element. In this particular application, the 16K ROM is used to store the control program that directs CPU operation. It may also store data that will eventually be output to some peripheral circuitry through the CPU and the peripheral input/output (P I/O) device.

PORTION OF ROM MATRIX AND OUTPUT CIRCUITRY OF MK 34000

Figure 1



If drain contact is made (1 state) when particular cell is accessed, storage transistor will cause OUT line on device A to pull high (to V_{CC}). If contact is not made to drain, device will pull OUT line low (0 state).

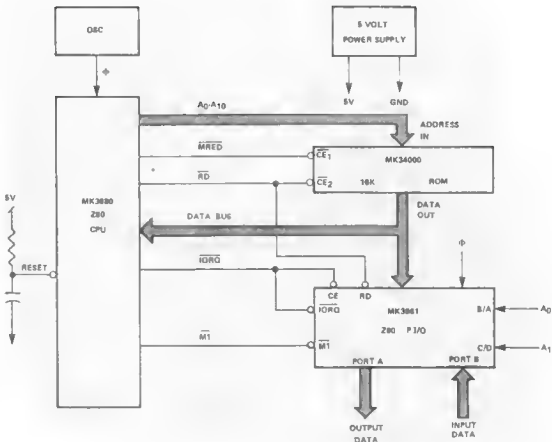
SYSTEM DEVELOPMENT CYCLE

In a microprocessor system development cycle, several types of memory (RAM, ROM, and EPROM or p/ROM) are normally used to aid in the system design. After system definition, the designer will begin developing the software control program. At this point, RAM is usually used to store the program, because it allows for fast and easy editing of the data. As portions of the program are debugged, the designer may choose to transfer them to p/ROM or EPROM while continuing to edit in RAM. Thus, he avoids having to reload fixed portions of the program into RAM each time power is applied to the development system.

Decision making on the part of designer and manufacturer is required during the next step in the development cycle. Depending on the type and quantity of microprocessor systems to be produced, a decision has to be made as to whether ROM, p/ROM, or EPROM will be used for permanent program storage. If only a few systems are to be manufactured, it may be more cost-effective to use either p/ROM or EPROM. EPROM-based storage also allows the main program to be changed at any time, even in the field by the end-user. The p/ROM-based system requires replacement; however, it is field programmable. If the main requirement is a minimum parts configuration and many microprocessor systems must be produced the decision should be to use ROM-based storage.

MICROPROCESSOR BLOCK DIAGRAM

Figure 2



Typical microprocessor system utilizes CPU, P I/O, and 16K ROM.

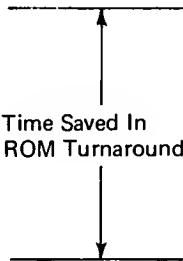
For many designs, fast manufacturing turnaround time on ROM patterns is essential for fast entry into system production. This is especially true for the consumer "games" market. Several vendors now advertise turnaround times that vary from two to six weeks for prototype quantities (typically 25 pieces) after data verification. Data verification is the time when the user confirms that data have been transferred correctly into ROM in accordance with the input specifications.

Contact programming is one method that allows ROM programming to be accomplished in a shorter period of time than with gate mask programming. The step-by-step ROM manufacturing process is listed in Table 1. N-MOS ROMs go through basically the same processing steps. In mask programming, most ROMs are programmed with the required data bit pattern by vendors at the first (gate) mask level, which occurs very early in the manufacturing process. In contact programming, actual programming is not done until the fourth (contact) mask step, much later in the manufacturing process. That technique allows wafers to be processed through a significant portion of the manufacturing process, up to "contact mask", and then stored until required for a user pattern. Some vendors go one step further and program at fifth (metal) mask. This results in a significantly shorter lead time over the old gate-mask-programmable time of 8 to 10 weeks; the net effect is time and cost savings for the end user.

MOS ROM MANUFACTURING PROCESS FLOW

Table 1

- Wafer
- Oxidation
- Nitride
- First Mask (Gate Mask)
- Etch
- Second Mask
- Implant
- Polysilicon
- Third Mask
- Oxidation
- Fourth Mask (Contact)
- Etch
- Metallization
- Fifth Mask
- Glassification
- Sixth Mask
- Test
- Assemble
- Ship



TECH
NOLOGY

ROM VS DISCRETE LOGIC COSTS

Table 2

ROM Capacity (Total Bits)	ROM Cost	Functional IC Gates	ICs	Estimated IC Dollars
8K	\$7 to 8	500 to 999	50 to 99	\$20 to 39
16K	\$8 to 9	1000 to 1999	100 to 199	\$40 to 79
32K	\$16*	2000 to 3999	200 to 399	\$80 to 159
64K	\$20*	4000 to 7999	400 to 799	\$160 to 319

*Projected cost

COST CONSIDERATIONS

Consider a typical microprocessor system and what ROM can provide in terms of cost savings over discrete logic and EPROM. Assume that a single gate function can be replaced with eight to ten bits of ROM and that most of today's transistor-transistor logic (TTL) integrated circuits (ICs) contain on the order of ten functional gates having an average selling price of \$0.40. The typical microprocessor system contains 20K bytes of ROM. Table 2 compares the costs of ROM versus discrete logic.

From the table, one 16K (2048 x 8-bit) ROM can replace 100 to 200 TTL packages. Depending on the total quantity of ROMs required, it can be seen that they are a cost-effective alternative to discrete logic.

Additional savings are possible when ROM is used. Board area is reduced, which lowers material cost; fewer packages reduce insertion costs; and, with smaller boards and fewer interconnections, the cost of incoming inspection is also decreased. When board troubleshooting costs go down, overall system reliability increases.

At this time, the largest cost-effective EPROM size available is 1024 x 8 bits or 8192 total bits. However, there are many 2048 x 8 bit, or 16K ROMs available. At an average selling price of \$16/EPROM and \$8/ROM, it is evident that ROM remains the most cost effective solution. For every two 8K EPROMs, only one 16K ROM is needed. The disadvantage of ROM in small quantities is the mask charge (usually \$500 to \$1000). In larger production quantities, the mask charge is waived when a minimum number of parts have been purchased (typically 500 to 1000 pieces/pattern).

KEY PERFORMANCE

With faster and more powerful microprocessors entering the market, ROM performance is more important than ever, especially since ROM has typically been the limiting factor in system processing

speed and operation. When 16K ROMs were introduced several years ago they were fairly slow, with access times ranging from 550ns to well over 1.0 μ s. These ROMs made it difficult to take advantage of the full speed capability of newer microprocessors. If processing speed was paramount, the designer usually selected bipolar ROMs, which possess fast speed but have high power dissipation. Density costs are also higher.

Newer MOS ROMs (such as the MK34000, and and 36000) provide the system designer with both speed and density. Access time is 300ns worst case, specified over the full power supply and temperature ranges. In addition, since many microprocessors now have only a single power supply requirement (5V), the trend in 16K/32K/64K ROM designs is also slanted to this single voltage. Most vendors offer a $\pm 5\%$ supply voltage tolerance and at least one specifies $\pm 10\%$.

OTHER PARAMETERS

Many ROM-based memory applications are subject to various detrimental environmental conditions. For instance, an intelligent data entry terminal used on a busy outdoor loading dock could be exposed to vibration-generated electrical noise, extreme temperature variations from -20 to 125°F (-28 to 51°C), machine-generated noise, and power line fluctuations. Critical ROM parameters, such as temperature range, input levels, output drive, power supply tolerance, and power dissipation, are being accommodated by innovative memory design and processing techniques to optimize performance and reliability.

Extensive use of ion implantation as a means of controlling circuit zero bias threshold voltages is now prevalent. One ROM vendor uses a substrate bias generator, often called a charge pump which results in much wider operating tolerances. Input levels of 2.0V, $\pm 10\%$ power supply tolerances, wider operating temperature ranges, faster access times, and lower power dissipation are now available.

Important data sheet parameters that a designer should examine when specifying ROMs are listed in Table 3. Of course, which parameters are important to the individual designer depends entirely on the application. In the loading dock example cited previously, temperature range may be the most critical. In a military airborne application, temperature range and power dissipation would be most important.

IMPORTANT DATA SHEET PARAMETERS

Table 3

General

Absolute maximum voltage ratings — voltages beyond which parts are likely to be destroyed

Absolute maximum temperature — operating and storage temperatures beyond which parts may be permanently damaged

“Recommended” operating conditions— operating conditions that the manufacturer requires for proper operation

DC parametrics— current and voltage parameters at specified conditions

Timing diagrams — part timing specifications essential for system design

Capacitance specifications — particular input and output specifications required to avert drive problems

Package specifications— pin-outs and package mechanical data for layout and environmental requirements

Specific

Voltage and current levels — input and output low and high voltage and current levels on all inputs and outputs

Power supply regulation — detailed power supply regulation specifications

Output capacitance test value — this value determines maximum number of parts which can be strung together and still meet specifications

Standby and output leakages

Input and output leakages

Timing parameters — all timing parameters required to totally specify system operation

Input methodologies — ROM’s truth table should indicate accepted input methodologies including card, tape, or transmit formats

Operating temperature specifications — should allow for proper system margins after enclosure temperature rises are taken into account

CHARGE PUMP TECHNIQUE

Although the ROM charge pump technique has been utilized for several years, a new design approach has evolved (Fig 3). The charge pump is an on-chip bias generator that is used to shift the thick-field thresholds (V_T) to their proper operating levels, as well as to reduce junction capacitance of the circuit. In dynamic RAMs, an external V_{BB} power supply is used for this purpose. This fixed value bias is useful, as such, but it does not compensate thresholds over temperature. In the MK34000 and 36000 ROMs (16K, and 64K respectively), the charge pump approach does temperature compensate for thresholds by utilizing a method of V_T feedback. A threshold detector compares V_T values of the circuit with an on-chip voltage reference (V_R). Significantly, V_R is always a fixed percentage of the V_{CC} supply rather than being V_T dependent. Normally, the V_{CC} supply can be held constant over a specified temperature range; thus, the reference will also remain constant, keeping V_T constant. Even if the supply voltage changes, the reference voltage will cause the effective V_T to be within its operating range for a particular supply potential.

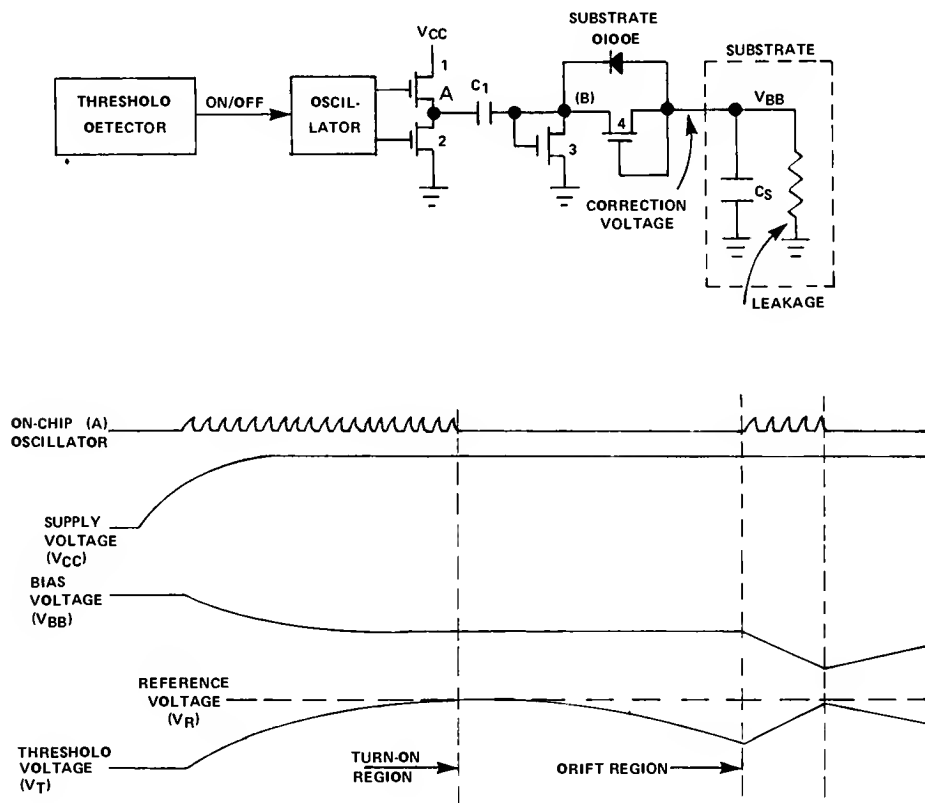
The bias generator is actually an on-chip gated oscillator (A) that, when operating, “charges up” the substrate capacitance of the chip with a negative potential. The threshold detector will turn the oscillator on or off if it detects either an inequality or an equality, respectively, of V_R and V_T . This is especially important for V_T versus temperature. Typically, as temperature goes up, V_T goes down; with normal process tolerance included in the total V_T , this could severely limit the allowable specified levels and temperature range. The threshold detector is sufficiently accurate so that it can compensate for small changes in V_T during normal operation of the part. Fig 4 shows the behavior of V_T , V_{BB} , and compensated V_{TC} over an extremely wide temperature range. The outstanding feature of the compensated V_T curve, is that it is flat over a significant range in temperature. It can be shown that the overall effect is an improvement in system margins, improved yields, and reliability. This is all possible with no increase in chip size and an insignificant increase in power supply current (typically 1 mA).

SYSTEM RELIABILITY

Replacing many random logic circuits with a single MOS ROM not only makes good economic sense, but also significantly increases reliability. Printed circuit (PC) board area is reduced along with a multitude of system interconnections. It is possible for a single ROM to eliminate 2000 interconnections when bonding wires and PC board etches are taken into account. This means fewer chances for opens, shorts and layout problems. When using ROMs, troubleshooting is

ON-CHIP SUBSTRATE BIAS GENERATOR

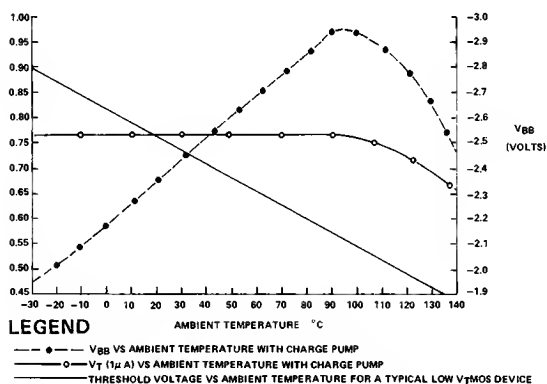
Figure 3



Simplified circuit diagram of an on-chip substrate bias generator which utilizes a method of V_T feedback. Circuit will only generate a negative bias when V_T does not equal reference voltage. When operating, circuit draws a minimum amount of power while requiring no additional layout space on chip.

OPERATING MARGINS

Figure 4



By comparing curves showing V_T versus ambient temperature for circuit with and without substrate bias generator, it can be seen that operating margins of a noncompensated device may be quite limited. By utilizing V_T feedback method of device operation, V_T can be held constant over significantly wide temperature range. Plot also shows V_{BB} versus temperature with generator operational.

simplified because there are fewer components, interconnects, and contacts.

In addition, vendors have learned techniques for lowering the power supply current requirements of ROMs. One method utilized is a static matrix with dynamic or "edge activated" control circuitry. The MK36000 ROM, for instance, draws a typical average current of only 40mA, compared with 80mA typical of a comparable density totally static device. When supply current is low, chip temperature is low and reliability is enhanced.

Many vendors now offer enhanced reliability screening as an option. This screening may include temperature cycling for detecting die- and bond-related problems, and also fine and gross hermeticity testing. In addition, many offer an option on burn-in to weed out infant mortalities. Extended temperature range 16K ROMs are available, as well as devices processed to MIL-STD-883A, Level B. Table 4 lists the 100% screening requirements called out by this specification. While this screening has historically been reserved for military applications, more users are requiring it as a matter of course. Screening of this type means that the user receives the highest reliability possible in his parts.

SCREENING REQUIREMENTS SPECIFIED FOR MIL-STD-883, CLASS B

Table 4

Test	Method	Condition	Test Level
Visual	2010.2	Condition B	100%
Stabilization Bake	1008.1	Condition C 24h at 150°C	100%
Temperature Cycles	1010.1	Condition C -65 to 150°C 10 cycles	100%
Centrifuge	2001.1	Condition E 30k Gs Y1 Plane	100%
Hermeticity Fine	1014.1	5×10^{-8} Atm-cm ³ /s	100%
Gross	1014.1	Condition C	
Pre-Burn-In Electrical Test	Static and Dynamic Tests		Mfg's Option
Burn-In	1015 (Dynamic Operating)	Condition D 160 h min at TA=125°C	100%
Final Electricals	Static and Dynamic per Data Sheet		100%
Quality Conformance	See Mfg's Quality Specification		Sample
External Visual	2009		100%

CONCLUSIONS

Turnaround time has been reduced to a tolerable level, pin-outs are being standardized, ROMs are providing larger memory capacity with higher performance, and data are more easily transferred. In the future, the greatest number of applications will most likely be in microprocessor systems. Microprocessor memory requirements continue to increase as control programs get larger and applications become more sophisticated. Concurrently the microprocessor is becoming higher performance with more control capability, as witnessed by recent 16-bit high speed devices. Today's new generation MOS ROMs are being designed to interface directly and easily while occupying a minimum of space. The importance and necessity of ROMs to system design have resulted in a continual effort by the semiconductor industry to improve performance, reliability, and cost.

ABSTRACT

In the past decade the computer industry has witnessed the introduction and domination of the MOS RAM. Technology changes from PMOS to NMOS occurred with storage mechanisms going from 3 elements to 1. Density, correspondingly improved by a factor of 16 times while performance improved by a factor of 2. In this time frame devices evolved from complex interface requirements to simple TTL circuitry. These remarkable performance/density improvements were achieved with clever process and design innovations. Techniques used in the past have reached their limit with ROM at 64K, dynamic RAM at 16K and static RAM at 8K. A new technology will need to emerge to permit further density improvements for the future. Process and design techniques of the past and future will be discussed with attention paid to products and applications they will serve and create.

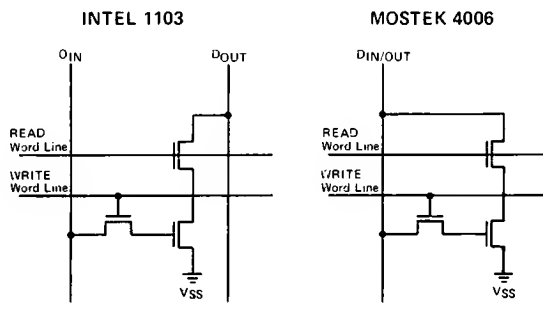
INTRODUCTION

The first density increment of MOS RAM to gain wide acceptance in the computer industry was the 1K device. The 1K device utilized P-Channel MOS technology due to the more tolerant nature of the process. Unlike its predecessors the 64 and 256 bit RAM, the 1K devices incorporated all decoding circuits on the chip. The 1K market was dominated by the 1103 from Intel and the 4006 from MOSTEK. The 1103 and 4006 were both dynamic memory devices using a small capacitor to temporarily store data. This storage technique required a periodic refreshing to retain data. The 1103 required high level clocks and complex timing considerations while the 4006 was designed for TTL compatibility and minimal timing requirements. The 1103 became the dominant part and was still being consumed in volume last year. The 4006 pinout was used by a static RAM of 1K bits. This device generically known as the 2102 has enjoyed enormous usage.

The 1103 and 4006 utilized a three transistor cell for bit storage. These cell configurations are illustrated in Figure 1. The primary difference in these cells being separate Read, Write, buses required by the 1103. These devices, the most dense of their generation, packaged 1024 bits of RAM in approximately 20K sq. mils of silicon. The 1K device promised ease of implementation when compared to core, and flexible

INTEL 1103 AND MOSTEK 4006

Figure 1



modularity as well as long term cost savings. However, due to unforeseen design complications these devices initially did not achieve their goal. The 1K RAM started the displacement of core. The next generations, the 4K and 16K dynamic RAMs, all but completed the task.

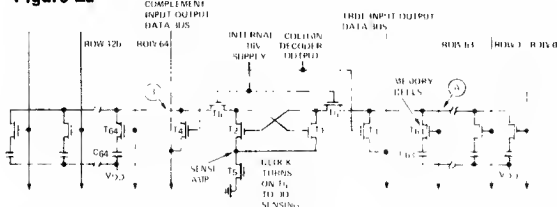
The 4K device, which became the next generation of semi-conductor memory, introduced to the world a wide variance in circuit types available. There were at least 5 major designs available to confuse the user. These were two differently pinned 22-pin devices, two differently pinned 18-pin devices, and a "maverick" 16-pin device which many people thought would never make it. As we all know today, the multiplexed device survived and in fact went on to become the industry standard. This standard pin configuration is presently being utilized in the 16K device as well as its successor the 64K RAM. The first 4K devices utilized a 3 transistor cell similar to that of the early 1K devices. However, N-channel MOS was the technology of all 4K devices rather than P-channel. The inherent advantages of N-channel such as low thresholds for TTL compatibility, faster inherent speed, and greater density, created the incentive needed to develop the required process capability.

The early 3T 4K devices did not survive and were rapidly replaced with the second generation 4K, which utilized a single transistor and capacitor for storage to greatly enhance density. The major problem to overcome with this cell was the small amount of signal available for detection. Several sensing

schemes were developed to handle this problem. One technique utilized a single ended sense amplifier. The balance technique had far better characteristics and became the dominant technique which is utilized today. These different sense configurations are shown in figure 2. It must be appreciated that without development of these sense amplifiers the single transistor cell would not be possible. MOSTEK combined an innovative layout scheme with the balanced sense amp to permit use of active rather than passive load circuits for writing through the sense amplifier. This has resulted in a halving of the dynamic RAM's power dissipation. The 4K devices were well accepted by the user community and slowly but surely began a long but continuous displacement of core memories.

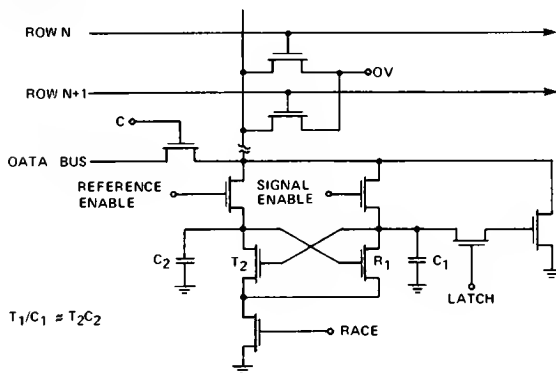
BALANCED SENSE AMPLIFIER

Figure 2a



SINGLE ENDED SENSE AMPLIFIER

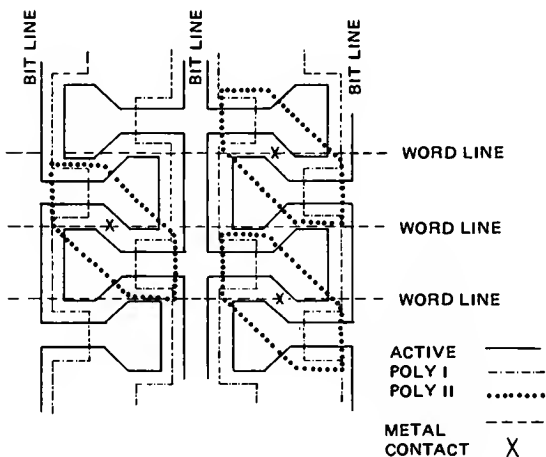
Figure 2b



The MK 4096 introduced by MOSTEK in 1973 established the industry standard pin out. The successor to the 4096 was the revolutionary MK 4027 from MOSTEK which dramatically reduced the die size while dramatically improving the speed. The 4027 set new standards within the industry and established the specification standards that have to be met. The 4027 utilizes MOSTEK's process known as Poly I. This process utilizes a single transistor cell which has an area of about 1.008 mil². The successor to the 4027 is MOSTEK's MK 4116, 16K dynamic RAM. The 16K was made possible by the Poly IITM process which reduced the single transistor cell size to .55 mil². The Poly IITM process utilizes two levels of Poly in the cell location. The implementation of this cell is shown in figure 3.

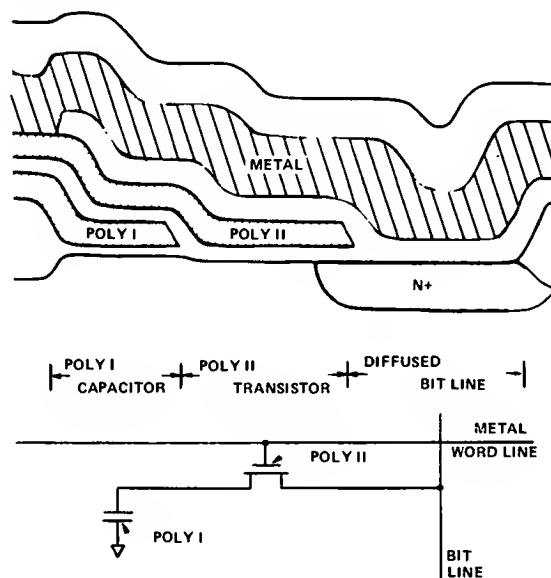
MK4116 CELL LAYOUT

Figure 3a



MK4116 CELL AND CROSS SECTION

Figure 3b

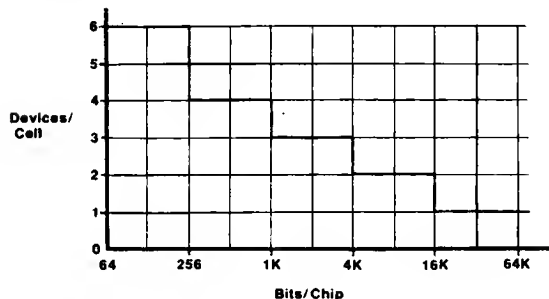


RAM density improvements in the past have come from both circuit and process innovations. The graph of figure 4 shows the evolutionary decrease in the number of devices per cell as a function of density increase. Today we are at a minimum cell configuration, one transistor and one capacitor. The Poly II (TM) process permits packaging the capacitor and transistor in the space of only one device, since no layout space is required to separate these components as in the Poly I process. A further decrease in

the number of components or improvements in layout seems unlikely. Process innovation will, however, continue. In devices through 16K a two dimensional shrinking of dimensions has been employed along with circuit improvement to create a manufacturable die size.

DEVICES/CELL VS BITS/CHIP

Figure 4

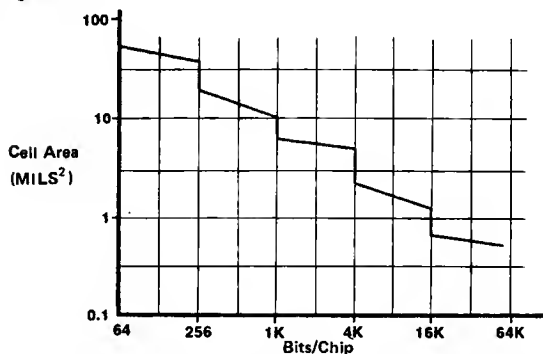


SQUEEZING

In the past device density has increased by reducing the number of elements per cell as well as a two dimensional reduction in geometry. The two dimensional reduction results in a "squeezing" of signal lines and spaces. The graph of figure 5 illustrates the storage cell area advantage gained by this technique.

MEMORY CELL AREA VS BITS/CHIP

Figure 5

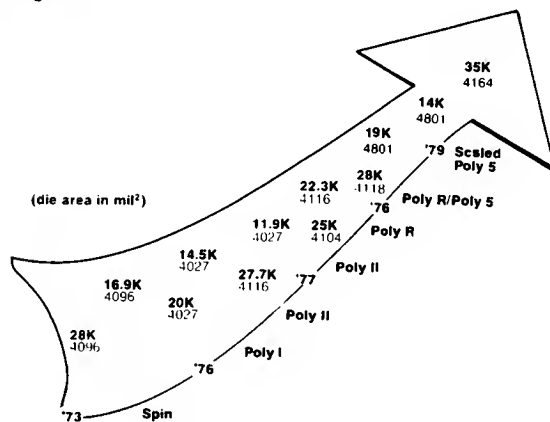


The slope in the graph lines indicate the squeezing mechanism while the verticle steps show cell element reduction. The one anomaly to this lies in the 4K region. Significant area reduction here was achieved by going from the MK 4096 metal gate single transistor cell to the silicon gate single transistor cell of the MK 4027. This required a major technology improvement as did the Poly II (TM) process of the 16K.

Two dimensional squeezing has been used on all previous generation products. Reductions of up to 40% have been realized, for a given design, using this technique. The chart of Figure 6 illustrates the die size and technology evolution of several major products from MOSTEK.

RANDOM ACCESS MEMORY DENSITY EVOLUTION

Figure 6



Looking back historically, the replacement of each generation MOS RAM by its successor has taken place by introducing a new memory cell of about one half the area of its predecessor and by tightening design rules used. As a result die size has increased by about a factor of 2 while the number of bits per chip has increased by a factor of 4. It is interesting to note that in evolving from a 64 bit device to a 16K device the RAM circuit density has increased by a factor of more than 60.

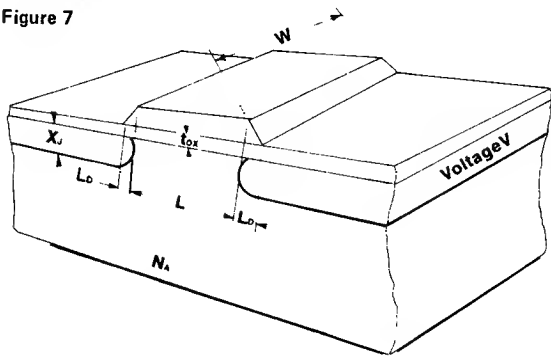
The devices per cell now stand at an effective 1, due to the Poly II process. It therefore seems unlikely that a further density improvement will happen here. The next generation will require significant improvement in the remaining area of impact, that is, device geometries. The technique which currently looks the most promising, and is being pursued by multiple companies, is known as scaling.

SCALING

Scaled process technology will be the process which permits the next generation of semiconductor components. "SCALED" refers to circuits in which all physical dimensions, horizontal and vertical have been reduced by scaling factor, as has the operating voltage. This differs from the "squeezing" previously discussed in that 3 dimensions rather than 2 are impacted. Figure 7 shows three dimensional characteristics affected by scaling. In scaling theory all parameters are scaled by a factor K. For a 5 volt part scaled from 12 volts to 5 volts the scaling factor K is 5/12ths. Figure 8 shows MOSTEK's current N-MOS technology compared to resulting geometries based on applying a 5/12ths scaling factor. This approach yields "a brute force" process which will not necessarily be manufacturable. Therefore, a slight modification to the straight-forward scaling technique must be made.

SCALING THEORY

Figure 7



“BRUTE FORCE” APPROACH

Figure 8

Try K = 5/12

Device Parameter	Current N-MDS	Scaled By	“Brute Force”
Channel Length L_{ch}	5	5/12	2.1
Oxide Thickness t_{ox} (Å)	850	5/12	354
Doping Concentration N_A (substrate resistivity) ($10^{17}/cm^3$)	10	12/5	2.4×10^{16} ($6 \Omega \cdot cm$)
Power Supply Voltage (V)	12	5/12	5
Junction Depth X_j	1.2	5/12	.45
Lateral Diffusion L_o	1.0	5/12	.41

The benefits of scaling are numerous. The most significant is that die area goes down by a factor of K² permitting the next generation of products. A second benefit of scaling is that device performance increases dramatically thereby permitting the N-MOS technology to participate in a broader applications spectrum than was previously available. The process developed by MOSTEK applying scaling theory is called SCALED POLY 5.

SCALED POLY 5

Scaled Poly 5 is MOSTEK’s process for the next generation of products. Scaled Poly 5 is MOSTEK’s customized utilization of the scaling theory previously discussed. In the section on Scaling Characteristics, characteristics of “brute force” scaling were shown. Figure 9 gives the key parameters of MOSTEK’s process.

SCALED POLY 5

Figure 9

Try K = 5/12

Device Parameter	Current N-MOS	Scaled By
Channel Length L_{ch}	5	2.5
Oxide Thickness t_{ox} (Å)	850	500
Doping Concentration N_A (substrate resistivity) ($10^{17}/cm^3$)	10	5×10^{16} ($30 \Omega \cdot cm$)
Power Supply Voltage (V)	12	5
Junction Depth X_j	1.2	0.4
Lateral Diffusion L_o	1.0	0.3

The modifications to “brute force” scaling were made to enhance manufacturability, performance and reliability. For example, the low substrate resistivity (6 ohm per centimeter) would result in higher junction capacity and body effect. Both are undesirable traits impacting performance. One must also consider manufacturing tolerance on parameters. This is a defi-

nite consideration when choosing a center for process parameters.

Reliability is a major concern. It was learned early in semiconductor memory days that an unreliable part cannot be applied to products. The scaled Poly 5 process has been optimized to meet MOSTEK’s high standards of reliability. Scaling’s impact on reliability influencers is shown in figure 10. The decrease in voltage and power dissipation will improve the inherent reliability of the device. The increase in current density shown will not impact the device due to the overly conservative guidelines used in past generations.

SCALING AND RELIABILITY

Figure 10

Reliability Parameter	Scaled by
Field Strength V/cm	1
Power Per Unit Area W/A	1
Current Density I/A	1/K
Device Power Dissipation	K ²
Device Voltage	K

1978 is a transition year between process technologies. At MOSTEK, all new products are being designed to work on either current process technology (5 microns) or new generation SCALED POLY 5. To accomplish this goal all new products are designed to operate on a single 5 volt power supply. All products use advanced state-of-the-art design techniques and perform very respectably on the standard process. The MK36000 64K ROM which has a typical access time of 80ns when manufactured utilizing Poly 1 process exemplifies this approach. This design was used as an R&D development tool for the Scaled Poly 5 process. The resulting device, termed MK 9009, has a typical access time of less than 40ns. Figure 11 gives the characteristics of the two devices.

POLY 5 PROCESS DEVELOPMENT

Figure 11

	MK36000	MK9009
Die Dimensions	183 X 190 MILS	105 X 109 MILS
Die Area	34,776 Sq. MILS	11,445 Sq. MILS
No. of Die/Wafer (3")	170	S75
Min. Poly Width	5.0 Microns	2.5 Microns
Min. Line Width	2.5 Microns	1.0-1.5 Microns
Junction Depth	1.3 Microns	.4 Microns
Access Time	80 nsec (typ)	40 nsec (typ)

SCALED POLY 5 PHOTOLITHOGRAPHIC REQUIREMENTS

We previously discussed the evolution of device/die size to achieve the level of integration required. Correspondingly, device geometries have significantly decreased. Geometry requirements as a function of device technology are shown in figure 12. During the evolutionary period from 1960 thru now, geometry requirements have increased by more than a factor of 5. Significant developments have also occurred in photolithographic technology to permit evolution from 1K to 16K. In 1980 our goal is to manufacture devices with two micron dimensions. A quick snapshot of typical equipment used in this segment shows

several problems must be overcome. Today's measuring equipment is accurate to a ± 0.18 microns (10% of what is to be measured). Measurement standards are accurate to ± 0.1 microns. The contact printers have a runout of ± 0.75 microns on 4 inch wafers, a huge percentage of the geometries involved for future technology. Advances in this area are obviously required. These are being attacked and overcome. Methods such as E Beam as well as "step and repeat" printing are available today. These techniques have the ability to address and resolve some of the problems facing the manufacturing aspect of the next generation of technology.

GEOMETRY REQUIREMENTS

Figure 12

	1960	1965	1970	1975	1980
Leading Technology	Discrete	Digital	P-Mos	N-MOS	Poly 5
Line Width (Microns)	10.0	7.0 - 9.0	5.0 - 8.0	3.5 - 5.0	2.0
Interconnect Technology	Metal	Metal	Metal	Metal Poly	Metal-Double Level Poly

The key to more complex, cost effective LSI is in Geometry Shrink and Device Creativity.

APPLICATIONS SPECTRUM

Circuit design and technology improvements are continuously opening up new markets for semiconductor memories. The semiconductor industry historically has decreased prices by about 28% with each volume doubling of the industries experience. Fortunately, the RAM market has proven itself to be very price elastic, creating new opportunities at each price level, thereby permitting the necessary increases in volume to keep the trend going.

The memory applications spectrum of Figure 13 indicates the broadening spectrum of the component market. At the left most end of the spectrum, technology improvements resulting in low cost are most significant, while at the right most end performance is key. In fact, the cache and 2900 (4 bit slice) market have previously been dominated by bipolar memory due to the inability of the MOS memory to meet the speed performance required. The introduction of scaled technology is currently permitting N-channel silicon gate MOS to enter this market segment.

MOS-MEMORY APPLICATION SPECTRUM

Figure 13

	PERFORMANCE				
COST	ELECTRONIC GAMES	MICROPROCESSOR APPLICATIONS	MINI COMPUTERS	MAINFRAME COMPUTERS	CACHE MEMORY
PERFORMANCE	1 μ S-450nS	450-200nS	250-150nS	200-100nS	100-30nS
PRODUCT	RAM ROM EPROM	SRAM ROM EPROM	D RAM --- ---	D RAM CCD ---	D/S RAM ---

MOSTEK will soon introduce several new products which utilize state of the art design techniques as well as the scaled Poly 5 process to expand our penetration into the memory application spectrum.

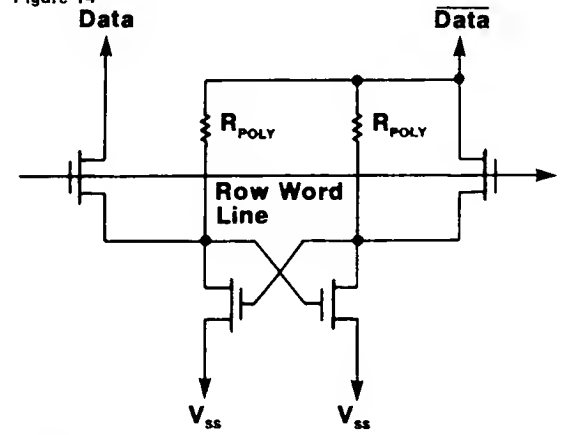
NEW GENERATION PRODUCTS MK4801

The MK 4801 is a 1Kx8 very high performance static RAM. This device combines a new circuit design technique (address activation) with enhanced process technology to achieve sub 100 nanosecond performance. The circuit will have speed grades available from 55 to 90 nanoseconds, with higher performances available in 1979. As all new static RAM products from MOSTEK, the 4801 can be manufactured on the Scaled Poly 5 or Poly R process. A typical access/cycle time of 75 nanoseconds at 200 milliwatts dissipation has been measured on devices manufactured on Poly R.

The 4801 uses a unique storage cell design to achieve a very small die size. Figure 14 illustrates this cell. The cell, a mere 2 mil², yields a die size of 27,900 square mils when utilizing 5 micron design rules, ala MK 4104. The design technology used yields approximately a 2 times density improvement on the standard process when compared to current generation 4K devices. Application of the Scaled Poly 5 process reduces this die size to approximately 14,000 square mils as well as significantly enhancing performance. Results similar to the 9009 R&D project are anticipated. The 4801 is architected for speed. The Address Activated™ interface permits asynchronous operation for the user while maintaining internal advantages of clocked circuit technology. A fast chip select path was designed to permit external decoder delays without impacting access time. The 4801 has been designed for use in all wide word high performance RAM applications.

HIGH PERFORMANCE 4801 2 MIL² STATIC RAM CELL

Figure 14



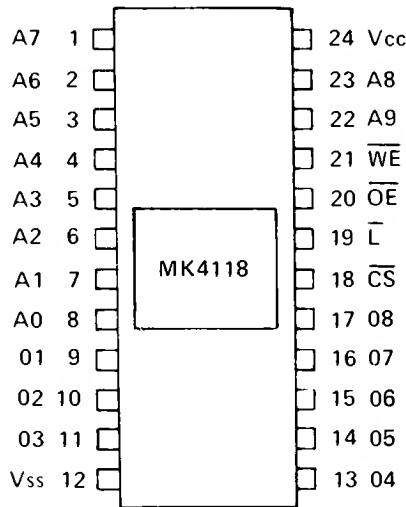
TECH
NOLOGY

MK 4118

The MK 4118 is a sister part to the MK 4801. The part is intended for medium to low speed applications. This device was architected with next generation as well as existing microprocessors in mind. Speed grades of 120 to 250 nanoseconds will be available. An output enable (\overline{OE}) and latch (\overline{L}) function has been included to permit use with common address and data I/O, 16 bit microprocessors. The MK 4118 is packaged in the industry standard 24-pin ROM/PROM compatible configuration shown in figure 15. The device is socket compatible with the 4801 and gives the user a static RAM configuration covering applications from 55ns through whatever. The MK 4118 can be used in an asynchronous mode, like the 4801, or a synchronous mode similar to the MK 4104. The part employs a function called Latch to accomplish the synchronous mode. When activated, LATCH will latch the status of the address and chip select pins. This easy to use memory packages 8K of RAM in an area comparable to a 4K device.

MK4118 PIN OUT

Figure 15



PIN NAMES

$\overline{A0} - \overline{A9}$	Address Inputs	\overline{WE}	Write Enable
\overline{CS}	Chip Select	\overline{OE}	Output Enable
\overline{DIN}	Data Input	\overline{L}	Latch
\overline{DOUT}	Data Output	$O1 - O8$	Data In/ Data Out Port
V_{ss}	Ground		
V_{cc}	Power (+5V)		

MK 4816

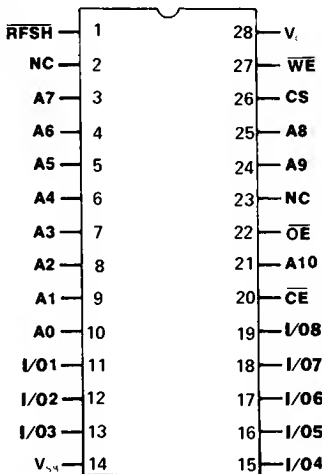
The MK 4816 is a 16K dynamic RAM organized as 2K x 8. The RAM operates with a single 5 volt $\pm 10\%$ power supply with performance in the 100-150ns region. Designed to function in cost sensitive wide

word applications the 4816 features several functions to enhance usability. The MK 4816 features a built in refresh mechanism controlled by an external pin called refresh. The refresh has two modes of operation; when the refresh pin is pulsed from high to low then back again an internal counter will replace external addresses and a RAM cycle occurs, refreshing one row of cells. This operation is repeated 128 times every two miliseconds. For standby mode operation the refresh pin may remain active. In this mode the MK 4816 will execute a refresh cycle approximately every 16 microseconds satisfying the data hold requirements with no external stimulus. This feature greatly simplifies control circuitry needed and eliminates all address multiplexer parts.

The MK 4816 employs an output enable function for common I/O operation and an extra chip select for multi-dimension selection. The 4816 employs MOSTEK's Edge Activated (TM) interface and operates with power dissipation of only 150 miliwatts when active and 28 miliwatts when in standby. The edge activated concept inherently features the address latch function required for common I/O machines such as the Z8000 and 8086. The MK 4816 packages 2K bytes of microprocessor memory in a die size of only 29K mil². This compares with competitive products supplying the same market with die sizes of about 25K mil² for 4K of static RAM or a total of 100 mil² of Silicon for the same bit density. The MK 4118 from MOSTEK reduces the Silicon area to 56K mil². The MK 4816 is packaged in the ROM/PROM compatible 28-pin configuration of figure 16.

MK4816 PIN OUT 5V ONLY DYNAMIC RAM

Figure 16



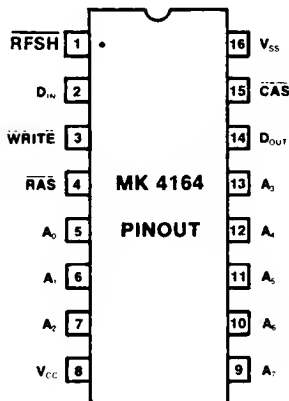
THE 64K RAM

In 1979 MOSTEK will sample a 5 volt only sub 100ns 64K RAM. The SCALED Poly 5 process developed in

1977/78 will be employed to make the 64K RAM a cost effective, produceable part. The 64K RAM will have a die size of approximately 35,000 sq mils permitting use of the industry standard 16-pin package. The pin out and key features are shown in figure 17. The pin configuration of figure 17 indicates that pin 1 is not needed in implementing the basic 64K RAM functionality. A new feature will appear at pin 1 which has not been implemented in previous generation RAMs.

MK4164 PIN OUT 64K RAM

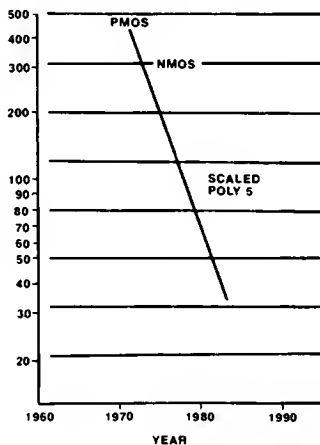
Figure 17



The design goal of the 64K RAM is to have 128 cycle refresh every 2ms making it compatible with its predecessor the 16K dynamic RAM. 128 refresh cycles require use of only 7 of the 8 address pins. To maintain refresh compatibility with previous generation dynamic RAMs, pin 9 (A₇) will not be used as a refresh address. The 64K being a scaled Poly 5 device will use 2 micron geometries. The device's dissipation will be a low 300mw at twice the operating frequency of the 16K. The MK 4164's performance evolution will follow the graph of fig 18.

PROJECT ACCESS TIME FOR DYNAMIC RAMS

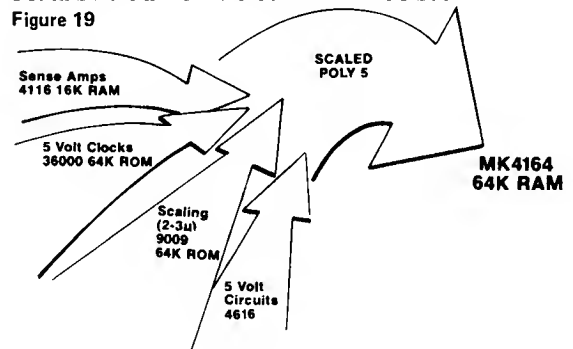
Figure 18



The 64K RAM design and process represents a convergence of several developments at MOSTEK during the past several years. The techniques needed to achieve a useable 64K RAM, required several breakthroughs which are currently being proven on predecessor parts. Figure 19 illustrates the evolutionary process required to develop this major product.

SCALED POLY 5 EVOLUTION PROCESS

Figure 19

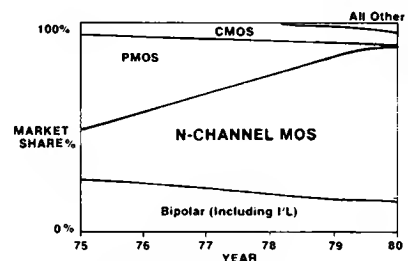


CONCLUSION

N-channel Silicon Gate MOS will continue to dominate the memory market. New technology breakthroughs such as Scaled Poly 5 and Address Activated design techniques will permit NMOS to conquer new market segments. Smaller die sizes and increasing volumes will continue to reduce costs, thereby further expanding the market. The chart of figure 20 illustrates the memory market share by technology. In conclusion, N channel MOS will continue to expand its application spectrum and remain the dominant technology in the 80's.

MEMORY MARKET SHARE BY TECHNOLOGY

Figure 20



GLOSSARY OF PROCESS NAMES

- SPIN - Metal gate N channel process. (Self-aligned Poly Interconnect N-channel)
- POLY I - Single level Poly N-channel Silicon gate
- POLY II - Double level Poly N-channel Silicon gate
- POLY R - Single level Poly N-channel Silicon gate incorporating Poly Silicon Resistive loads.
- SCALED POLY 5 - Double level Poly N-channel Silicon gate ion implant.

MOSTEK®

WIDE-WORD RAMS

Technology

INTRODUCTION

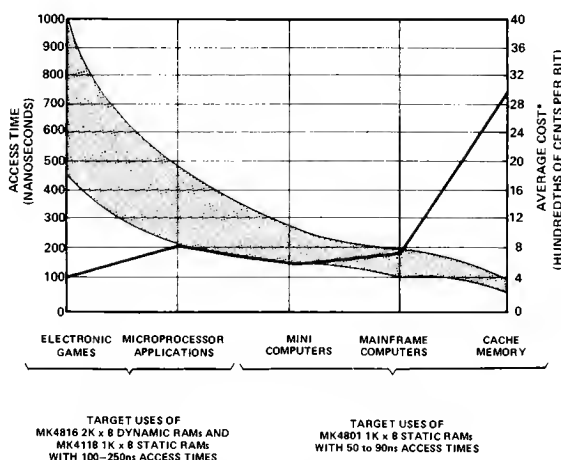
Until recently most leading-edge memory chips have been designed primarily for large mainframe storage. To use them in microprocessor systems required not only considerable adaptation but also additional ICs to interface the memory chips. But now comes a new breed of smart memory chips—a 2-k x 8 dynamic RAM and two fully static 1-k x 8s—specifically designed for μ P applications, and cache memory uses as well.

While conventional memory chips can accept only read, write, and select commands, the smart memory devices do that and more: Besides accepting additional commands, they present parallel data on byte-wide outputs, and provide many other features for users, including the following:

- 5-V-only operation.
- Automatic power-down.
- Automatic refresh for dynamics
- ROM/PROM/EPROM compatibility.
- Output enable (OE) command.
- Chip select (CS) command.
- Latch command—for synchronous operation.

TODAY'S MEMORY-USE SPECTRUM

Figure 1



* (BASED ON ACTUAL INDUSTRY SURVEYS; SOME ANOMALIES ARE DUE TO COST VARIANCES IN CERAMIC vs PLASTIC PACKAGES, AND QUANTITY BUYS)

To see the design tradeoffs possible with this family, see Table 1.

The 16K dynamic MK4816 (with single-pin refresh) and the 8K static MK4118 can both be used readily with any of the present-generation and new generation MOS microprocessors such as the Z80, Z8000, 8085, and 8086. For high-performance applications, another 8K static (MK4801) provides a choice of 55, 75, and 90-ns access times.

The new parts are configured as 1024 words x 8 bits in fully static designs or as 2048 words x 8 bits in an internally refreshed format. The refresh timing cycles are supplied by the chip itself and are largely transparent to the user. Whatever the configuration, the Mostek RAMs typically dissipate a low 200 to 300 mW of power, and offer fast data access down to 55ns.

THE MEMORY-USE SPECTRUM

The impact of this family cannot be appreciated fully without noting that semiconductor memory applications cover a broad spectrum, from low-speed uses in games to very high-speed applications in cache memory. For μ P applications, medium-performance RAMs generally suffice, and cost is a major selection factor. But as Fig. 1 shows, cache memory users pay a higher price for high speed.

In the center of the spectrum is main-store memory, which has relatively balanced density, performance, and cost requirements. A typical main-store memory is 32 bits wide and 1/2 to 1-million words deep. Memories this large (in fact, most memories larger than 64K to 128K bytes) warrant some sort of error-detection/error-correction scheme, which favors a "by 1" or serial-output memory device.

So far, the NMOS dynamic RAM using address multiplexing and a "by 1" bit-serial organization has been the most efficient and cost-effective for main memory. So long as the needed memory depth is greater than the depth of the available by-1 memory chips, the by-1 minimizes the number of lines, the input and output capacitances, the pin count, the board area and the cost. However, while by-1 RAMs are excellent for conventional main storage applications, they are less than attractive for many others.

The most dynamic growth over the past four years has come from electronic games and μ P-based products. Increased use of memory in such systems has been the

WIDE-WORD DEVICES—A RESPONSE TO CHANGING NEEDS

As the spectrum of microprocessor applications continues to expand and as high-speed, general-purpose computers continue to grow, the semiconductor industry is preparing for a surge in memory demand. Designing products that will ease the system designer's work, the industry is providing the most cost-effective, highest-density and highest-performance memories ever.

Bit density for semiconductor memory has increased steadily and quickly since the integration of an R-S flip-flop into the integrated circuit. In just 15 years, single-bit memories have given way to 64-K bit memories. There was one goal behind this evolution: Replace core-implemented main memory with something cheaper and smaller.

added for single-step capability. The 8085 also interfaces easily by taking advantage of the 8085's status bits (S_0 and S_1) to refresh the MK4816 following each instruction fetch.

Latched refresh is particularly easy to implement in microprocessor systems since RFSH can be delayed slightly from \overline{CE} to accomplish asynchronous refresh in minimum time. The MK4816 may also be used in multiplexed data and address systems, with the \overline{OE} pin for control, and in CRT systems where the normal sequential addressing automatically refreshes the memory by addressing all positions within 2ms.

While recognizing that clocked, dynamic RAMs with automatic refresh will clearly be the most cost-effective byte-wide RAM for use with microprocessors, MOSTEK has also developed two fully static 1K x 8 RAMs. Functionally alike, and identical in pinout, the 4801 and 4118 differ only in production process and in speed.

BIT DENSITY WAY UP

With a die the same size as the 4816's and using the standard N-channel production process and tolerances, the 4801 typically runs a 50 to 90ns access/cycle with typical power of 250mW. This means an 8-to-1 increase in bit density per chip over the 93415 bipolar 1K x 1, and 15-to-1 decrease in system power per bit.

Low power and high speed are achieved using a 2-mil² cell that eliminates connections to Vcc. Power is fed to the cell from the column lines, through 1-nA intrinsic poly load resistors (see Fig. 5).

This economical design limits the matrix current to just 8 μ A. Column and row decoders are modified tree decoders (Fig. 5) that dissipate only leakage current in both active and standby modes.

The key to the 4801's high speed is an ECL-style linear differential amplifier for sensing the column signal (Fig. 5). The differential amplifier's output is amplified and translated to full TTL levels with a strobed differential latch. The strobe signal, derived by sensing an address change or address activation, allows fully static ripple-through operation.

But core replacement is no longer a problem. Now the concern is differing consumer/industrial memory requirements. Where typical μ P systems have a more fixed need for memory per CPU at lower cost per bit, cache and scratchpad memories require very high performance, with less emphasis on cost. The result? High-speed, but low-cost MOS RAMs—both dynamic and static.

The new dynamic and static chips are configured in a "by 8" or "byte-wide" organization. They will be effective for those applications outside main store memory where a "by 1" bit organization is either not attractive technically (because of system constraints such as power) or not efficient for implementing wide-word shallow memories.

Since a completed cycle results in automatic chip power-down until the next address change, the user doesn't have to deselect the chip, but can use the simple, fast \overline{CS} . The result is a chip that is as easily used for retrofit as for newer clocked systems.

Some very useful features on both the 4801 and 4118 increase their flexibility. As shown in Fig. 10 several control functions have been added. In addition to the normal R/W, and \overline{CS} (chip select) there is also \overline{OE} (output enable) and L (latch). Both L and \overline{OE} inputs may be used to simulate a clocked RAM for easy interface to any μ P (see Table 2).

The 4801 and 4118 may be tied to any μ P or mini bus without SSL interface devices. The pinout, like a 2708's or 2758's may be used interchangeably with EPROMs or bipolar PROMs to assist in μ C product development (see pinout in Fig. 2).

Besides being able to interface easily in a "clocked" mode, both the devices may also be used as fully static ripple-through RAMs. The latch input may be tied high, \overline{OE} low, and the part can be used to replace directly eight 93415/425s, eight 2102s or two 2114s. This means existing designs can be upgraded for improved density, power and cost.

Some conflicts occur when these common-I/O three-state RAMs are used to replace separate I/O open drain/collector products. But these are painlessly resolved by correctly using \overline{OE} , the latch input, or both. But even without \overline{OE} , and even when RAMs with access times of 50 and 90ns are used in parallel, bus conflicts are resolved on-chip. During read accesses, the outputs of the 4801 are first opened at 30% of TAA and closed later in the cycle. Similarly, the tON time transition of \overline{CS} is slower than tOFF (\overline{CS}). Holding the R/W pin low for a write cycle unconditionally opens outputs in 20ns.

The 4801 can be used with popular minicomputers that time-multiplex the address and data by having the latch input trap addresses and \overline{CS} . Data inputs are trapped on the rise of R/W during a write cycle.

Available at speeds as low as 55ns max, the 4801 is the first high-speed, byte-oriented memory chip. Two important applications for this high-density 1K x 8 RAM

TRUTH TABLE FOR 4801/4118 1K x 8 RAMs
Table 2

\overline{OE}	\overline{WE}	\overline{CS}	Latch	Mode	Output	Power
L	H	L	H	Read Select	D_{OUT}	Address Activated
L	H	H	H	Read selected	Open	Address Activated
H	X	X	H	Chip deselected	Open	Address Activated
L	L	X	H	Write address & \overline{CS} latched until cycle terminated by $\overline{WE} \rightarrow H$	Open (D_{IN})	Active
—	—	—	L	Latches addresses and \overline{CS} at state present when latch switched low	See above	Standby

are cache and read/write microprogram memory for efficient emulation of different instruction sets with a bit-slice μP . Both applications require fast read cycles, while caches need a fast write cycle as well. Typically, the depth of these memories is shallow, less than 16-K, with words that can be 72 to 100 bits wide. For these applications, the by-8 organization makes the 4801 ideal.

Consider \overline{CS} . There has lately been much interest in using this pin to power-down the chip on by-1 memory parts. This is done in Intel's 2147 4K x 1 but only by making \overline{CS} delay similar to tAA.

On the 4801, \overline{CS} gates the outputs only and inhibits write when disabled. Since \overline{CS} delay is just 30% of tAA, memory depth can be expanded incrementally from 1K

up without the additional delay of a decoder to allow memory expansion. Further \overline{OE} is provided to assure that three-state can be used rather than open collector and to resolve the problem of two chips being on simultaneously.

In the write mode, addresses and \overline{CS} are automatically latched on the selected chip when R/\overline{W} goes low, which avoids the early write of a previously selected cell when entering a write cycle. On a typical static part, every address bit must settle and write before any bit change. But autolatch on the 4801 chip can substantially improve skew sensitivity of write timing relative to address. Further, the addresses are internally held after R/\overline{W} goes high for as long as the chip needs to complete the write cycle.

Meanwhile, the addresses on the bus may be changed in preparation for the next read or write cycle. This also relieves the address-to-write skew on the trailing edge of write.

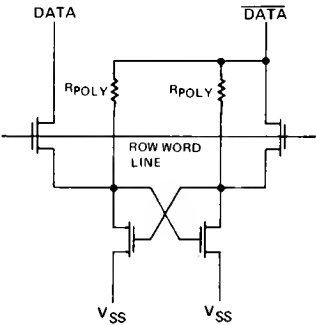
Loading on the address lines is significantly improved by replacing eight 93415s with one 4801 or 4118. This also improves board density 4-to-1 (since the 4801 is in a 24-pin package) and pin count by 5-to-1.

The 4118 is slower than the 4801, but it's also more economical. It has the same pinout and operates in the same modes. The differences stem from the process technologies that are used to manufacture two devices.

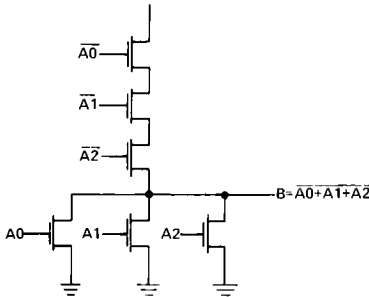
Since the 4801 is intended for high-speed, high-performance applications, it is offered in 55, 75, and 90ns speed selections and is manufactured using Mostek's new "Scaled Poly 5"™ technology, which will eventually reduce chip size to approximately 14,000

MK4801 STATIC RAMs 55ns ACCESS TIME
Figure 5

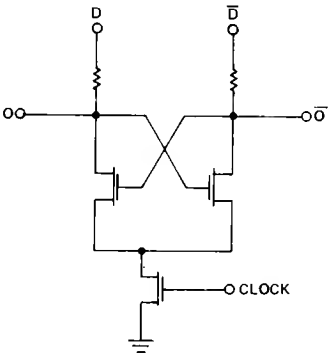
2 MIL² STATIC RAM CELL



ZERO-POWER "TREE" DECODER



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TECH-
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CHARACTERISTICS OF NEW BYTE-WIDE RAMs

Table 1

Type Number	Memory Organization	Process/ Pinout	Access Time	Unique Features	Other Leading Features
MK4816	2K x 8 Dynamic	N-Channel Si gate 28 pin	150 typ	First byte-wide dynamic First 5V only dynamic First one-pin refresh	Edge activated™ 150mW active, 25mW standby Competes with 2102 and 2114, statics, cutting cost and space
MK4801	1K x 8 static	Scaled Poly 5 24 pin	55 75 90	First 2 mil ² static RAM cell Fast as the 4K x 1 2147	Fully static, 250mW typical Double capacity at double speed, compared to 4K statics now dominant
MK4118	1K x 8 static	N-Channel Si gate 24 pin	120 150 200 250	Faster than the X8s now available	Fully static Lower cost than 4801 Competes with 2102 and 2114 static, cutting cost and space

key item in penetrating low-cost/high-volume markets. As a result, both general-purpose minis and dedicated microcomputers have come down in price while staying functionally equivalent. Indeed, CPU cost is so low in this area that μ P system costs tend to be in proportion to memory requirements.

Until the 2114 (1K x 4) static RAM, it took eight 2102-type RAMs to implement 1K x 8 of memory. Before the 2114, few RAMs were designed to interface directly with a microprocessor, because chip designers concentrated on the processors themselves. Even the better RAMs would not work with all processors.

ROM and PROM grabbed a lot of attention because of their nonvolatility, which was needed for fixed instruction set storage, usually a bigger requirement than RAM. ROMs and PROMs have always been "by 4" or "by 8" because of the convenience of putting instructions in the least amount of packages.

WHY BYTE-WIDE RAMS?

Recently however, three trends have stepped up the demand for wide-word RAMs—declining cost of μ Ps, further improvements in memory density and cost, and the emergence of high-volume dedicated-computer markets such as the automotive market. Such applications as μ P memory, CRT refresh memory, CRT buffer memory—being very shallow—all lend themselves to a "by 8" memory organization and its minimum number of packages.

Cache memory, high speed buffer memory, writable control store, scratchpad memory and terminal/communications buffer memory stress speed much more heavily than cost. Fast bipolar memories have usually been used here, at the expense of package count, cost, and high power. However, recent technological innovations such as scaling and the four-transistor (six-element) static cell concept enable MOS memories to compete with bipolar for cache.

Though cache applications have a large number of bits, there are usually a small number of words; that is, they

are wide but shallow memory matrices. For instance, a typical cache memory in a minicomputer is 32 bits wide but only 2K to 4K words deep. Clearly, a wide-word memory chip is most efficient here.

MK4816—FAST BUT LOW-COST

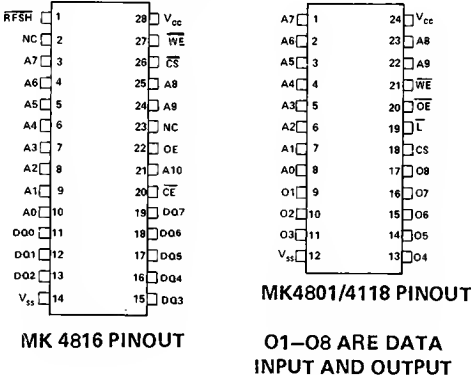
The MK4816 16K dynamic RAM is the first 5V-only dynamic MOS memory. It's also the first wide-word dynamic RAM, and the first RAM designed specifically for present and future microprocessor systems. Using small dynamic-memory cells offsets the cost of the slightly greater overhead circuitry required for proper operation of dynamic memories.

The MK4816 is designed to minimize the off-chip support circuits, while maintaining the internal efficiency of a dynamic RAM. Its cell size is three times smaller than in typical static cells, while its die size—29,000 mil²—approaches that of 4K static RAMs. Built with standard N-channel silicon gate technology, the device requires only a single +5V power supply.

High speed, low-power operation stems from edge-activated dynamic logic, which produces a typical

16K DYNAMIC RAM MK4816

Figure 2



access time of 100ns at a power-dissipation of only 25mW standby and 150mW active.

System-oriented features include single-pin refresh, automatic refresh in battery back-up mode, and common data I/O. Full TTL compatibility is also provided on all inputs and outputs. See Fig. 2 for the pinout.

The MK4816 can handle a variety of read, write, and refresh cycles. Read and write cycles are initiated by the falling edge of chip enable (\overline{CE}) which also latches the state of 11 address inputs and the chip select input. In a read cycle, data become valid after one access time assuming that both \overline{CE} and \overline{OE} (output enable) are low. After the data are read or written, the memory returns to a precharged condition.

After it's fully precharged, the internal logic will initiate a refresh cycle, provided the \overline{RFSH} pin is brought low during the previous cycle. Waveforms for this type of latched-refresh cycle, together with those for typical read and write cycles, are shown in Fig. 3. Since the single-refresh step renews the charge in only one row of the RAM matrix, 128 such steps must take place every 2ms.

Although latched-refresh operation is particularly convenient for achieving refresh in minimum time, the chip may also be refreshed simply by clocking the \overline{RFSH} pin 128 times every 2ms, while \overline{CE} remains high. In this as in all types of refresh cycles, addresses are generated internally and automatically incremented and stored at the end of each refresh cycle. Since the on-chip refresh function in the 4816 uses an extremely small part of chip area, it's clear that, at least for wide-word RAMs, refresh is more efficiently performed on-chip.

Ultimately, the single-pin refresh concept could be extended to fully static operation, by means of an internal oscillator to generate refresh-request pulses at fixed intervals. But this function has not been implemented on the MK4816 because of the long access and cycle times involved and because arbitration logic always has some finite probability of indecision. In such "hidden refresh" designs, if an external cycle is requested at precisely the same time as an internal refresh request, arbitration logic allows either cycle to go ahead, with the other immediately following. From a user's viewpoint, such a "hidden-refresh" device appears totally static with an access time equal to one refresh cycle time plus a normal access time.

Instead, the 4816 has a battery back-up or self-refresh mode, which is initiated after \overline{RFSH} has been low for about 15 μ s. During the self-refresh mode, the states of all inputs except \overline{RFSH} are ignored and refresh is performed automatically through refresh-request pulses derived from an internal oscillator. A rising edge on \overline{RFSH} terminates the self-refresh mode and active read or write cycles can follow after one cycle time.

The self-refresh mode, with its fully automatic on-chip timing, is also particularly useful for single-step operation, since it is not necessary to provide external refresh pulses between instructions. The memory will always refresh itself independently of the time interval

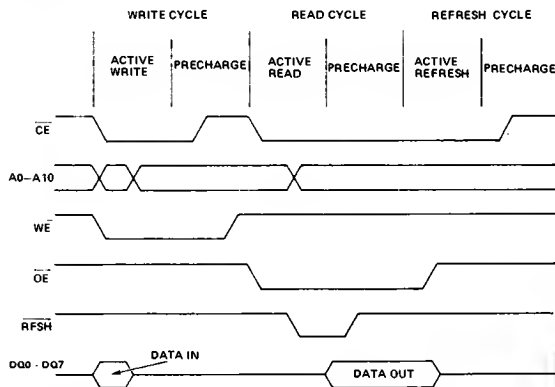
between clock pulses. Data can be read during the self-refresh mode since output data will remain valid throughout the self-refresh interval if \overline{CE} and \overline{OE} are held low.

The MK4816's memory matrix is structured around a single row of 128 sense amplifiers each fed by a balanced bit line loaded with 64 memory cells. Data from both ends of eight selected bits are amplified, latched and buffered into eight data I/O pins. Input addresses are derived from either the external address pins or the internal refresh counter. Refresh-request pulses controlling the refresh counter are derived either from the \overline{RFSH} pin itself or the internal oscillator, which also doubles as the charge pump for generating the negative substrate bias.

Architecturally, the MK4816 is easy to use with all microprocessors. As shown in Fig. 4, it can be connected directly to the Z80 with only one logic gate

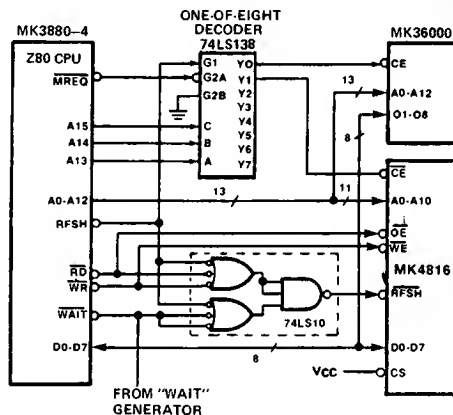
MK4816 2K x 8 RAM

Figure 3



Built-In Control Logic

Figure 4



mil². The 4118, on the other hand, will be run on Mostek's standard N-channel silicon gate production line and is intended for μ P applications calling for 10% power-supply tolerance, TTL compatibility, density, low cost, and easy interface. Its access/cycle times are 120, 150, 200, and 250 ns.

FUTURE TRENDS

Obviously, if history means anything, the trend toward higher density will continue—2K x 8 statics are under way and 16K x 1 are planned. These new static RAMs will eventually have to go to a 28-pin package, at least.

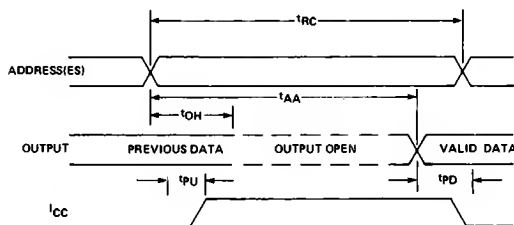
Dynamic byte-wide RAMs should also start proliferating. Since this market is geared to reducing space and cost, the dynamic, byte-wide trend may move into any of several directions. On one hand, semiconductor vendors are heavily involved in designing 64K x 1 dynamic RAMs. On the other hand, it is reasonable to expect that a family of devices will also emerge, organized as 4K x 8 and 8K x 8.

However, with rock-bottom cost and space weighing in more heavily than specific implementations, several vendors are considering clocked static RAMs with multiplexed data and address, which will reduce pin count considerably for specialized applications. With a multiplexing scheme, 1K x 8 of RAM could be in a 300-mil wide, 18-pin package.

Clocked multiplexed RAMs can be implemented two ways. One is to multiplex the eight outputs onto eight of the 10 address pins using two clock cycles—one for address and the second for data. But unless the data are unmultiplexed and remultiplexed off-chip to achieve 16 bits of address and data, data width will be limited to 8 bits.

MK4801/4118 BYTE-WIDE STATIC RAMs

Figure 6

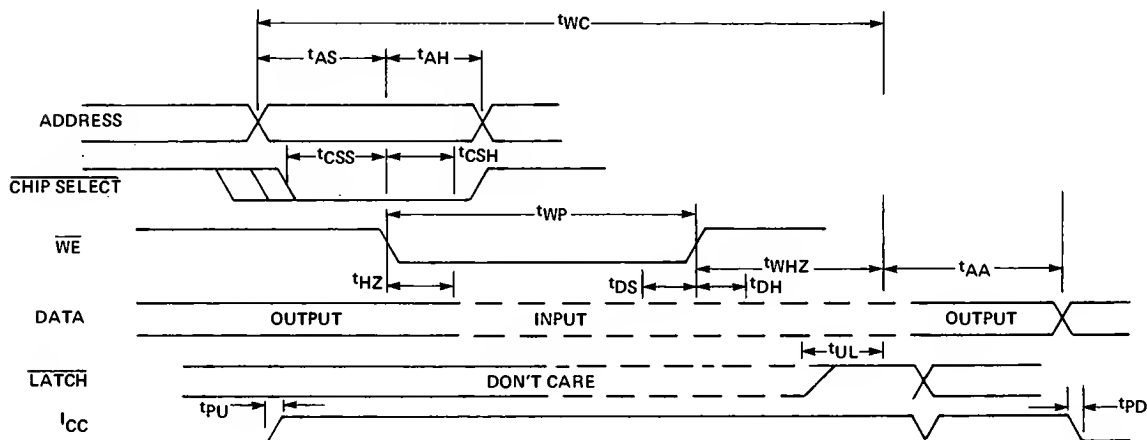


A better alternative is to multiplex eight bits of address, followed by eight more bits of address, and then multiplex eight data bits onto the same 8-bit bus, using hard-wire select to choose a given package. This method requires three clock cycles for eight data bits or four cycles for 16 data bits.

This latter concept, used successfully at the 4-bit level on the Intel 4004 μ P, can result in a very low-cost minimum-pin-count byte-wide memory with the best packing density. The most severe limitation (because of the number of clock cycles) would be lowered data bandwidth, but the success of multiplexed 16-pin dynamic RAMs and the demands for lower costs will outweigh this drawback.

WRITE-CYCLE TIMING OF 4801/4118 8K STATIC

Figure 7



1980 MEMORY DESIGNERS GUIDE

X	Dynamic Random Access Memory	DYNAMIC RAMS
XI	Static Random Access Memory	STATIC RAMS
XII	Read Only Memory	ROMS
XIII	Technology	TECH- NOLOGY
XIV	Memory Systems	MEMORY SYSTEMS

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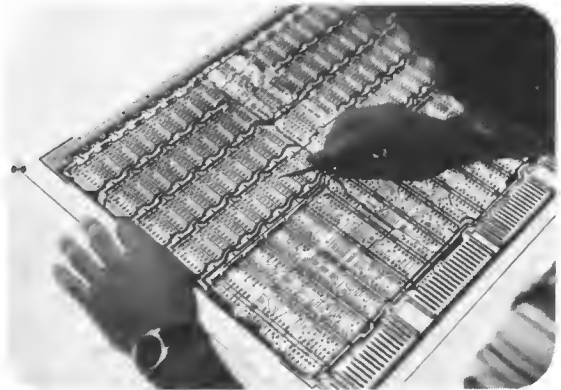
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	Make	Buy
Cost	Variable—affected by inflation Estimate often low, G&A and overhead not considered	Known and exact
Delivery	Subject to internal scheduling priorities	Certain—set by contract
Inventory	Maximum—typically 60 POs for each memory type	Minimum—one item required
Overhead	Maximum added	Minimum added
Design Experience	Variable	Team of engineers specialized in memory designs
Warranty	Absorbed by manufacturer	One year
Capital Resources	Must be spent on special test equipment and fixtures	Available for alternate uses.

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